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Upgrade of the ATLAS Tile Calorimeter Electronics

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Abstract. The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region of the ATLAS experiment at LHC. The TileCal readout consists of about 10000 channels. The bulk of its upgrade will occur for the High Luminosity LHC phase (Phase-II) where the peak luminosity will increase 5 times compared to the design luminosity (10^{34} $cm^{-2}s^{-1}$) but with maintained energy (i.e. 7+7 TeV). An additional increase of the average luminosity with a factor of 2 can be achieved by luminosity levelling. This upgrade is expected to happen around 2024. The TileCal upgrade aims at replacing the majority of the on- and off-detector electronics to the extent that all calorimeter signals will be digitized and sent to the off-detector electronics in the counting room. To achieve the required reliability, redundancy has been introduced at different levels. Three different options are presently being investigated for the front-end electronic upgrade. Extensive test beam studies will determine which option will be selected. 10 Gbps optical links are used to read out all digitized data to the counting room while 5 Gbps down-links are used for synchronization, configuration and detector control. For the off-detector electronics a pre-processor (sROD) is being developed, which takes care of the initial trigger processing while temporarily storing the main data flow in pipeline and derandomizer memories. One demonstrator prototype module with the new calorimeter module electronics, but still compatible with the present system, is planned to be inserted in ATLAS this year.

1. Introduction

The Tile Calorimeter [1] (TileCal) is a sampling hadronic calorimeter which covers the most central region of the ATLAS [2] experiment at CERN. TileCal detector is made out of steel absorber plates and plastic scintillator and it is divided in three cylindrical parts along the beam axis as figure 1a shows: a central Long Barrel (subdivided in Long Barrel A and Long Barrel C) and two Extended Barrels (Extended Barrel A, Extended Barrel C). Each barrel is composed of 64 modules which are divided in cells. The PhotoMultiplier Tubes (PMTs) and on-detector electronics used to read out the cells are hosted in the outermost part of the modules, called drawer, as figure 1b shows. TileCal contains a total of 256 drawers comprising ~10000 readout channels.

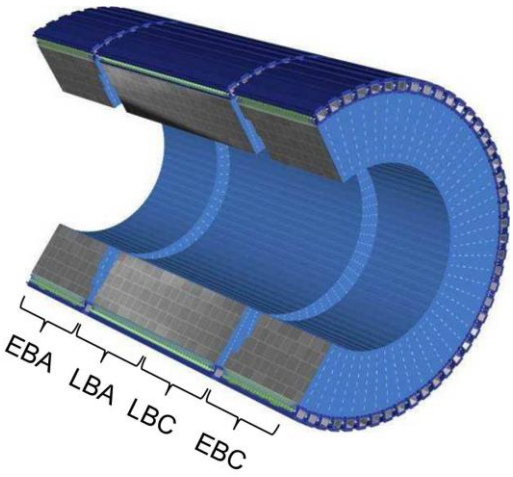

Figure 1a. Tile Calorimeter detector

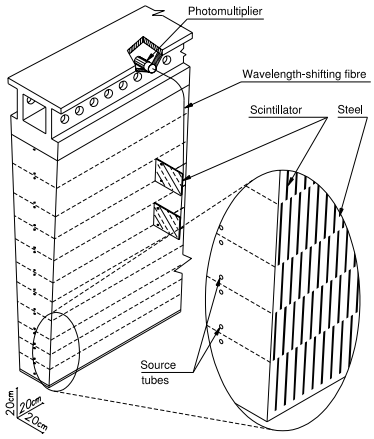

Figure 1b. TileCal module

Light generated by charged particles crossing the plastic scintillating tiles are collected by wavelength shifting fibres and carried to the PMTs. The analog signals produced by PMTs are conditioned and digitized by the on-detector electronics every 25 ns, while analog tower sums are transmitted to the Level-1 trigger system for trigger decision. Once the on-detector electronics have received the Level-1 trigger accept signal, the digitized data for the selected event is transmitted to the off-detector electronics.

In the off-detector electronics, the Read-Out Drivers (ROD) [3] receive the digitized data coming from the on-detector electronics at a maximum Level-1 trigger rate of 100 kHz. RODs are in charge of performing data processing tasks in real time and sending the processed data to the Read-Out Buffers (ROB) in the Level-2 trigger. A total of 32 ROD modules are needed to read out the ~10000 channels.

Figure 2 shows the dataflow of the current readout architecture.

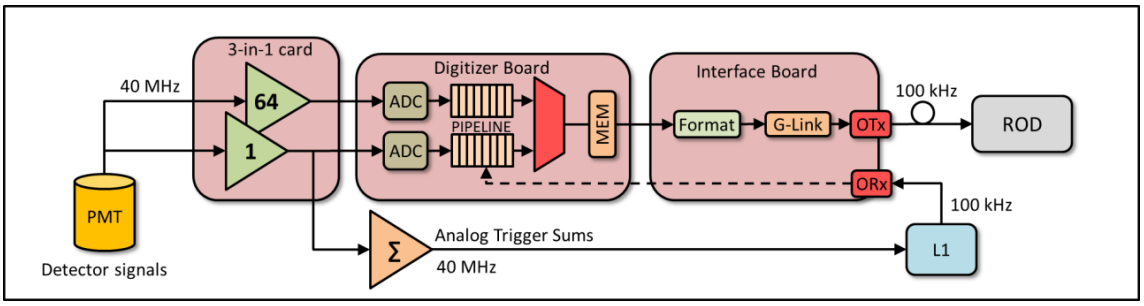

Figure 2. Present Tile Calorimeter readout architecture

2. Tile Calorimeter Upgrade plans for HL-LHC

The Phase-II Upgrade [4] of the LHC, called High Luminosity LHC (HL-LHC), is scheduled around 2024 and plans to increase the luminosity to a value of around $5\text{-}7\cdot10^{34}\text{cm}^{-2}\text{s}^{-1}$ with a pileup close to 200 events in order to reach a total integrated luminosity of 3000 fb^{-1}.

A full redesign and replacement of the readout electronics of TileCal is mandatory due to the increase of radiation level and the implementation of a new readout architecture with a full-digital trigger system raising the total bandwidth from 165 Gbps up to 80 Tbps. With the purpose of operating with high radiation doses, the new readout electronics system will include redundant optical fibers between on- and off-detector electronics, radiation-tolerant electronics, redundant low voltage power supplies and will use reliable protocols with error correction for data transmission.

The readout architecture for Phase-II points to a full digital readout where the on-detector electronics will transmit digital data from all the channels to the off-detector electronics for every

bunch crossing. Then, the off-detector electronics will pre-process and transmit the data to the first level of trigger with improved precision and granularity.

Figure 3 shows a diagram of the upgraded TileCal readout architecture for the HL-LHC.

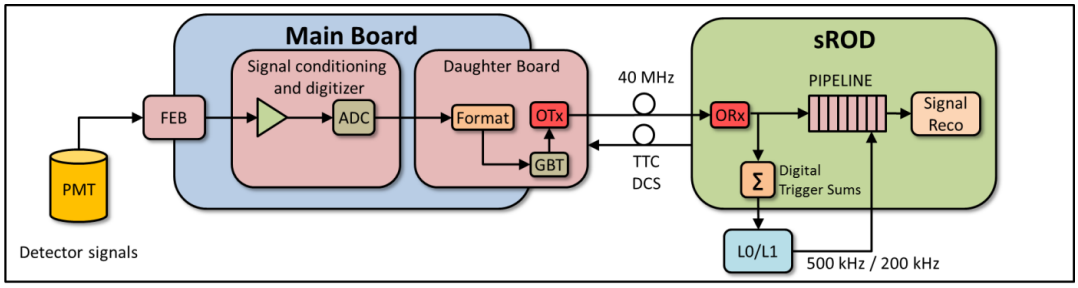

Figure 3. Upgraded Tile Calorimeter readout architecture for HL-LHC

2.1. The Tile Calorimeter Demonstrator Project

The Tile Calorimeter Demonstrator Project activities are intended to evaluate and qualify the new electronics before the complete replacement of the on- and off-detector electronics for Phase-II Upgrade. These activities not only comprise the development and test of electronics which fulfil the future conditions, but novel trigger algorithms, monitoring and control software and new mechanics.

Furthermore, the Demonstrator Project plans to replace one of the TileCal drawers with the new electronics and install it into the detector during the Long Shutdown 1 (LS1) scheduled for 2013-14. Since the interface of the current Level-1 trigger system is analog, the Demonstrator drawer will provide analog trigger signals keeping backward compatibility with the present system. Due to this functionality, this upgraded drawer is so-called hybrid drawer.

3. Tile Calorimeter electronics for HL-LHC

3.1. On-detector Electronics

As figure 3 shows, Front-End Boards (FEB) are connected directly to the output of the PMTs and provide conditioned signals to the readout electronics in the Main Board, integrated data for minimum bias monitoring and electronics for the calibration of PMT gains. The Daughter Board is responsible for gathering and transmitting the digitized data to the off-detector electronics.

3.1.1. Front-End Boards

Three FEB options are being evaluated for the HL-LHC. The first FEB option is an improved version of the present 3-in1 card [5] designed by the Enrico Fermi Institute of the University of Chicago. This FEB has been designed using Commercial Off-The-Shelf components and provides analog outputs with two different gains, as well as calibration capabilities for PMTs. The modified 3-in-1 card shows better linearity and lower noise than the current version and has passed successfully the radiation tests.

The second option is a custom ASIC called Charge Integrator and Encoder (QIE)[6], developed in joint collaboration between the Argonne National Laboratory (ANL) and Fermilab. The QIE ASIC divides the signal coming from the PMTs with a current splitter followed by a gated integrator providing four different ranges (16/23, 4/23, 2/23, 1/23). A 6-bit flash ADC digitizes the selected range covering a dynamic range of 17 bits. The QIE version 10.5 also includes a Time-to-Digital Converter (TDC) with sub-nanosecond resolution for out-of-time pulse identification.

The third option for the FEB is an ASIC called Front-end for ATLAS TileCal Integrated Circuit (FATALIC) [7] developed by The Laboratoire de Physique Corpusculaire de Clermont-Ferrand (LPC). FATALIC includes a 3-gain current conveyor associated with shaping stages which covers the full dynamic range of the PMT signal. Three 12-bit ADCs, designed by LPC and called Twelve bits ADC for s-ATLAS TileCal Integrated Circuit (TACTIC), read out the conditioned signals from the

current conveyor stage. Both chips have been designed using the IBM 130 nm CMOS technology. Final version of FATALIC will combine both ASICs functionalities in a single chip.

The modified 3-in-1 card has been selected as FEB for the hybrid drawer, since it is the unique FEB which provides analog outputs required for the current trigger system.

3.1.2. Main Board

The Main Board is responsible for the control, monitoring and readout of the FEBs and low voltage power supplies, and provides a digitized data to the Daughter Board. Three different types of Main Board will be designed in order to evaluate the three FEB options.

The Enrico Fermi Institute has designed the Main Board that will be used in the Demonstrator Project which is able to host and manage up to 12 modified 3-in-1 cards, so one drawer will include four Main Boards. This Main Board includes 4 Altera Cyclone IV FPGAs for control and configuration purposes, and 12-bit Linear Technology LTC 2264 ADCs for the digitization of the analog signals. The Main Board is functionally divided into halves each of them hosting 6 FEBs. Each half has a separated low voltage power supply and is diode-ORed with the other half, ensuring the completely functionality if the power supply for one half stops working. Figure 4 shows a picture of the first Main Board prototype for the Demonstrator.

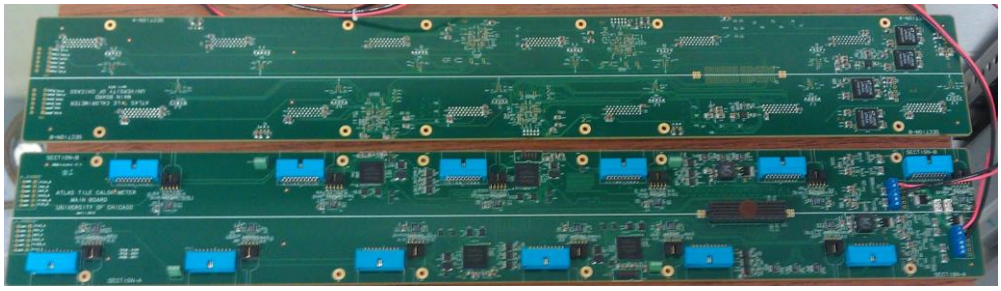

Figure 4. First prototype of the 3-in-1 Main Board

3.1.3. Daughter Board

The Daughter Board [8] is in charge of the high speed communication between the on- and off-detector electronics in the counting room. The Daughter Board collects, formats and transmits the data to the off-detector electronics using redundant high speed links at data rates of 10 Gbps. It also implements slow control functionalities as the distribution of Detector Control System (DCS) commands needed for the control and monitoring of the Main Board and the high voltage power supplies.

The Daughter Board has been developed by the Stockholm University. The third generation of the Daughter Board includes two Xilinx Kintex 7 FPGAs, two Quad Small Form-factor Pluggable (QSFP) optical modules, two GBTx chips and an FPGA Mezzanine Connector (FMC) for the communication with the Main Board. Figure 5 shows a picture of a third generation Daughter Board.

Figure 5. Third generation of the Daughter Board

3.2. Off-detector Electronics

The super Read-Out Driver (sROD) [9] is the key component of the off-detector electronics. This system is responsible for receiving and processing the data coming from the detector, sending pre-processed data to the trigger system, interfacing the DCS and the on-detector electronics, as well as the reception and distribution of Trigger, Timing and Control (TTC) information towards the detector.

The sROD demonstrator module, developed by the IFIC-Valencia group, is a prototype for the Demonstrator Project able to read out a complete hybrid drawer. The sROD demonstrator board has been designed in a double mid-size Advanced Mezzanine Card (AMC) form factor which can be plugged in an Advanced Telecommunications Computing Architecture (ATCA) carrier or in a Micro Telecommunications Computing Architecture (μTCA).

This module contains two FPGAs for data processing: one Xilinx Virtex 7 and one Kintex 7 FPGAs with embedded GTX transceivers capable of data rates above 10 Gbps. Figure 6 shows the connectivity between the two FPGAs and the optical modules and peripherals. The Virtex 7 FPGA is connected to 4 QSFP modules providing high speed communication with the on-detector electronics at a maximum data rate of 160 Gbps in each direction. This FPGA performs signal reconstruction algorithms and handles the communication between the DCS and the on-detector electronics.

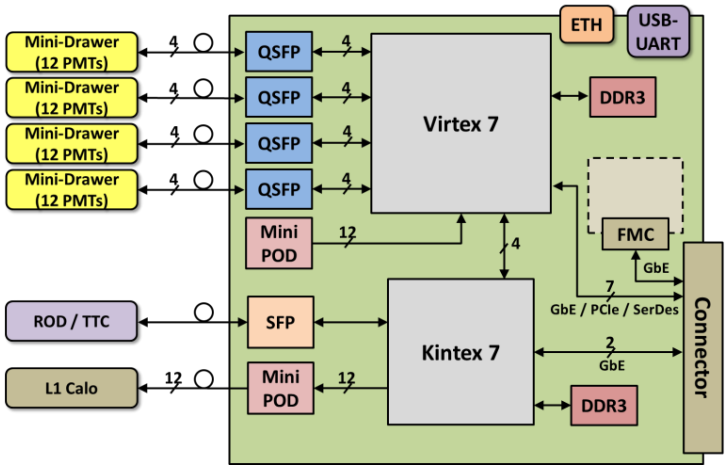

Figure 6. Block diagram of the sROD demonstrator

A Small Form-factor Pluggable (SFP) module connected to the Kintex 7 interfaces the hybrid drawer with the current system, sending data from the hybrid drawer to the present RODs and receiving TTC information which is decoded in the Kintex 7. The Avago MiniPOD transmitter is used to transmit the pre-processed data to the trigger system from the Kintex 7 FPGA. Figure 7 shows a picture of the PCB of the sROD demonstrator.

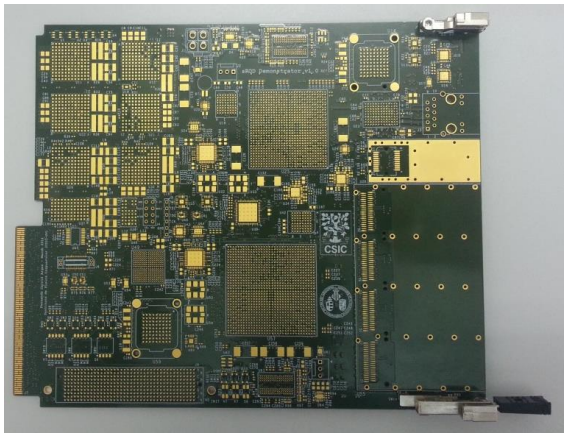

Figure 7. sROD demonstrator module

3.3. Optical Links

QSFP modulators based on Mach-Zehnder interferometers from Luxtera will be used as data links between the on- and off-detector electronics at data rates of 40 Gbps per module [10].

Several radiation tests carried by ANL have shown that while electro-optical chip exceeds the required radiation levels, the microcontroller used to configure and monitor the QSFP module does not fulfil the requirements to operate into the detector. For that reason, flash-based FPGAs are being evaluated to replace the original radiation soft microcontroller.

4. Conclusions

The increased luminosity for the HL-LHC implies the complete redesign of all the readout electronics in TileCal. The new readout architecture will include a full digital readout and trigger fitting the new requirements in the future HL-LHC.

The Demonstrator Project aims to gain experience and evaluate the new electronics before its full replacement around 2024. This project plans to install a hybrid drawer with the new readout electronics into the detector during the LS1 and based on the results more upgraded drawers could be installed during the next Long Shutdown 2 scheduled for 2018-2019.

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