Miniature fuel cell with monolithically fabricated Si electrodes - Uniformity of Catalyst Layer Thickness -

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Abstract. Uniformity of catalyst layer thickness was improved to obtained higher output with our miniature fuel cells. Though the miniature fuel cells demonstrated high power density about 500mW/cm^2 with 1 mm^2 reaction area, it was difficult to maintain the power density with larger reaction area and careful observation of the prototypes revealed that the porous Si layer, which should be etched away completely, remained on the channel bottoms. Non-uniform porous Pt catalyst layer thickness was suspicious for the residual porous Si, and rotation of the plating vessel in the Pt deposition process was performed to mitigate variation of the catalyst layer thickness. Though the power density was still low with larger reaction area, the larger output was successfully obtained with the vessel rotation.

1. Introduction

A lot of attention has been paid to miniature fuel cells for portable power sources and some products had been sold. But they did not achieve commercial success yet, and further miniaturization and cost reduction are needed. MEMS fabrication technology is an important tool to reduce the fuel cell structure to micrometer scales and is advantageous for mass production. Therefore, various studies using Si substrate and MEMS techniques have been performed [1-3]. Among those studies, Prinz et al demonstrated high output by their solid oxide fuel cell, and several research groups are now studying the concept, though there are difficulties in high temperature treatment and catalyst durability. Novel electrolyte concepts have also been explored and chemically modified porous Si shows promising results [4-5].

We also have proposed a miniature polymer electrolyte fuel cell (PEFC) design using monolithically fabricated Si electrodes. We found that porous Pt layer can be obtained on a Si substrate by immersing high-porosity porous Si into a Pt plating bath containing HF, and the porous Pt layer is used as a catalyst layer for the PEFC. Applying plasma etching on the backside of the porous Pt layer, fuel channels are opened on the Si substrate and monolithic Si electrodes are made. Porous metal layer is resistive to the plasma and the plasma etching is automatically stopped when the etching reaches to the porous metal layer.
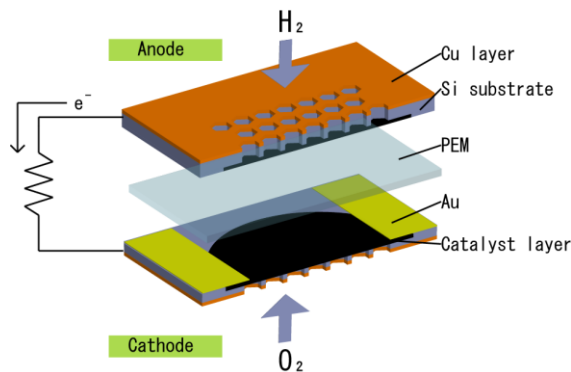
Figure 1. Schematic of the miniature fuel cell with monolithically fabricated Si electrodes.

Figure 2. Fabrication process of the Si electrode.

Table 1 Condition for the catalyst layer formation.

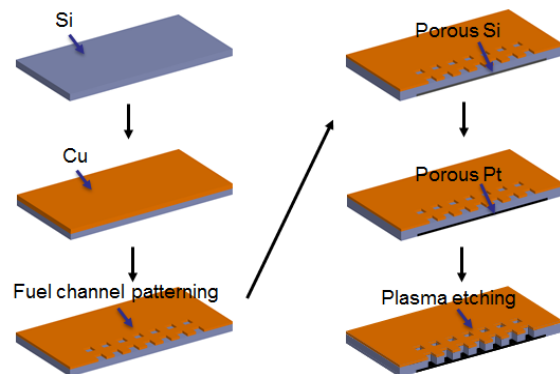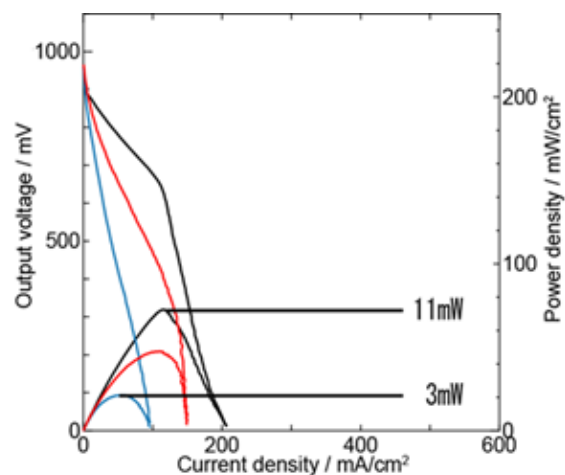| Property of Si substrate	
Crystal Orientation	(100)
Type	N
Thickness of Si substrate	100μm
Resistivity [Ωcm]	0.001-0.003
Anodization condition	
Composition of solution	Water:HF(46%):Ethanol=5:3:2
Pt immesion plating condition	
Composition of solution	20mM H_2PtCl_6 + 1M H_2SO_4 + 450mM HF
Plating time [min]	15
Temperature [K]	283

Figure 3. Polarization curves of cells with 4×4 mm^2 reaction area.

Recently, we found that the porous Si sometimes left on the porous Pt layer after the plasma etching, and the residual porous Si lowered the fuel cell performance by blocking reactant gas supply. Then, the residual porous Si was reduced by optimizing formation process of porous Si. The best performance was demonstrated by cells with the least residual porous Si [6] and the peak power density reached 500mW/cm^2 with 1×1 mm^2 reactive area. However, we still have difficulty in making the Si electrodes with no residual porous Si especially with larger reaction area.
 In this study, we carefully observed the prototype cells, and attempted to reduce the residual porous Si to obtain higher output with larger reaction area.

2. Miniature fuel cell with Si electrodes
Figure 1 illustrates our fuel cell structure. The Si electrode chip has quite simple structure, in which a catalyst layer and fuel channels are monolithically fabricated on a Si wafer. A polymer electrolyte membrane (PEM) sheet is combined with the two Si electrodes using a Nafion® solution as an adhesive, and the thickness of the cell is about 230μm.
Figure 2 illustrates the fabrication process of the Si electrode. A highly As-doped Si wafer (resistivity 0.001-0.003 Ω cm) was used as a Si substrate. Due to its low resistivity, the Si substrate is expected to work as current paths. The wafer was cut into 15×15 mm chips by a dicing saw. After removing surface oxide films by a HF solution, copper thin film was deposited on the Si wafer by sputtering.
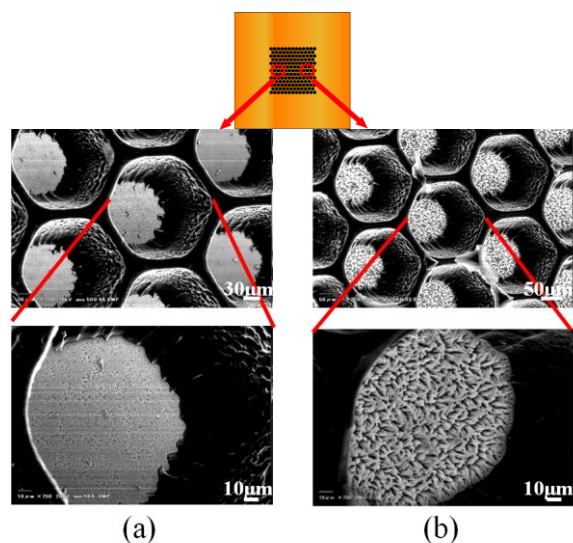
Figure 4. SEM images around channel bottoms on a Si electrode with 4×4 mm^2 reaction area. Almost no residual porous Si was observed in (a), while obvious residual porous Si was observed on some channels, as shown in (b).
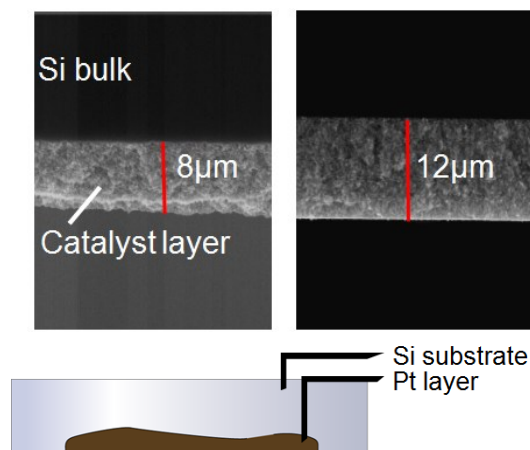
Figure 5. Cross sectional observation and schematic of the non-uniform thick porous Pt layer.

Copper thin film was patterned by conventional photolithography and wet etching, and a mask for the plasma etching was made. Porous Si layer was formed on the opposite side of the Si chip by anodization in an electrolyte containing HF. The porous Si layer was subsequently immersed in a Pt plating bath, and porous Pt layer was obtained. Detailed formation process is described in ref. [7]. Fuel channels were opened by applying plasma etching on the backside of the porous Pt layer with the copper thin film mask. Conventional parallel plate reactive ion etching system (Samco RIE-10N, Japan) was used and 18 sccm of SF$_6$ and 4 sccm of O$_2$ gases were supplied for the etching. In this plasma etching process, porous Pt layer was supposed to work as a stopping layer to the plasma etching, because the etching rate is low at the porous metal layer, and through-chip porous Pt layer can be relatively easily fabricated. In this way, monolithic Si based electrodes were prepared.

3. Non-uniform Catalyst Layer Thickness

Several prototype fuel cells were built with optimized porous Si formation conditions based on ref.[6]. Table 1 shows the conditions for the catalyst layer formation. To obtain larger output, reaction area was enlarged to 4×4 mm^2 from 1×4 mm^2, and power generation tests were performed. The result is shown in figure 3. Only 11 mW (70 mW/cm^2) was observed and the power density was far lower than the expected value (500 mW/cm^2). The performance also varied from cell to cell. In order to find out the possible factors for the deterioration, the Si electrode chips were observed carefully.

Figure 4 shows example SEM images around channel bottoms on a Si electrode with 4×4 mm^2 reaction area. As shown in the figure, on some channels there were no residual porous Si as we expected, while obvious residual porous Si was also observed on some channels. The residual porous Si may cause the performance deterioration.

With the optimized porous Si formation process, almost uniform thick porous Si layer is expected to be formed. However, non-uniform partial residual porous Si was observed. Cross-section of the Si electrode chips was observed widely, and significant non-uniformity in the porous Pt layer thickness was found in some chips. Even within a Si chip, thickness of the porous Pt layer varied from 8 − 12μm as shown in figure 5. Such variation in thickness and pore morphology of porous Si layer are hardly expected, and the wet Pt plating process was suspicious. Figure 6 shows a schematic of the non-uniform catalyst layer.
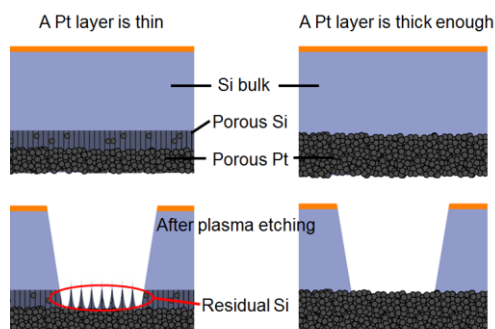
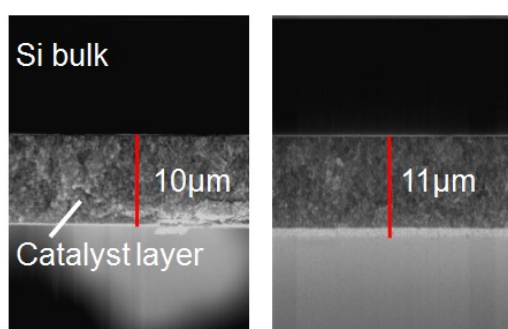Figure6. Schematic of the non-uniform thick catalyst layer.

Figure 8. Cross-sectional SEM imaged of the porous Pt layer levelled by vessel rotation.
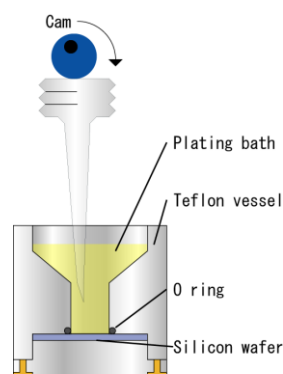

Figure 7. Plating vessel for the porous Pt formation.

In the wet plating process, Si is oxidized while Pt ion is reduced and deposited on the porous Si. Oxidized Si is removed by HF. Basically, this replacement reaction progresses from the top surface to the deeper region. However, small amount of Pt deposition in deep area was observed frequently even in an initial period of the wet plating process, and the porous Si could not be etched away due to the slight Pt deposition and the residual Si might be formed. Anyway, the thickness of the porous Pt rich region (bright region in SEM images) must be levelled.

4. Leveling Catalyst Layer Thickness

4.1 Vessel Rotation during the Pt Plating
Empirically, we found that strong agitation is necessary to obtain porous Pt layer in the wet plating process. Without agitation, deposition sometimes masks the top of the porous layer and significant uneven Pt deposition was observed. Therefore, syringe pumping has been used for agitation in the wet plating process as shown in figure 7. But uniform agitation cannot be expected with the syringe system. Agitation may be sensitive to the syringe tip location in the vessel.

To mitigate the agitation non-uniformity, we decided to rotate the plating vessel during the plating process. The vessel was rotated 3 times during the plating. With each time, 90 degree rotation was applied manually.

Figure 8 shows the cross section of the porous Pt layer formed with the vessel rotation in the plating process. Maximum and minimum thicknesses of the porous Pt layer in a whole cross section were 11 and 10µm, respectively. Though there is still variation, thickness of the porous Pt layer was successfully levelled. Using the vessel rotation technique, the Si electrode chips were fabricated. Figure 9 shows the typical channel bottoms. Magnified view of channel bottoms around each corner of $4 \times 4 mm^2$ reaction area showed almost no-residual porous Si, and the residual porous Si was successfully reduced by levelling the porous Pt layer thickness.

4.2 Power generation tests
Several Si electrode chips were made, and prototype fuel cells with 4×4 mm^2 reaction area were constructed. To test the performance of the cells, 10 sccm of hydrogen gas and 5 sccm of oxygen gas were fed into the cells in a in a temperature controllable chamber at 318K. In order to obtain good ion
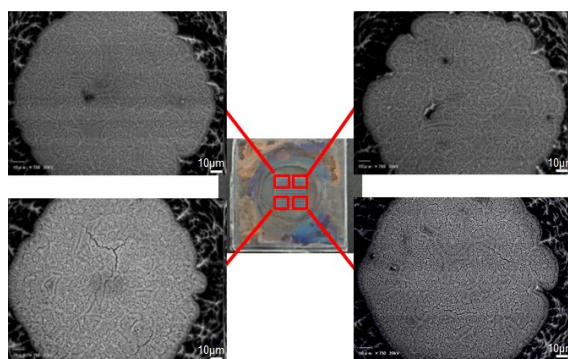
Figure 9. Channel bottoms on a Si electrode fabricated with the vessel rotation.
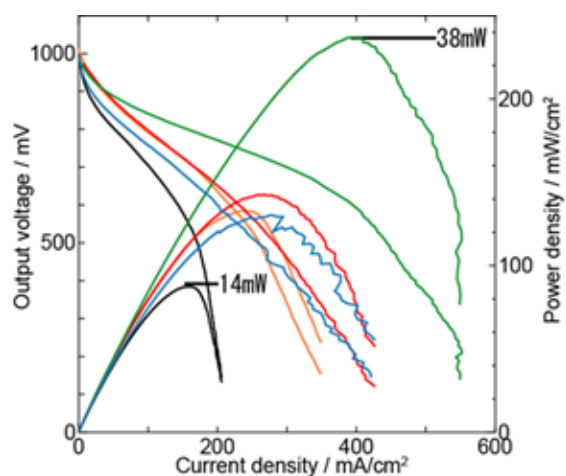

Figure 10. (a) Power generation tests with vessel rotation

conductivity of PEM, hydrogen gas was humidified by bubbling through a water containing tank which was heated to the testing temperature.

Figure 10 shows the result of power generation test. Without the vessel rotation, the output power varied from 3-11 mW as shown in figure 3, while larger output of 14-38 mW were obtained with the vessel rotation. It is found that non-uniform catalyst layer thickness was the major cause of the residual porous Si layer, and the residual porous Si lowered the fuel cell performance. However, the output still varied from 14-38mW, and the maximum power density was 240 mW/cm^2 and was still lower than expected. Therefore, different factors for the performance deterioration must exist. During our study, prototype cells with small reaction area sometimes showed very poor performance. Those cells were not well considered, and they were just thought as broken cells. Contact between catalyst and PEM might be poor in those cells. If the poor contact happened frequently, with larger reaction area, incursion of the poor contact area may be inevitable, and we think that the poor contact is most suspicious factor for the performance deterioration.

5. Conclusions

Residual porous Si, which blocks the fuel supply and deteriorates the cell performance, was found when the reaction area was enlarged to obtain higher output by our miniature fuel cells. The residual porous Si was caused by non-uniform thick porous Pt layer, and the porous Pt thickness was levelled by vessel rotation during the wet Pt plating process. By this improvement, residual porous Si was reduced. Prototype fuel cells were constructed with the least residual porous Si chips, and higher power generation performances were successfully obtained. However, the power density was still lower than that expected from small reaction area test results, and the peak outputs also varied from cell to cell. We think that poor contact between the catalyst and PEM is most suspicious, and further study especially about the contact will be performed.

References

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