

# Carbon nanotubes film preparation on 3D structured silicon substrates by spray coating technique for application in solar cells

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**Abstract.** This paper firstly reports the preparation of carbon nanotubes (CNTs) film on silicon substrate of three-dimensional (3D) inverted pyramid structure (IPS) by spray coating. The effect of different substrate temperatures, spraying times and opening sizes on CNTs sidewall covering properties were investigated. The results show that the CNTs covering ratio of sidewall is much lower than that of flat surface and gradually decrease with depth.  $40\mu\text{m}\times 40\mu\text{m}$  opening obtained the best sidewall covering by CNTs suspension of  $40\mu\text{g/ml}$  at  $120^\circ\text{C}$  after 30min spraying so that the CNTs can reach the bottom of IPS and cover about 68.9% sidewall area. At last, it is demonstrated that the output power of the CNTs film-Si solar cell can be enhanced 5.7 times by this method compared to that of the plane structure.

## 1. Introduction

Carbon nanotubes (CNTs) film is a two-dimensional network structure, formed by many CNTs arranged orderly or disorderly. Because of the low defect, high conductivity and unique physical and chemical properties, it has broad application in film transistors, sensors, batteries, and so on [1].

There are many CNTs film growth methods which can be divided into two categories of direct growth and solution deposition methods. The former one mainly includes graphite arc, chemical vapor deposition (CVD) and laser evaporation. As for the latter, the grown CNTs are dispersed into solution, then the suspension is transferred to the substrate, and finally the agent is removed to form CNTs film. Compared to the direct growth method, the solution deposition method absorbs more interest in industry and academia because of low temperature ( $<150^\circ\text{C}$ ), non-vacuum environment and low cost. Among the solution deposition methods, Langmuir-Blodgett (LB) and chemical self-assembly are used to control the orientation or positioning of CNTs [2, 3]. While, the drop coating and spray coating has the advantages of the simple operation, time-saving and the needlessness of modifying CNTs so that they are widely used in the preparation of random CNTs film [4, 5].

Usually, the output characteristics have positive correlation to the active area. Therefore, forming three-dimensional (3D) inverted pyramid structure (IPS) on silicon substrates is a conventional approach to enlarge surface area of micro-devices for improving their performances, especially in solar cells. Although various CNTs films deposition techniques have been studied in detail, there is little report on the preparation of CNTs film on 3D structured substrates. In this paper, we firstly reports the preparation



of CNTs film on 3D inverted pyramid structured silicon substrate by spray coating, and the application in the CNTs film-Si solar cell was proved at last.

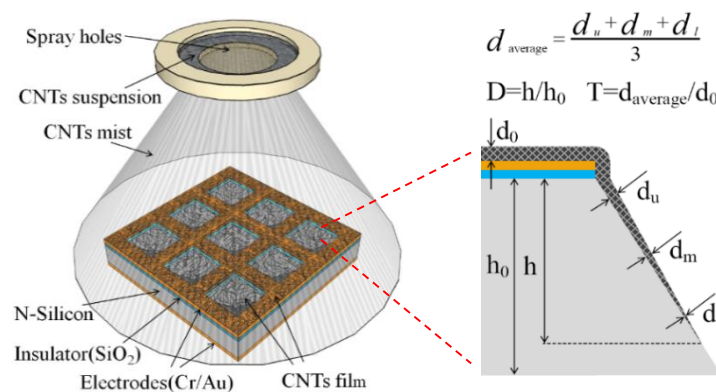
## 2. Design

For solar cells, the output characteristics get better along with the increase of the surface area. However, because electron and hole is bound to recombine in the transport process, the shorter of the distance before the collection of metal electrode, the lower is the probability of recombination. So the metal electrode is usually designed to be square arrays structure and the width is designed to be  $20\mu\text{m}$  with the consideration of the technique limitation. In addition,  $10\mu\text{m}\times 10\mu\text{m}$ ,  $40\mu\text{m}\times 40\mu\text{m}$  and  $80\mu\text{m}\times 80\mu\text{m}$  three different opening size arrays are designed to study effects of different 3D structures on the sidewall coverage and optimize the spray coating technique parameters at last.

We choose the n-type Si (100) wafer ( $2-4\Omega\text{cm}$ ) as substrate. CNTs film is generally regarded as metallic, which forms a Schottky junction with the silicon substrate. Both front and back electrodes are made of Cr/Au and play roles of collecting and transporting carriers. The role of the  $\text{SiO}_2$  layer was to isolate the front electrode and the Si surface to avoid short-circuit. Finally, the microcell was set up on a piece of Printed Circuit Board (PCB), and the front electrode of each microcell was conducted to the external circuit. When the CNTs film-Si heterojunction is illuminated, electron hole pairs are excited. Those generated in the depletion region can be swept across the junction by the built-in electric field into external circuit generating current. Holes are collected by the p-type SWNTs thin film, and electrons are collected by the n-type Si substrate.

## 3. Fabrication

The fabrication process started on n-type Si (100) wafer.  $300\text{nm}$   $\text{SiO}_2$  were thermally grown on both sides of Si wafer, and the back side one was wiped off by buffered hydrofluoric acid (BHF). Then phosphorus ions were implanted to the back surface followed by annealing at  $1000^\circ\text{C}$ .  $30\text{nm}/150\text{nm}$  Cr/Au were deposited on the front surface. The Cr/Au and  $\text{SiO}_2$  of the front surface were patterned respectively into  $10\mu\text{m}\times 10\mu\text{m}$ ,  $40\mu\text{m}\times 40\mu\text{m}$  and  $80\mu\text{m}\times 80\mu\text{m}$  square opening arrays. After that the Si was wet-etched by KOH until self-stop, achieving 3D IPS.  $30\text{nm}/150\text{nm}$  Cr/Au were deposited on the back side of Si wafer and was annealed at  $320^\circ\text{C}$  to form ohmic contact with Si. Finally, the wafer was diced into  $5\text{mm}\times 6\text{mm}$  pieces on which we would deposit CNTs thin film. In order to contrast with the 3D IPS, we also designed plane structures. The fabrication process of plane structures is similar to the process introduced above except for the KOH wet-etched step.



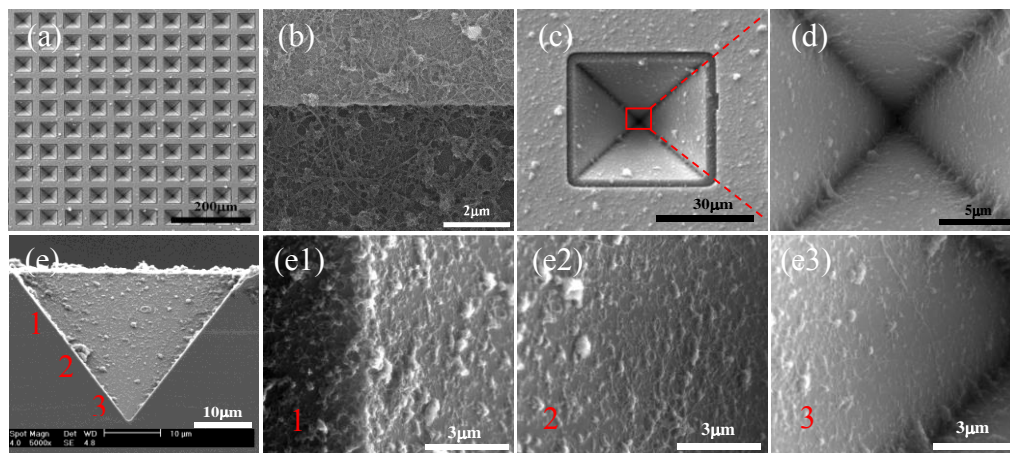
**Figure 1.** A 3D schematic view of the spray coating method (inset: measurement parameters of CNTs film).

Spray coating technique is a method to atomize the CNTs suspension which is sprayed to the hot substrate to get CNTs film (Fig. 1). At first, CNTs powders (purity>90%) were ultrasonically dispersed in dimethylformamide (DMF). Then CNTs suspension was converted into mist and sprayed onto baked

Si substrate by ultrasonic sprayer. At the same time, the Si substrate was heated to evaporate DMF rapidly and totally. Different spraying conditions were investigated experimentally, including the substrate temperature of 70°C, 100°C, 120°C 150°C and 200°C, spraying time of 15, 30 and 45min and CNTs suspensions concentration of 20 and 40 $\mu$ g/ml.

#### 4. Test and results

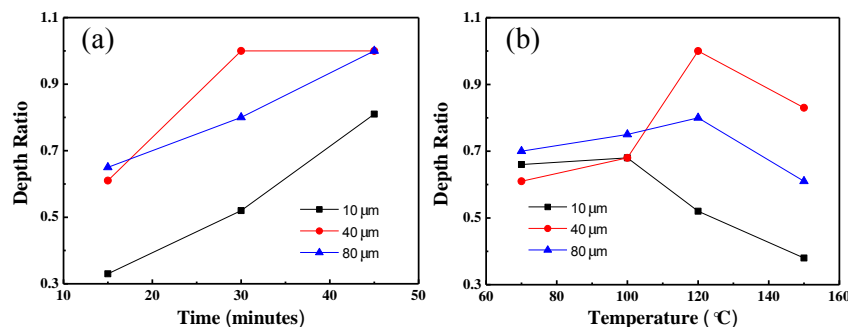
The sidewall covering degrees are characterized by the depth ratio of IPS that CNTs film reached and the CNTs film thickness ratio along the sidewalls. For plane structures, the thickness of CNTs film can be measured directly. However, for 3D IPS, the thickness of CNTs film is measured by average method because the sidewall covering properties change with the depth of the groove. We define the thickness of CNTs film on plane structures as  $d_0$ , the CNTs film covering ratio of plane structures as  $C_0$ . As for the IPS, we define the depth of IPS as  $h_0$ , the depth CNTs reached as  $h$ , and the thickness of CNTs film in different depth on 3D structures sidewall as  $d_u$ ,  $d_m$ ,  $d_l$  (Fig. 1 insert). The average thickness on 3D structures sidewall is  $d_{\text{average}} = (d_u + d_m + d_l)/3$ . The depth ratio is  $D = h/h_0$  and the thickness ratio is  $T = d_{\text{average}}/d_0$ . So the covering ratio can be expressed approximatively as  $C_0 \times d_{\text{average}}/d_0$ .



**Figure 2.** SEM images of CNTs film prepared by spraying 30min at 120°C on 3-D structured Si substrates with 40 $\mu$ m $\times$ 40 $\mu$ m opening: (a) IPS array covering; (b) planar covering on Au and Si surface forming a network structure; (c) single IPS covering; (d) enlarged view of bottom area covering of IPS; (e) cross-section of IPS covering; (e1)-(e3)enlarge views of the IPS sidewall covering at points 1,2,3 of (e).

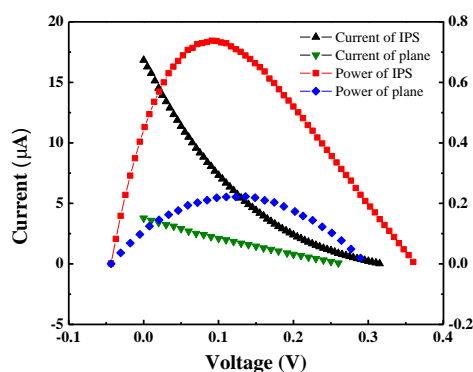
Fig. 2 is the SEM of the CNTs film prepared by spraying 30min at 120°C with 40 $\mu$ m $\times$ 40 $\mu$ m opening. Spray coating technique can form uniform CNTs film in whole array (Fig. 2(a)) and the surface of Au and Si (Fig. 2(b)). This spraying condition obtained the best sidewall covering of  $D=1$  and  $T=0.725$ , indicating that the CNTs can reach the bottom of IPS and cover about 68.9% (estimated  $C_0=95\%$ ) sidewall area (Fig. 2(c) and (d)). Fig. 2(e) gives the SEM of the whole sidewall covering. We enlarged 1, 2 and 3 position (Fig. 2(e1~e3)) and can find the CNTs covering ratio of sidewall is much lower than that of flat surface and gradually decreases with depth.

Fig. 3 is the curve of depth ratio versus spraying time and temperature of three different opening sizes. The CNTs film covering ratio increases along with the spraying time (Fig. 3(a)). What's worth noting is that the depth ratio of 40 $\mu$ m $\times$ 40 $\mu$ m opening size is better than 10 $\mu$ m $\times$ 10 $\mu$ m and 80 $\mu$ m $\times$ 80 $\mu$ m opening sizes at 120°C after 30min spraying. With the increase of temperature, the CNTs film covering ratio shows a downward trend after the first increases (Fig. 3(b)). The 40 $\mu$ m $\times$ 40 $\mu$ m and 80 $\mu$ m $\times$ 80 $\mu$ m opening sizes get the best depth ratio at 120°C, while the 10 $\mu$ m $\times$ 10 $\mu$ m opening size decreases above 100°C. And, it was found that concentration of the CNTs suspension has almost no influence on 3D covering properties.



**Figure 3.** (a) The depth ratio versus time when temperature is 120°C and CNTs suspension is 40μg/ml; (b) The depth ratio versus temperature when spraying time is 30 minutes and CNTs suspension is 40μg/ml.

Fig. 4 is the Current-Voltage (I-V) curves and Power-Voltage (P-V) curves under light (AM 1.5G, 100mW/cm<sup>2</sup> illumination) for IPS and plane structures. It can be seen that the short circuit current and the open circuit voltage of IPS structure are respectively  $I_{SC}^{IPS}=17.5\mu A$  and  $V_{OC}^{IPS}=0.32V$ , while  $I_{SC}^{plane}=3.7\mu A$  and  $V_{OC}^{plane}=0.26V$  for plane structure. So the output power of the CNTs film-Si solar cell can be enhanced 5.7 times by IPS structure.



**Figure 4.** The Current-Voltage (I-V) curves and Power-Voltage (P-V) curves under light (AM 1.5G, 100mW/cm<sup>2</sup> illumination) for IPS and plane devices, with  $I_{SC}^{IPS}=17.5\mu A$ ,  $V_{OC}^{IPS}=0.32V$  and  $I_{SC}^{plane}=3.7\mu A$ ,  $V_{OC}^{plane}=0.26V$  respectively.

## 5. Conclusion

This paper firstly reports the preparation of carbon nanotubes (CNTs) film on 3D inverted pyramid structured silicon substrate by spray coating. The effect of different substrate temperatures, spraying times and opening sizes on CNTs sidewall covering properties were investigated. The results show that the CNTs covering ratio of sidewall is much lower than that of plane surface and gradually decrease with depth. With the increase of spraying time, the CNTs film covering ratio increases. While covering ratio shows a downward trend after the first increases with the increase of temperature. 40μm×40μm opening obtained the best sidewall covering by CNTs suspension of 40μg/ml at 120°C after 30min spraying so that the CNTs can reach the bottom of IPS and cover about 68.9% sidewall area. Finally, it is proved that the output power of the CNTs film-Si solar cell can be enhanced 5.7 times by this method.

## References

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