Design of an Integrated Thermoelectric Generator Power Converter for Ultra-Low Power and Low Voltage Body Energy Harvesters aimed at EEG/ECG Active Electrodes

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Abstract. This paper describes a design procedure for an efficient body thermal energy harvesting integrated power converter. This procedure is based on loss examination for a self-powered medical device. All optimum system parameters are calculated respecting the transducer constraints and the application form factor. It is found that it is possible to optimize converter's working frequency with proper design of its pulse generator circuit. At selected frequency, it has been demonstrated that wide area voltage doubler can be eliminated at the expense of wider switches. With this method, more than 60% efficiency is achieved in simulation for just 20mV transducer output voltage and 30% of entire chip area is saved.

1. Introduction

In a wide range of diseases, clinicians are looking for solutions to provide an early diagnosis. Alzheimer and Epilepsy are neurological disorders that are frequently screened by physicians. Early diagnosis requires monitoring the subject's physiology and symptom development through Electroencephalography (EEG) and Electrocardiogram (ECG) signals over long periods. These examinations, done with complex devices, are currently very expensive. Furthermore they disturb normal life of patients because they have to be performed in hospital environment. Although wearable sensors can significantly benefit mankind in this long-term monitoring process, today's solutions invade the user's normal life as their platforms require removal, replacement and reconfiguration due to battery recharging. Moreover, size and weight of integrated electronic systems are usually set by batteries.

The "Zero Power" Medical devices approach can revolutionize human parameters monitoring thanks to new architectures which will lead to drastically lowering the power needs. Energy can then directly be harvested from natural sources. This makes possible to implement systems that minimize their impact on the everyday life of patients. In zero power medical applications, body energy harvesters produce unreliably small amounts of power and moreover at low voltages. On the other hand, local processing operation in body sensor nodes is power hungry. Thereby, designing an optimum architecture with ultra-low power custom integrated circuit is an inevitable choice.

Body heat can be a source for energy harvesting when autonomous medical devices have been placed directly on a human skin. In that case, miniature Thermoelectric Generators (TEG) are used as transducers. The output impedance of TEG cell is relatively constant. However, output voltage changes according to the environmental conditions and have been shown to be very small [1]. Power converter is then responsible for tapping such infinite but unreliable low potential energy from the harvesters and

provide it as a high potential and reliable power source for applications. The conversion of small output voltages, in the range of a few tens of millivolts, have been achieved but with poor efficiency [2-4].

In this paper, a design procedure for an optimum integrated power converter aimed at an autonomous EEG active electrode will be presented. The procedure is based on losses examination in circuit blocks and the system. In the literature, the losses analysis of converters has been used for study of power converter characterization [2], [5]. Recently [6], this analysis has been used for optimizing specific circuit parameters such as switch sizes or frequency independently, for a fixed architecture and a transducer. However, in a body powered system different power converters are used with diverse specifications. This means that the design procedure to reach an optimum should be algorithmic, with the aim of reduce design time. Here, the design process for a simpler and more efficient converter system is discussed. Section 2 describes an autonomous active electrode as our medical platform. Section 3 introduces the design method for the converter followed by section 4 presenting the simulation results.

2. Body powered active electrode with TEG integrated

Long term EEG signal monitoring devices must be convenient while maintaining the precision compared to conventional devices. Accordingly, readout electrodes and electronic components must be tiny and lightweight and must provide high Signal to Noise Ratio (SNR) and low distortions. However, EEG signals are weak and are accompanied by strong interferences. To achieve signals with high SNR and low distortions, it is mandatory to amplify signal and reject interferences immediately after acquiring the signal. This becomes possible if active components are placed right next to the electrodes.

An autonomous active EEG electrode based on TEG harvester was introduced in [1]. It consists of a metallic plate as EEG electrode and thermal contact, TEG transducer, heat transfer structures, and electronics responsible for EEG signal conditioning and TEG power conversion. The size of entire system should be same as one electrode (i.e. 12mm×12mm in our case). This implies a hard limit form factor for the power converter. Besides area constraints, power converter must have enough efficiency to provide adequate power for the integrated EEG amplifier which consumes less than 7µW from a 1.2V supply. Table I summarizes the experimental specifications of these TEGs when transducers harvest body thermal energy [1]. This table suggested about 20% efficiency with conversion factor of 60 for low voltage TEG and 70% efficiency with a conversion factor of 15 for higher voltage transducer.

3. Power converter design

Figure 1 a) shows a modern general power converter architecture [3-4], [6] considered here. Circuit blocks including comparator are activated only when they are triggered by clock signals. Therefore, it offers the best of compromise between continuous analog control loop and power hungry precise digital one, resulting in minimizing the power consumption. In this architecture, first, the harvester charges input capacitor C_s in *tc* duration while both NMOS and PMOS switches are off. Then, NMOS transistor is turned on, PMOS is kept off, and harvested energy stored in C_s is transferred in inductor L_s, during period *t1*. After *t1*, NMOS is turned off and PMOS is switched on, so, energy will be transferred from L_s to the final *Load* during a period *t2*. This function will repeat with frequency f_s. Durations *t1* and *t2* are set by two pulse generators dedicated. To maximize energy efficiency, power transferred to the output should be maximized and converter losses be minimized. Presuming low loss on board components and big inductance L_s, the energy transferred from input to the *Load* could be written as:

$$E_T = \frac{L_s.I_P^{\,2}}{2} + \frac{V_{in}.I_P.t2}{2} \quad (1)$$

Table I: TEGs body harvester electrical characteristics at 24°C ambient temparture [1]

	Material, Size, Condition	Available Power	Output Voltage	Voltage type	Output Impedance	Impedance type
Thermal 1	**Macro TEGs 15x15x4 mm**	**40µW**	**20mV**	**DC**	**2.5Ω**	**Constant**
Thermal 2	**Micro TEGs, 15x15x4 mm**	**10µW**	**80mV**	**DC**	**160Ω**	**Constant**

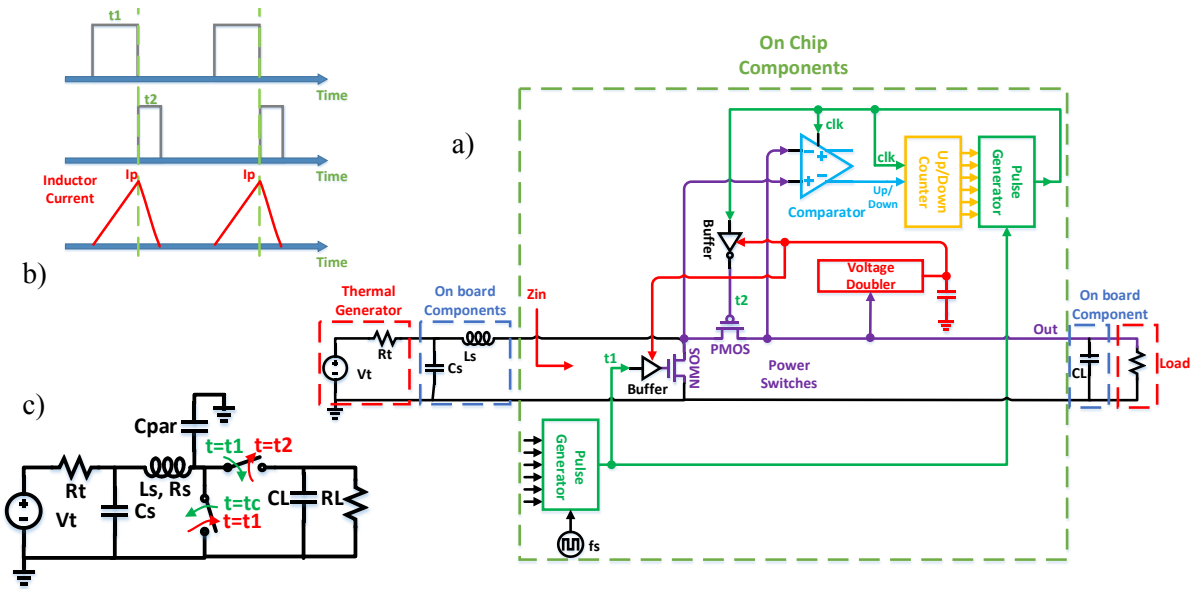

Figure 1: a) General architecture of a converter [3-4], [6], b) timing diagram, and c) its basic schematic

where the first term and second term are related to energy transmitted during *t1* and *t2*, respectively and I_p is peak current of the inductor. Simplifying equation (1), transferred power can be expressed as:

$$P_T = f_s.E_T = V_{in}{}^2.\left[f_s\left(\frac{t1^2}{2L_s} + \frac{t1.t2}{2L_s} \right) \right] \tag{2}$$

In (2), the statement brought in a bracket can be interpreted as the system input admittance. For maximizing power transfer, the input impedance, Z_{in}, should be matched to the harvester impedance, R_t. If it is assumed that *t1* is much longer than *t2* (it will be shown later), Z_{in} can be written as:

$$Z_{in} = \frac{2.L_s}{t1^2.f_s} \tag{3}$$

Therefore, Z_{in} is related to *t1* and it is tuned by the duty cycle of the clock frequency f_s.

Switching losses can be divided in static losses related to "On"-resistance of switches, dynamic losses including switches' gate and buffers' gate charging and discharging losses, and leakages loss. There is a trade-off in the switches sizing. Indeed, the static power losses decrease with wider switches but the dynamic power consumption increases. Based on the equations for these losses and for on board component parasitics, an optimum switches' sizes in each operating frequency can be found (Figure 2). This optimization was calculated using transducer characteristics for the worst case i.e. low voltage TEG scenario. In our micro-watts power regime, our examination showed that leakages loss does not have major effect on efficiency since it is in order of nano-watts. Inductor parasitics can also be neglected here. A simplified system loss around the optimum points presented in Figure 2 can then be stated as:

$$P_{Loss} = I_{Ls,RMS,t1}{}^2.\left(\mathrm{R}_{NMOS} + \mathrm{R}_{PMOS}\frac{t2}{t1} \right) + f_s.V_{SW}{}^2.\eta.\left(1+\frac{1}{\alpha} \right).\left(C_N + C_P \right) \tag{4}$$

where R_{NMOS}, C_N, R_{PMOS}, C_P are channel's resistances and gate's capacitance of NMOS and PMOS switches, respectively. The ratio of switch sizes to the size of the buffers which drive the switches was introduced by α. V_{SW} is switching gate source voltage and η is the efficiency of the circuit that provides this switching voltage. Root-mean-squared current through L_s during *t1*, $I_{Ls,\,RMS,\,t1}$ can be written as:

$$I_{Ls,RMS,t1} \approx \frac{V_{in}}{\left(L_s.f_s \right)^{1/4} Z_{in}{}^{3/4}} \tag{5}$$

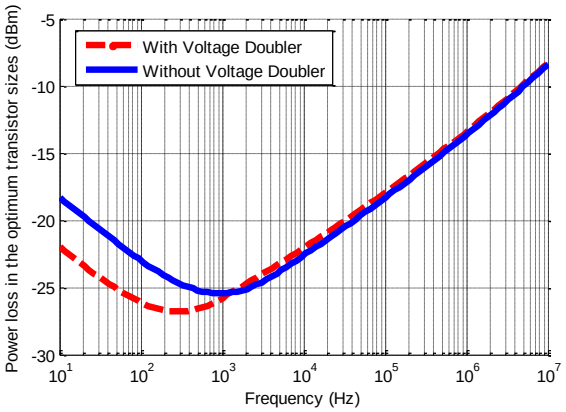

Figure 2: Optimum power loss for optimized switches' sizes versus frequency

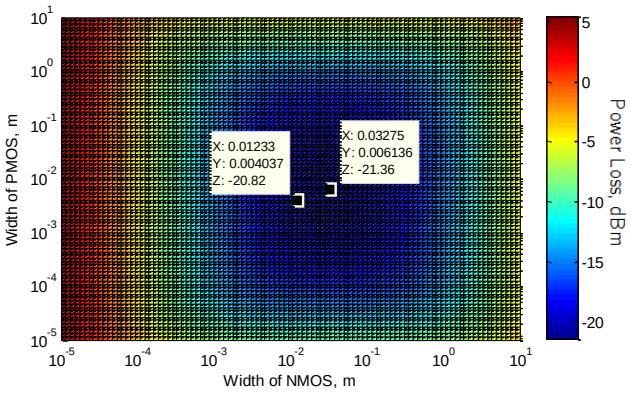

Figure 3: Power loss versus switches' sizes at f_S

From (4) and (5), it is clear that for having maximum efficiency the biggest possible inductance should be selected, however; system form factor confines inductance value. Here, the largest possible inductance with the package size of 8mm×8mm, a 47µH was selected. Simplified close form Equation (5) was written assuming that V_{in} is almost constant during inductor charging. However, V_{in} might vary during charge transfer. The exact current-voltage relations for the schematic shown in Figure 1 c) were derived and it verifies the inductance-current behavior of equation (5).

For low power applications, Discontinuous Conduction Mode (DCM) converters have a higher efficiency. In DCM, PMOS should be turned off exactly when current of the inductor reaches zero. A pulse generator and a comparator have been used to synchronize the switching off of PMOS. Comparator in Figure 1 a) detects whether PMOS is turned off early or late at the end of *t2*. Based on that pulse width of *t2* is tuned by the counter and the pulse generator dedicated to *t2*. With detail analysis of Figure 1 c) and simplifying equations during discharge of L_s in the output capacitor, *t2* can be estimated as:

$$t2 = \frac{t1.V_{in}(\mathrm{t}=\mathrm{t1})}{V_{out} - V_{in}(\mathrm{t}=\mathrm{t1})} \tag{6}$$

Output voltage, V_{out} must have less than 10% ripple and its fluctuations are set by C_L capacitance. $V_{in}(t=t1)$ is the input voltage at the end of charging L_s. The input voltage variation during *tc* and *t1* is inversely related to f_s, L_s, and C_s. If the system has a large V_{in} ripple, $V_{in}(t=t1)$ may reach to a small value and generating of *t2* becomes impossible. Considering that our form factor which limits the board area to the size of one EEG electrode, a C_s with also a size of 1.6 mm × 0.8mm was selected. The largest commonly available capacitance within this size is 10µF. As shown by Figure 2, maximum efficiency occurs when f_s is around 500Hz. With this frequency and the chosen C_s, our relations show that input voltage ripples become large and V_{in} reaches zero even before *t1* duration. Thus, it is not possible to create *t2* pulses. Common approach in literatures suggested increasing f_s up to have a less than 10% variation of input voltage. As Figure 2 illustrated, along the increase of frequency, losses will increase linearly. Here, frequency is increased up to the point that entire loss deviates less than 10% of input available power from the optimum point. With f_s equal to 20kHz, input voltage reaches to 5mV at end of *t1*. Therefore, by designing an apt pulse generator which provides pulses with duration of 180nsec, system can be functional with higher efficiency than a system designed with conventional approaches.

"On"-resistance and leakages loss of switches and are inversely related to switches' gate voltage. A voltage doubler is usually used to provide higher gate voltage. The output of voltage doubler is stored into on-chip capacitors. The on-chip capacitance of the voltage doubler should be large since it should supply enough energy for switching the power transistors. The voltage doubler may occupy more than 50% of area of a power converter because of its on-chip capacitors. Based on our analysis (Figure 2) it was demonstrate that if we remove the voltage doubler for f_s higher than 1kHz, power loss remains constant but the switches will be bigger. Power loss versus switches' size for the selected f_s without

Table II: Summarized this design and the prior arts

	[3][1]	[4][1]	[2][1]	This work[2]
Topology	**Inductor based**	**Inductor based**	**Inductor based**	**Inductor based**
Technology	**0.35µm**	**0.35µm**	**0.13µm**	**0.18µm**
Voltage Conversion	**26~100mV to 1.8V**	**100mV to 2V**	**20~100mV to 1V**	**20mV to 1V**
Output Power	**10µW @25mV**	**1.3mW @100mV**	**25µW @20mV**	**25µW @20mV**
Quiescent Power		**-**	**1.3µW**	**1.2µW**
Efficiency at 20mV	**<20%**	**40%**	**46%**	**60%**
Core area	***1.6mm²**	***2.5mm²**	****0.12mm²**	****0.14mm²**

[1] Measurement results [2]Layout post-simulation results *entire chip **core

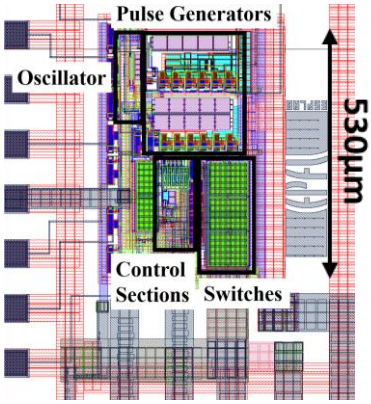

Figure 4: Layout designed in UMC 0.18µm CMOS

voltage doubler, is shown on Figure 3. Exact optimum widths supporting selected f_S for NMOS and PMOS pose large parasitics. By accepting a deviation of 10% from the optimum (Figure 3), a suitable transistor width can be achieved. With this technique, area of the chip due to switches is just 20% bigger, but overall circuit area circuit is reduced by 30%, while complexity and design procedure are drastically reduced. Also, with decreasing number of blocks the quiescent power consumption is reduced.

4. Simulation results

With the introduced algorithmic design procedure and taking into account the form factor, an ultra-low power DC-DC converter for the thermal body harvesters was designed in UMC 0.18µm CMOS technology. According to post-layout simulations, the design of 6 bit *t2* pulse generator can produce pulse durations from 44nsec to 665nsec. Such conservative circuit implementations help the system to work around its optimum point when input voltage varies depending environment or when high voltage TEG harvester characterized in Table I is used as transducer. Here, it is assumed that output energy storage has some charge during start-up that is to say that the cold start has not focused on this paper. The area of the power converter is 0.14mm^2. Its layout is shown in Figure 4. The quiescent power consumption of the system is 1.2µW and more than 60% efficiency has been achieved in post-layout simulations for 20mV TEG output voltage while the reported efficiencies in similar situation in state-of-art are below 50% [2-4]. Table II summarizes chip performances and other the state-of-the-art.

5. Conclusion

Energy transfer and loss formulas were used for a general power converter to find an optimum architecture and all the design parameters. To support calculated optimum frequency f_S, a huge input capacitance was required. With a slight deviation from the optimum f_S and design a proper pulse generator, and reasonable sizes for passive elements were achieved. Besides, the method led to a simpler design and lower power consumption since voltage doubler was eliminated without increasing loss. Presented method reduced unnecessary system complexity and area while enhancing efficiency.

Acknowledgments

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References

[1] M. Thielen, M. Ataei, et al. , *International Conference on Thermoelectrics - ICT2014*, 2014
[2] E. Carlson, et al. , *Solid-State Circuits, IEEE Journal of* , **vol.45**, no.4, pp.741,750, April 2010
[3] Y. Ramadass, et al., *Solid-State Circuits, IEEE Journal* , **vol.46**, no.1, pp.333,341, Jan. 2011
[4] S. Bandyopadhyay, et al. , *Solid-State Circuits, IEEE Journal* , **vol.47**, no.9, pp.2199,2215, 2012
[5] X. Zhou, et al. , *Applied Power Electronics Conference and Exposition*, **vol.2**, pp.612, vol.2, 1997
[6] S. Bandyopadhyay, et al. , *Solid-State Circuits Conference (ISSCC), IEEE,* pp.396,397, 2014