

Deep sub-micron stud-via technology for superconductor VLSI circuits

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Abstract. A fabrication process has been developed for fully planarized Nb-based superconducting inter-layer connections (vias) with minimum size down to 250 nm for superconductor very large scale integrated (VLSI) circuits with 8 and 10 superconducting layers on 200-mm wafers. Instead of single Nb wiring layers, it utilizes Nb/Al/Nb trilayers for each wiring layer to form Nb pillars (studs) providing vertical connections between the wires etched in the bottom layer of the trilayer and the next wiring layer that is also deposited as a Nb/Al/Nb trilayer. This technology makes possible a dramatic increase in the density of superconducting digital circuits by reducing the area of interconnects with respect to presently utilized etched contact holes between superconducting layers and by enabling the use of stacked vias. Results on the fabrication and size dependence of electric properties of Nb studs with dimensions near the resolution limit of 248-nm photolithography are presented. Superconducting critical current density in the fabricated stud-vias is about $0.3 \text{ A}/\mu\text{m}^2$ and approaches the depairing current density of Nb films.

1. Introduction

In order to realize the tremendous advantages of superconducting digital integrated circuits over semiconductor circuits in speed and reduction of energy dissipation [1], their integration scale must be increased from its current medium level to very large scale integration (VLSI) levels and beyond by increasing the density of Josephson junctions (JJs) from the present density of $\sim 10^4 - 10^5$ JJs per cm^2 to $10^6 - 10^7$ JJs/ cm^2 , with a corresponding increase in the density of interconnects. This can be achieved by scaling down the dimensions of all circuit elements and increasing the number of superconducting metal layers available for circuit integration. In all reported fabrication processes [2]-[6], superconducting interconnects between wiring layers (vias) are made by etching contact holes in the inter-metal dielectric and depositing the next Nb layer by physical vapor deposition (PVD). This limits the minimum size of contact holes to $\sim 0.5 \mu\text{m}$, as it becomes difficult to achieve reliable superconducting contacts with sufficient critical currents in smaller holes. In practice, the contact hole also needs to be surrounded by metal overlay to allow for photolithography misalignment and etch bias, making the typical via size around $1 \mu\text{m}$ and yet larger when many vias need to be stacked on top of each other to make low-inductance connections between the bottom and top layers in a 10-metal layer circuit. As a result, vias became one of the largest components in superconducting digital circuits, occupying up to 30% of the circuit area because the number of vias is much larger than the number of Josephson junctions.



In this paper we propose new processes for deep-submicron vias, which uses etched Nb pillars (studs) between wiring layers instead of etched contact holes with metal filling. The studs are formed by Nb etching with subsequent dielectric deposition followed by dielectric chemical mechanical planarization (CMP). We present results of the practical realization of one of the processes, including electrical characterization of the resultant vias. We have found that this process allowed us to form Nb stud-vias with design sizes down to our photolithography resolution limit (~ 250 nm) and with superconducting critical current density approaching the depairing critical current density of Nb.

2. Stud-via process description

Instead of etched contact holes with metal filling we propose to use etched Nb pillars (studs) from a deposited Nb film in contact with bottom wiring layer M_i . An interlayer dielectric could be deposited over them and planarized using CMP to make access to the top of the stud. Then, the top wiring layer would be deposited. A detailed description of the dielectric CMP processes can be found in [7].

There are two possible realizations. The first is shown in figure 1 and referred to as a single etch and planarization (SEAP) process. Here, the bottom Nb wiring layer M_i is deposited and patterned, figure 1(a). This layer is then planarized by depositing a thick layer of SiO_2 [figure 1(b)] with subsequent CMP to get the planar structure shown in figure 1(c). After this, Nb deposition for subsequent studs follows, figure 1(d). Since Nb studs need to be etched while stopping on the bottom Nb wiring, it is useful to have a good etch stop (ES) layer – a material with a lower etch rate than Nb. This ES layer must not degrade the superconducting properties of the interface in order to maintain high critical current in the superconducting state. There are very few materials suitable for this, and a thin layer of aluminium (a few nanometers thick) is one of them. After etching the studs, figure 1(e), the process flow repeats planarization steps (b) and (c) to planarize studs and open access to their top surface, figure 1(g). Finally, the top Nb wiring layer is deposited and patterned to complete the via-stud interconnects between a pair of Nb layers M_i and M_{i+1} . The process can further be repeated for the next pair of wiring layers M_{i+1} and M_{i+2} and so on in a straightforward manner. It also allows for stacking studs on top of each other.

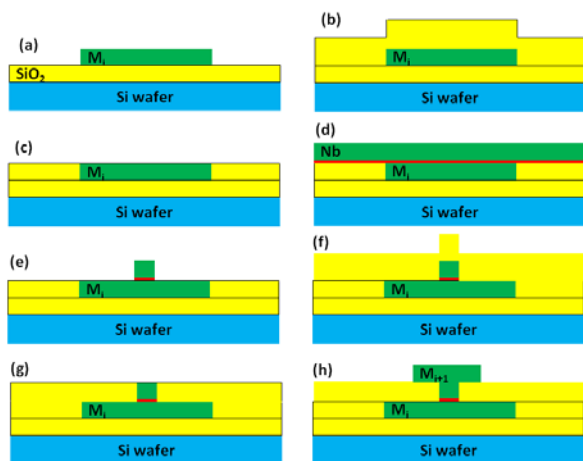


Figure 1. Cross sections of the SEAP version of a stud-via process for superconducting circuits: (a) – deposition and patterning of (Nb) wiring layer M_i over the wafer; (b) – deposition of a blanket SiO_2 layer for CMP planarization; (c) CMP of the SiO_2 layer; (d) deposition of an etch-stop layer (ES) and Nb stud metal bi-layer; (e) patterning of Nb studs and ES layer; (f) blanket SiO_2 deposition for CMP planarization; (g) CMP of SiO_2 to access the top of Nb studs; (h) deposition and patterning of the next Nb wiring layer, M_{i+1} . Prior step (a) the wafer may already contain several patterned and planarized layers. A convenient etch stop layer is Al. The bi-layer deposition should be done in-situ to minimize contamination of the interface between Al and Nb stud.

The described process can be simplified by noticing that the structure formed after stud etching, figure 1(e), resembles the standard trilayer-type SNS Josephson junction where the base electrode is bottom wiring layer M_i , the counter (top) electrode is the stud, and the Al etch stop layer is N-layer or Al- AlO_x barrier layer in tunnel junction trilayers [6] without oxidation. Therefore, the stud-via formation can be done in the same manner as the formation of Josephson tunnel junctions in a whole-wafer trilayer process [6] with the addition of planarization [8]. This second version of the stud-via process, shown in figure 2, is referred to as a dual-etch and planarization (DEAP) process.

Instead of depositing a single wiring layer as in the previous (SEAP) version, in this process each wiring layer is deposited in-situ as a Nb/Al/Nb trilayer, figure 2(a). The top layer of the trilayer is then patterned by photolithography and dry etching to form Nb studs as shown in figure 2(b). Aluminium serves as an excellent etch-stop layer for etching Nb in F-based chemistries. Then, the bottom electrode of the trilayer is patterned in Cl-based chemistry to etch through the Al layer and form the wiring pattern M_i . Etching is followed by blanket SiO_2 deposition and CMP to access the tops of Nb studs, figure 2(e). Then, the next layer M_{i+1} is deposited as a Nb/Al/Nb trilayer and patterned in the same manner to form the next layer of interconnects, and so on. If no more stud-vias are required above, a single metal wiring layer can be deposited. The described processing unit needs to be repeated as many times as there are wiring layers in the full process.

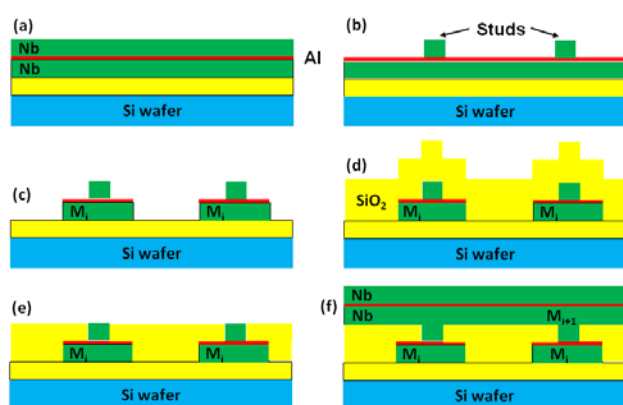


Figure 2. Cross-sections of Nb/Al/Nb trilayer-based (DEAP) stud-via process: (a) Nb/Al/Nb in-situ trilayer deposition; (b) patterning of the top electrode to etch Nb studs; (c) patterning of the bottom electrode to form wiring layer M_i ; (d) blanket SiO_2 deposition for planarization by CMP; (e) CMP down to the tops of Nb studs; (f) Nb/Al/Nb wiring layer deposition to form wiring layer M_{i+1} and Nb stud to contact next layer M_{i+2} . If no additional stud-vias are required above, a single Nb wiring layer M_{i+1} can be deposited instead. This process is to be repeated as many times as there are wiring layers in the entire process.

3. Stud-via fabrication

Nb/Al/Nb trilayers were deposited over 200-mm Si wafers with 500 nm of thermal oxide. The target thickness of the top Nb layer (Nb studs) was 250 nm, and of the bottom layer and the wiring layer was 200 nm. The thickness of the Al etch-stop layer was 8 nm. The photolithography was done using a positive deep-UV photoresist, bottom antireflection coating, Canon FPA-3000 EX4 248-nm stepper with 5x reduction and 250-nm nominal resolution. The circular shape for stud definition was implemented with diameters from 200 nm to 15 μm . The typical SEM images are shown in figure 3.

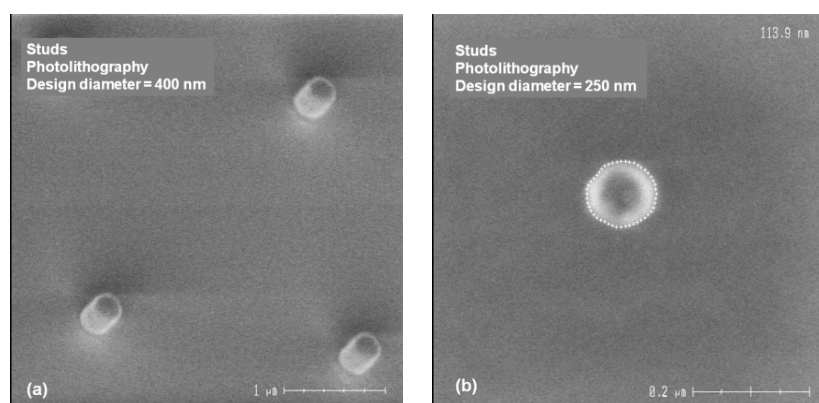


Figure 3. SEM images of the photoresist mask and etched Nb features: (a) tilted view of 400-nm photoresist posts masking Nb/Al/Nb trilayer used for stud-via definition; (b) top view of a photoresist post with design diameter of 250 nm, showing the automated CD measurement of the mean diameter using 48 points around the feature perimeter and giving 113.9 nm (right upper corner).

Nb etching was done using the high density plasma etching chamber of an Applied Materials Centura system with end-point detection. The results are shown in figure 4. Etching of the bottom wire was done in a Cl-based chemistry to break through the Al etch-stop layer first. A SiO_2 film was deposited using plasma-enhanced chemical vapor deposition (PECVD) from $\text{SiH}_4/\text{N}_2\text{O}/\text{Ar}$ mixture for the subsequent CMP using Applied Materials Mirra polisher.

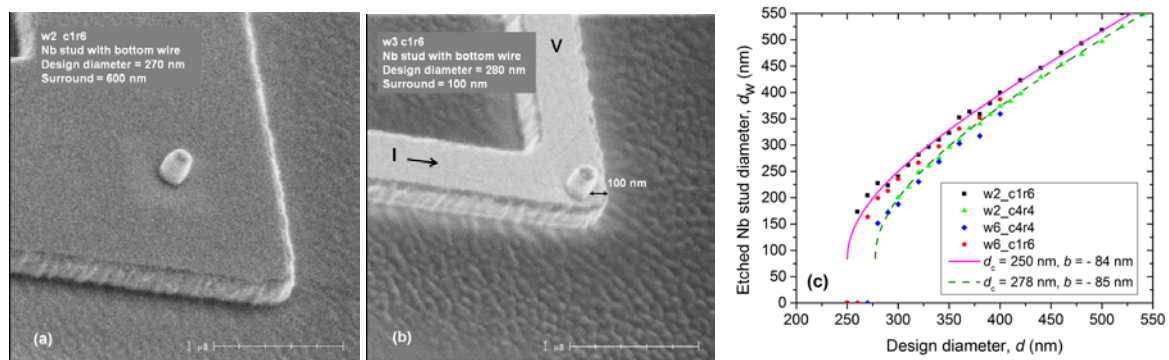


Figure 4. Etched Nb studs with various diameters on top of bottom Nb wire: (a) 270-nm design diameter, 600-nm surround; (b) 280-nm design diameter, 100-nm surround. The bottom wire has an L-shape that with the corresponding L-shape in the top wire will form a cross-bridge Kelvin resistor (CBKR) configuration for electric measurements of studs. (c) The bottom diameter of the etched Nb studs as a function of the design diameter.

We have found that the size of the photoresist features and etched Nb studs can be well described by the relationship $d_w = k(d^2 - d_c^2)^{1/2} - b$ for $d > d_c$, and $d = 0$ for $d \leq d_c$, as shown in figure 4(c). Here d is the design diameter, d_c is a photolithography cut-off size that depends on the photolithography parameters, and b is the process bias. The scaling factor k characterizes the accuracy of the projection optics and SEM magnification. We have found that for the stable and optimized process $d_c \approx 250$ nm, $k = 1 \pm 0.7\%$, and b is within the range of ± 50 nm.

The top wiring layer of Nb was deposited and patterned similarly to the bottom wiring and with the same overlap. The SEM picture of the completed stud-via structure is shown in figure 5.

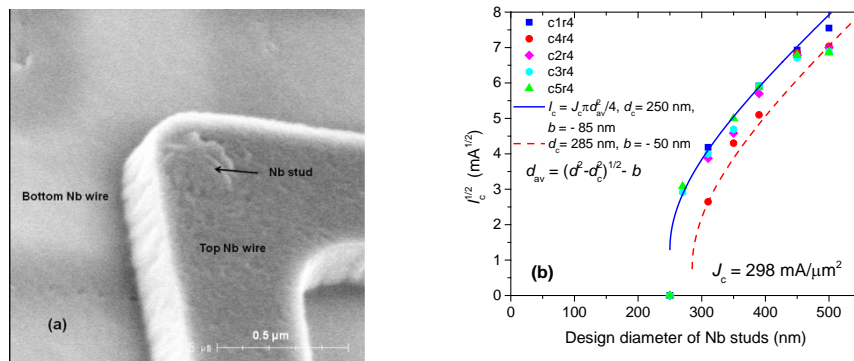


Figure 5. (a) SEM image of the completed stud-via structure with 350-nm stud between two L-shaped wires. Clearly visible is the top Nb wire, lighter blurry image is the bottom wire as seen through the planarized SiO₂ dielectric. The outline of the stud can be also seen due to a difference in niobium grain structure. (b) Critical current, I_c , of the fabricated Nb stud-vias along with the fits to $I_c = J_c \pi d_{av}^2 / 4$, where $J_c = 0.3$ A/μm² is the critical current density and d_{av} is the mean of the top and bottom diameters of the fabricated studs, shown for two values of the lithography cut-off parameter and process bias: $d_0 = 250$ nm $b = -85$ nm, and $d_0 = 290$ nm $b = -50$ nm.

4. Electrical test results and discussion

The critical currents, I_c , of the fabricated stud-vias are shown in figure 5(b). I_c scales with the actual area of the studs. The current density J_c was found to be $3 \cdot 10^7$ A/cm² (0.3 A/μm²), only about a factor of 2.5 lower than the Ginzburg-Landau depairing critical current density $J_c^{GL} = (2/3)^{3/2} B_c / (\mu_0 \lambda)$ in our films, where $\mu_0 = 4\pi \cdot 10^{-7}$ H/m, B_c - the thermodynamic critical magnetic field, λ - the magnetic field penetration depth [9]. Indeed, for Nb at 4.2 K, $B_c \approx 0.145$ T [10] and λ is in the range from 80 nm to 90 nm for our films. This gives J_c^{GL} in the range from 7×10^7 A/cm² to 8×10^7 A/cm². In the actual structure, the J_c should be somewhat lower than J_c^{GL} of the film due to the presence of an 8-nm Al

etch-stop layer at the interface between the Nb stud and the bottom Nb wire. On the other hand, in the studied range, the diameter of the studs is larger than 4ξ , where ξ is the coherence length that in our films is about 20 nm. Hence, instead of the depairing, the stud critical current can be caused by the entry and motion of Abrikosov vortices when the current-induced magnetic field at the stud surface reaches H_{c1} . This gives an estimate for the critical current density $j_c = H_{c1}/(\mu_0\lambda)$, where $H_{c1} = H_c \ln(\kappa + 0.08)/(\sqrt{2}\kappa)$ [11]. Using $\kappa = \lambda/\xi = 4$ for our films, we get $j_c \approx 0.36 \text{ A}/\mu\text{m}^2$ in a perfect agreement with the J_c observed in the fabricated Nb stud-vias.

Independently of the actual critical current mechanism, the observed critical currents are more than sufficient for the use of stud-vias in superconducting integrated circuits for interlayer connections. At $d = 0.5 \mu\text{m}$ the critical currents of stud-vias exceed those observed in etched contact holes of the same diameter filled with deposited Nb metal.

5. Conclusions

We have developed and demonstrated a novel process for making deep sub- μm superconducting multilayer interconnects for use in VLSI and ULSI superconductive digital circuits. These interconnects are formed using Nb/Al/Nb trilayer wiring layers by etching Nb studs in the top layer and Nb wires in the bottom layer of the trilayers with subsequent planarization of the formed interconnects by dielectric CMP. The purpose of this process development is to replace the currently used etched-contact holes filled with sputtered Nb that are too big for VLSI SFQ circuits. Nb stud-vias with diameters as small as 150 nm have been fabricated by the developed process. For the design diameters $\geq 280 \text{ nm}$, the yield of the fabricated Nb stud-vias was 100% on the test structures available. The critical currents of the obtained Nb stud-vias approach the maximum possible superconducting currents for Nb and are certainly sufficient for interconnects in superconducting VLSI circuits.

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