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Three-Dimensional Electro-Thermal Verilog-A Model of Power MOSFET for Circuit Simulation

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Abstract. New original circuit model for the power device based on interactive coupling of electrical and thermal properties is described. The thermal equivalent network for a three-dimensional heat flow is presented. Designed electro-thermal MOSFET model for circuit simulations with distributed properties and three-dimensional thermal equivalent network is used for simulation of multipulse unclamped inductive switching (UIS) test of device robustness. The features and the limitations of the new model are analyzed and presented.

1. Introduction

Today's circuit simulators are standard tools in the development and optimization of electronic systems. However, until now the simulations have been limited to electrical functions because the temperature dependences of parameters of simulation models available today are taken into account at the best by changing the static global temperature. In power electronic systems in particular, temperature is one of the critical parameters due to the non-negligible self-heating effects and the fact that many properties of power semiconductor devices are strongly temperature dependent [1]. The standard equivalent models of the power devices for circuit electro-thermal simulations consist of one-dimensional Cauer or Foster type thermal equivalent networks. The one-dimensional heat flow can be insufficient particularly for large power devices and large power pulses. An inhomogeneous temperature distribution caused by three-dimensional heat flow from the semiconductor chip to the package and cooling assemblies can cause an inhomogeneous distribution of the electric properties of the power device along the whole chip. Therefore, it is necessary to split the structure into several cells with thermal interaction in three dimensions. In this paper we present new electro-thermal model of power MOSFET for circuit simulation, which contains a dynamic link between electrical and thermal components description. Also the thermal equivalent network for a three-dimensional heat flow is shown. The designed electro-thermal model of the analyzed power MOSFET is used for a simulation of UIS test [2].

2. Thermal system description

During a search for an electrical analog model for heat conduction inside structure, we assume that a thermal system can be in general modeled with a discrete element electrical circuit, composed by resistances and capacitances, where the temperatures and the thermal powers are considered as voltages and currents, respectively (figure 1b) [3][4]. Power dissipation of the electrical circuit is determined at all times and a current proportional to the dissipated power I(t) is fed into the thermal equivalent network. The V_{Tj} node voltage represents the junction temperature inside the structure. All

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non-linear electrical temperature dependent parameters of the power structure are driven by the actual temperature distribution inside the structure [5]. Due to a close relationship with physical reality of the one-dimensional heat flow, the parameters for the *RC* equivalent circuit diagram can be derived directly from equation (1) and (2) [6]. The physical variables are specified in their thermal equivalents by using the geometries, thermal conductivities and thermal capacities of materials, where A is the surface, d_i is the thickness, κ and c are the thermal conductivity and heat capacity of the elements. Then we can define:

$$R_i \approx R_{th\,i} = \frac{d_i}{\kappa \cdot A} \tag{1}$$

$$C_i \approx C_{th\,i} = c \cdot d_i \cdot A \tag{2}$$

The modification of one-dimensional Cauer-type equivalent thermal network to three-dimensional network is shown in figure 1c [7].

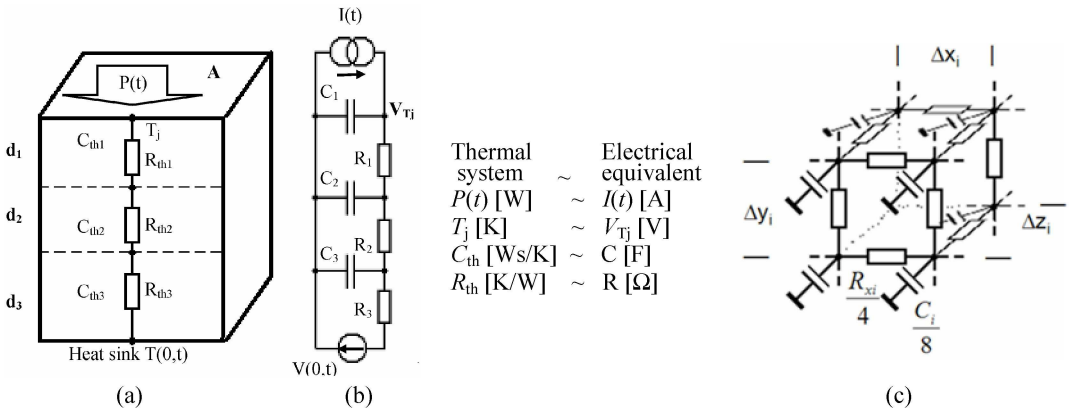


Figure 1. (a) Thermal structure, (b) Cauers electrical equivalent of the thermal system (c) equivalent thermal network for three-dimensional heat flow.

3. Structure description

The structure under investigation is the power super-junction vertical MOSFET [8][9] in DPAK 2 package (figure 2a). The two-dimensional cross section of the structure is shown in figure 2b. The trench gate MOSFET is created on top of the n^{++}-type doped substrate and n^{-}-type doped epitaxial layer. The super-junction trench, created by p-type and n-layers around an air gap, provides charge balance and a high breakdown voltage for low on-resistance. Referring to [10] and device simulation (figure 2c) the most of heat generated during the avalanche operation of UIS conditions is located at the bottom of the air gap epitaxial layer.

Electrical circuit is created by 8 × 8 transistor cells connected in parallel. The power MOSFET is electrically modelled with a SPICE Level 3 built in Verilog-A [11]. The electrical model is defined considering the temperature dependences of the most relevant parameters extracted from the characterization of the structure at different operating temperatures. The temperature dependence of threshold voltage V_{T0}, drain resistivity R_D, body diode D_B, leakage current through leakage resistance R_L, avalanche breakdown voltage V_{BR} and over current/thermal destruction S_{BURN} are implemented in the model [12].

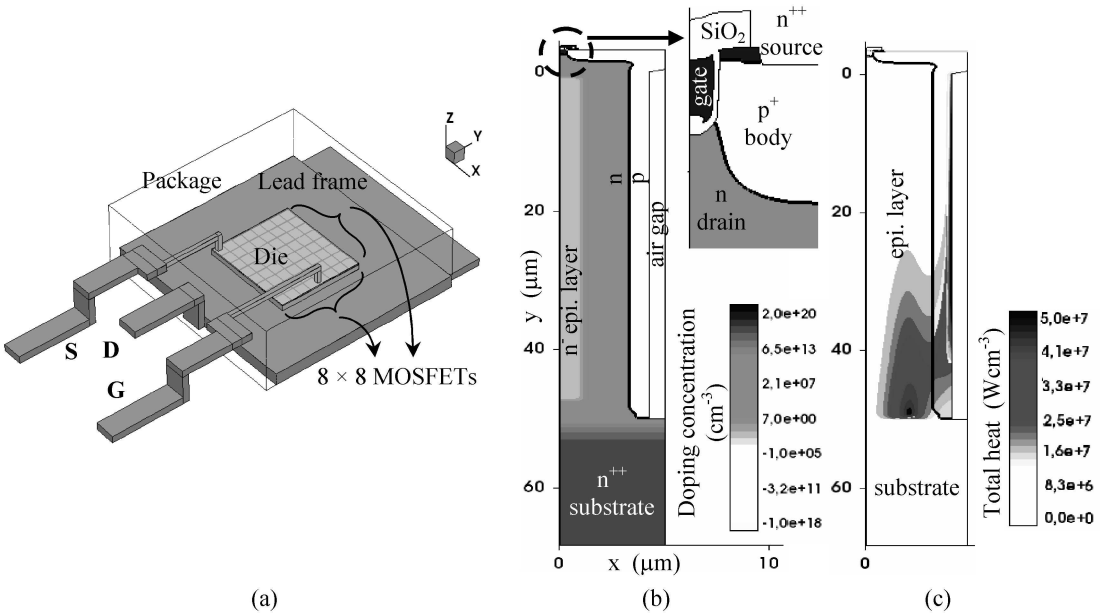


Figure 2. (a) Structure of the MOSFET in DPAK 2 package, (b) two-dimensional cross section of the super-junction MOSFET, (c) total heat distribution inside the structure during UIS breakdown condition.

Figure 3 shows experimental data compared with simulations of transfer characteristics at different temperatures, output characteristics for different gate biases and *C-V* characteristics of the analyzed MOSFET. The three-dimensional thermal equivalent network is created by an RC network allowing three-dimensional heat flow. The three-dimensional mesh is generated automatically by Verilog-A program cycle which allows easy use user defined placement. The thermal material properties, geometry and dimensions are used as the input parameters for mesh creation. Only the lead frame, substrate, epitaxial layer and package are taken into account for the simplicity of the model. The current sources which represent thermal heating are placed between the epitaxial layer and substrate where occurs heat generation during avalanche conditions. The electrical circuit diagram of one transistor cell and view of the tree-dimensional equivalent thermal mesh are shown in figure 4.

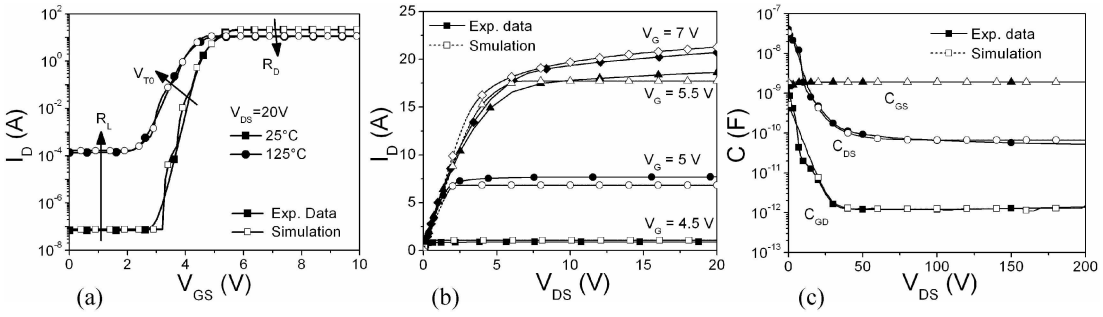


Figure 3. Experimental data and simulation of (a) transfer characteristics at different temperatures, (b) output characteristics and (c) *C-V* characteristics of analyzed MOSFET.

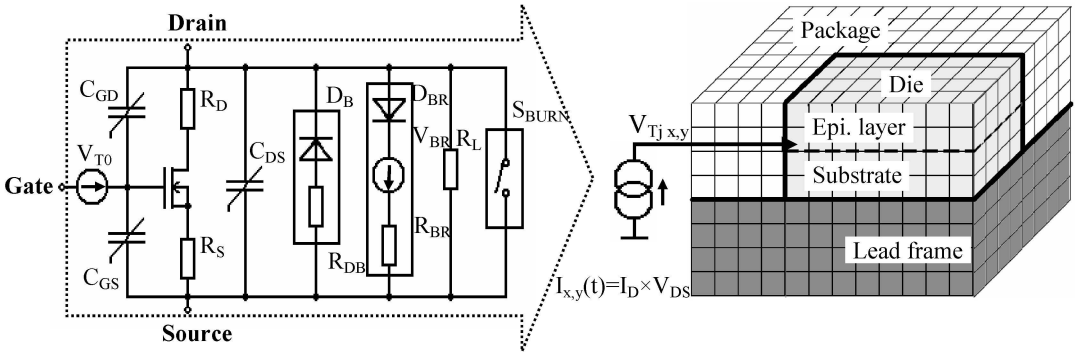


Figure 4. The electrical circuit diagram of one transistor cell (left) and view of the tree-dimensional equivalent thermal mesh (right).

4. Experiment

The designed electro-thermal model of the analyzed power MOSFET has been used to simulate the multipulse UIS test. UIS condition represents the robust test of circuit switching operation for evaluating the ruggedness, which characterizes a device capability to handle high avalanche currents during the applied stress. In case the current flowing through the inductance is quickly turned off, the

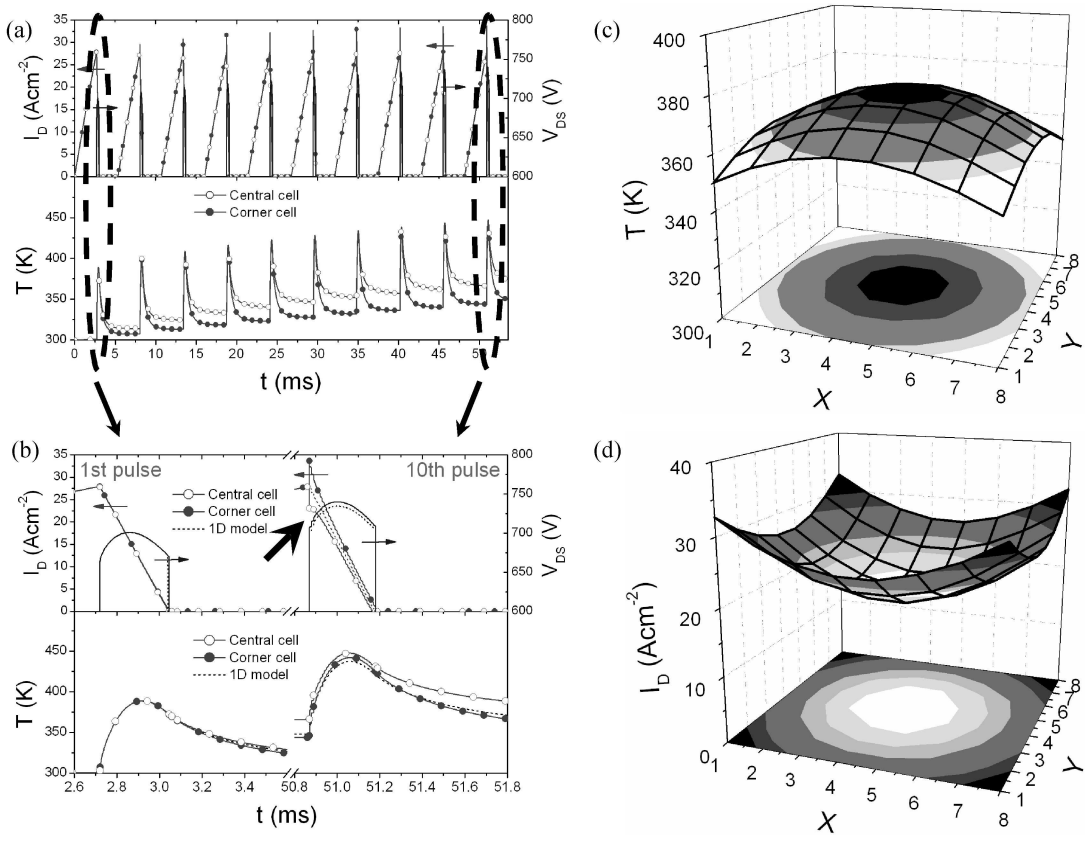


Figure 5. (a) Comparison of the drain current, drain voltage and temperature of the corner and central parts during multipulse UIS test. (b) Comparison of simulation with three-dimensional and one-dimensional thermal network. (c) Temperature and (d) current density distribution at the beginning of the tenth UIS pulse for structure using three-dimensional thermal network.

magnetic field induces a counter electromagnetic force that can build up surprisingly high potentials across the device under test. Comparison of the drain currents and the temperatures of the corner and central parts cells of the transistor are shown in figure 5a and figure 5b. The temperature is almost evenly distributed and the currents through the transistors are equal during the first pulse. After some period of the power load, the temperature and breakdown voltage of the central transistor cell increase more significantly in comparison with the corner transistor cell because the corner cell is cooled more effectively. Therefore, the corner current becomes higher what is clearly seen at the beginning of the tenth UIS pulse. The inhomogeneous distributions of the temperature and current density are shown in figure 5c and figure 5d. Figure 5b shows comparison of the multipulse UIS for the MOSFET model using three-dimensional and one-dimensional thermal network. The inhomogeneous behavior along whole structure is neglected for one-dimensional simulation and the differences of the structure temperature and the drain breakdown voltage become more significant for the longer time simulation (tenth UIS pulse).

5. Conclusions

The super-junction vertical MOSFET was used for simulation of multipulse UIS test. The simulation approach helps to assess the device robustness by means of the evaluation of both temperature and current distributions in the MOSFET structures operating under critical conditions. The implemented three-dimensional thermal flow and distributed parameters of the MOSFET transistor provide more realistic simulation results. The advantages of the method are the relative simplicity of implementation, the speed of simulation time and the capability of full structure analysis.

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