

Electro-Thermal Analysis and Optimisation of Edge Termination of Power Diode Supported by 2-D/3-D Numerical Modelling and Simulation

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Abstract. Numerical modelling and simulation provide an efficient tool for analysis and optimization of device structure design. In this paper we present the analysis and the geometry optimization of the power module with high power pin diode structure supported by the advanced 2-D/3-D mixed-mode electro-thermal device simulation. The structure under investigation is P^+NN^+ power diode device designed for high reverse voltages and very high forward currents, with a maximum forward surge current up to 2.7 kA.

1. Introduction

Various physical phenomena in semiconductor devices are very complex and, depending on applications, are described by partial differential equations of different level of complexity [1]. The parameters of electro-physical models and the boundary conditions of used equations can be very complex. They depend on microscopic physics, the structure of the device, its actual temperature, and applied biases. Device simulator SDevice [2] allows to simulate electrical characteristics for selected combinations of transport equations and physical models. These models provide the potential to simulate a wide spectrum of semiconductor devices. Many parameters of power semiconductor devices are temperature dependent. Their thermal behaviour contributes to the overall performance of the system. Thermodynamic simulation allows analysis of the influence of structure edge termination profile on the electrical properties of analysed diode. Lowering the diode temperature by structure edge termination shape will allow withstanding the higher current pulses and suppressing the damage of the analysed structure by thermal breakdown. Electro-thermal simulation provides an overview of the chip power and heat dissipation and corresponding temperature distribution for various pulses of load currents [3]. 3-D numerical modelling and simulation using well calibrated parameters provide an efficient tool for analysis and optimization of the device structure design, prediction of its properties, and electro-physical interpretation of obtained data as well.

2. Problem description

Maximum peak forward current is the maximum current which can diode sustain in forward bias mode. Its value is limited by the diode junction thermal resistance and thermal capacity and it is usually much higher than the average operational current due to thermal inertia. It is based on a fact that it takes a non-negligible finite time interval for the diode to reach the maximum temperature for a given current. Ideally, this value should be infinity [4]. This current peak can generate intensive heat



(Joule losses) due to the thermal resistance of metallization and passivation layers. The heat dissipation into the individual layers and their interfaces may be insufficient and it can lead to uncontrolled temperature increase which finally destroys the diode [5]. Therefore, it is necessary to find the critical regions and to optimize the device structure. 2/3-D numerical electro-thermal modelling and simulation provide a very effective solution of this problem. In a mixed mode electro-thermal simulation we combine the electro-thermal simulation of diode chip and analysis of the chip packages from a thermal budget management perspective. The framework required for such analysis is developed and some examples are presented to illustrate its role and effectiveness. The electro-thermal simulations were performed by SDevice tool. There is a possibility to simulate the whole spectrum of semiconductor devices, from high-power to submicron devices. The thermodynamic (or non-isothermal) model [6] extends the drift-diffusion approach to account for electro-thermal effects, under the assumption that the charge carriers are in thermal equilibrium with the lattice. The thermodynamic model is defined by the Poisson equation, current continuity equations, and the lattice heat flow equation (equation 2). The relations generalized to include the temperature gradient as a driving term:

$$J_{n,p} = -nq\mu_{n,p}(\nabla\phi_{n,p} + P_{n,p}\nabla T) \quad (1)$$

where J_n is the electron current density, J_p is the hole current density, μ_n and μ_p are the electron and the hole mobilities, ϕ_n and ϕ_p are the electron and the hole quasi-Fermi potentials, P_n and P_p are the absolute thermoelectric powers [7]. To calculate the temperature distribution inside the device due to self-heating, the following equation is solved:

$$\begin{aligned} c \frac{\partial T}{\partial t} - \nabla \cdot \kappa \nabla T = & -\nabla \cdot \left[(P_n T + \phi_n) \vec{J}_n + (P_p T + \phi_p) \vec{J}_p \right] - \left(E_C + \frac{3}{2} k_B T \right) \nabla \cdot \vec{J}_n \\ & - \left(E_V - \frac{3}{2} k_B T \right) \nabla \cdot \vec{J}_p + qR(E_C - E_V + 3k_B T) \end{aligned} \quad (2)$$

where κ is the thermal conductivity and c is the lattice heat capacity. E_C and E_V are the conduction and the valence band energies, respectively, and R is the recombination rate. Simulator performed the analysis for small part of the investigated device. By default, SDevice assumes a 'thickness' (effective gate width along the z-axis) of 1 μm . Area Factor is a multiplier for the electrode currents and charges.

3. Modelling and simulation

The structure under investigation is the P+NN+ power diode designed for the reverse voltages up to 1800 V and the high forward currents up to 100 A with a maximum forward surge current up to 2,7 kA. Due to the large diode dimensions ($9,8 \times 9,8 \text{ mm}$) and approximate symmetry of the device only a small part of the structure marked by rectangle in figure 1a was used for simulation. The cathode was created by diffusion of a highly doped n-type layer ($N_d = 2 \times 10^{20} \text{ cm}^{-3}$) into the highly resistive ($63 \Omega\text{cm}$) n-type substrate with thickness of 350 μm . The anode was formed simultaneously by highly doped p-type layer ($N_a = 2 \times 10^{20} \text{ cm}^{-3}$) on the opposite side of substrate with a pn junction located 290 μm from cathode. To achieve a good agreement between measured and simulated breakdown voltages we need to calibrate the electro-physical models. For simulation of I - V characteristics we used University of Bologna model (UniBo) [8] with default values of carrier lifetimes for generation-recombination mechanisms equal to $\mu_{\max}(\text{electrons}) = 1 \times 10^{-5} \text{ s}$, $\mu_{\max}(\text{holes}) = 3 \times 10^{-6} \text{ s}$ and corresponding values of parameters characterizing Trap Assisted Auger recombination (TAA) $c_n^{\text{TAA}} = c_p^{\text{TAA}} = 1 \times 10^{-12} \text{ cm}^3 \text{ s}^{-1}$ [9, 10].

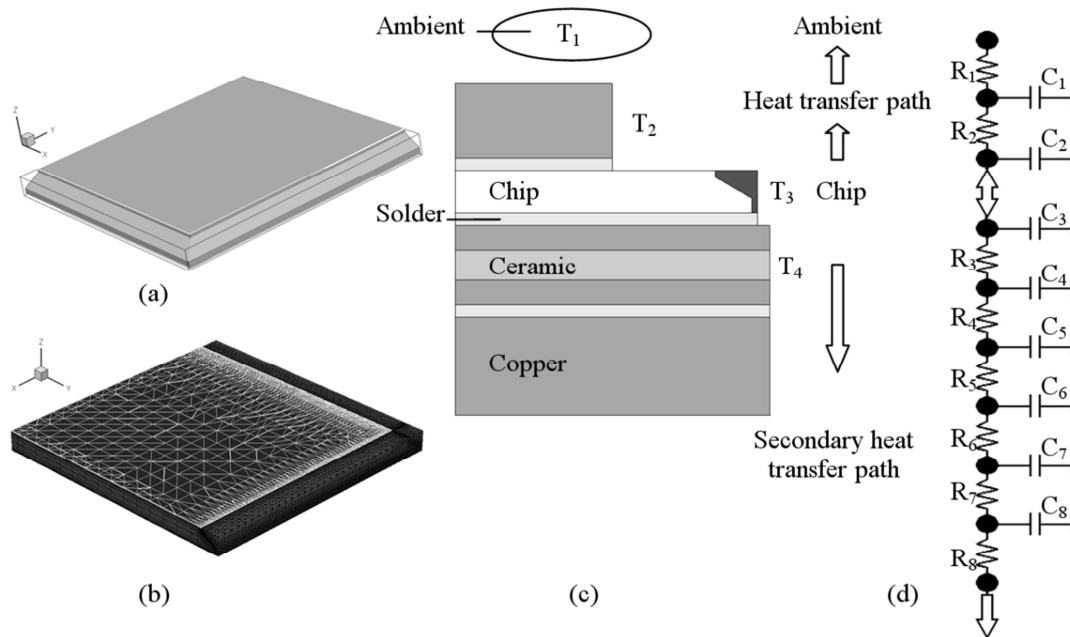


Figure 1. (a) Diode chip without metallization and passivation layer. (b) Structure with passivation layer and grid without package. (c) Cross-sectional view of a chip in package. (d) Thermal RC network.

The best agreement with experimental data we found using $\tau_{max}(electrons) = 3 \times 10^{-3} s$, $\tau_{max}(holes) = 5 \times 10^{-4} s$ and $c_{pn}^{TAA} = 1,3 \times 10^{-12} cm^3 s^{-1}$ which corresponds to the TAA lifetimes dependent on the carrier densities as follows:

$$\frac{1}{\tau_{n,p}^{TAA}} = c_{p,n}^{TAA} (n + p) \quad (3)$$

The doping dependence of the Shockley-Read-Hall (SRH) recombination lifetimes was modeled in SDevice by the Scharfetter relation.

The experimental characteristics are depicted in range which corresponds to the main application area of the investigated power devices. We achieved a very nice agreement between experimental data and simulations using the calibrated values of parameters. The simulated value of $V_{BR}^{sim} = 2161 V$ nicely coincides with that obtained from experimental measurements $V_{BR}^{exp} = 2187 V$ within experimental error (figure 2).

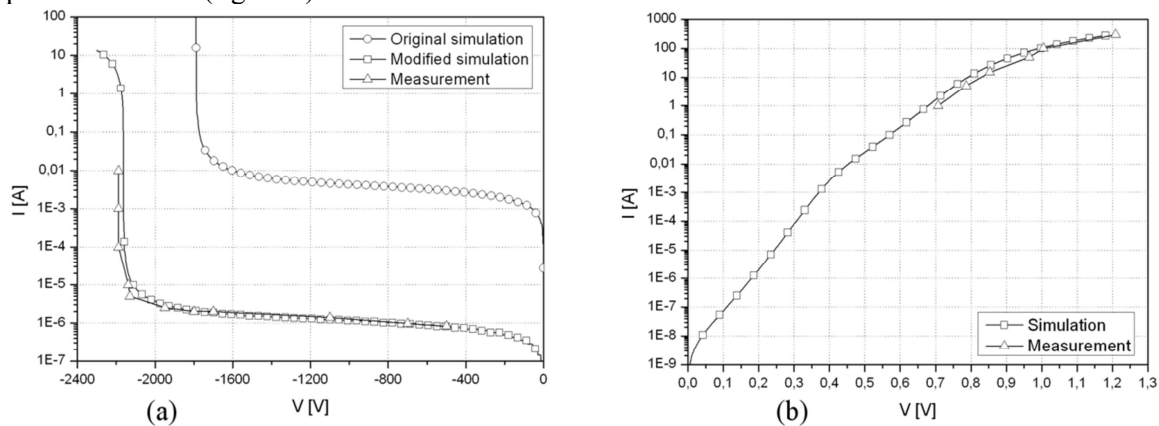


Figure 2. Simulated and measured I–V characteristics. (a) Reverse and (b) forward.

4. Experimental results

As the correct thermal modeling plays a significant role in the combined electro-thermal modeling and simulation of power devices the additional metallization and passivation layers were added to perform more realistic heat dissipation from the diode structure. Figure 4 shows a typical chip in package with a simplified thermal resistance network model. For the short current pulses up to 10 ms we can assume, that the primary heat transfer path through the interface material, spreader and heat sink to the ambient on the top of the structure is of sufficiently low thermal resistance, so that any heat dissipation through the secondary path can be neglected due to high thermal resistance of ceramic block [11, 12]. The heat path from the chip to the back of the lead frame or to a heat sink can be modeled, for example, using the transmission line equivalent circuit diagram. In this case, the current source represents the power dissipation (heat flow) occurring in the chip in the thermal equivalent. Analogous to the electrical transmission line, thermal resistance and thermal capacitance (figure 1d) per unit length need to be considered for exact characterization of the thermal properties of individual components. However, to simplify the description, it is helpful and permissible to combine single volume elements in lumped equivalent elements (R_{th} , C_{th}). Both contact and component resistances are included in these quantities. High thermal resistance of passivation layers and their interfaces prevent the heat dissipation from the chip, which subsequently can destroy the diode. The simple diode structure (without passivation layers and metallization) sustain maximum peak current $I = 1100$ A in the dynamic simulation, while the measured maximum peak current was $I = 2700$ A. Electro-physical model of the diode with additional layers was used for the simulations and for the analysis of internal properties of the diode structure during the peak current pulse $I = 3100$ A.

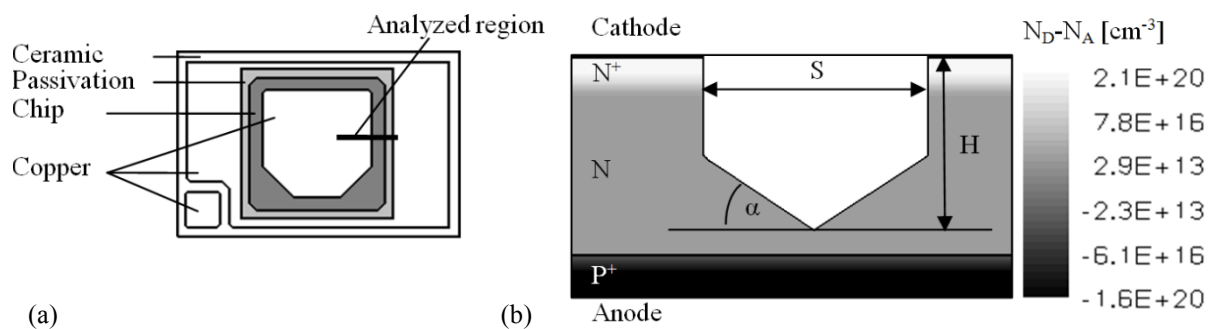


Figure 3. (a) Structure layout, (b) Semiconductor cross section: S , H , α – parameters of edge termination.

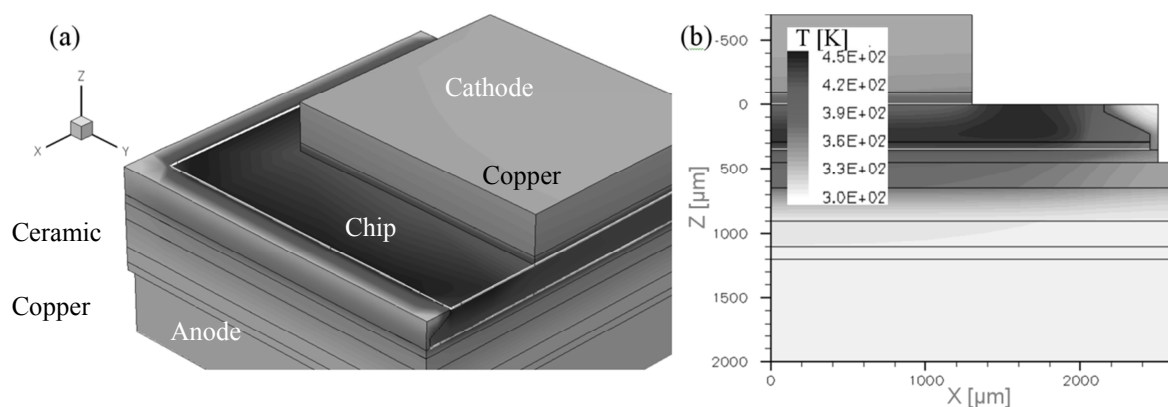


Figure 4. Temperature distribution (a) 3-D profile, (b) 2-D simulation cut during 3100 A inside structure int the time of 7.5×10^{-3} s.

We focused on structures with geometry varies. Several modifications of the diode edge termination using different shapes (angle α) height (parameter H) and width (parameter S) of side wall were designed (figure 3). Measured samples are structures 1-6 marked in figure 5 c, d. The combinations of different simulation parameters influence the diode structure breakdown voltage and distribution of the current density at the peripheral regions of structure as well. Figure 5 shows the dependence of the maximum temperature on the width, depth and angle of edge termination profile with angles 30° and 60° . Characteristics were made for 3100 A stress and in the time of current pulse 7.5×10^{-3} s. All simulations were performed at the same conditions. We observed, that increasing the angle of edge termination, the maximum temperature decreasing. Increasing the width and depth of the edge termination profile, the temperature rises. The lowest temperature was observed for a structure with the angle of 60° . While for small angles (up to 30°) minimum temperature of 430 K was obtained, for structure with the angle of 60° the temperature reaches its maximum of 429 K from all simulations.

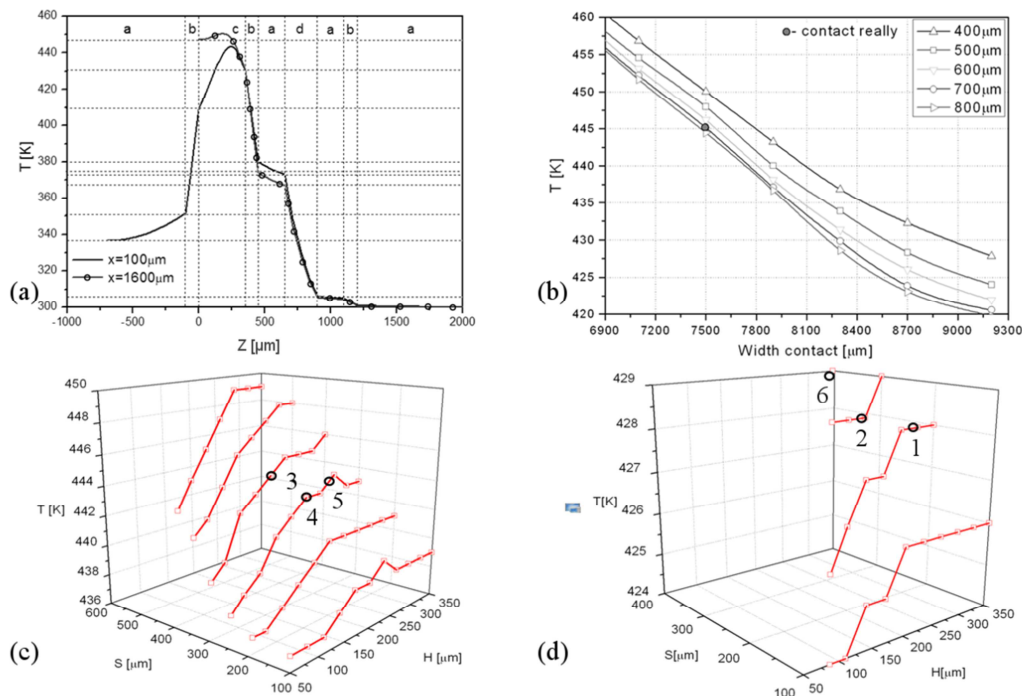


Figure 5. (a) Temperature in 2-D simulation cut, (b) maximum temperature dependence on width and depth of cathode thickness. And max. temperature dependence on height, width and angles (c) 30° , (d) 60° of side wall fewer than 3100 A stresses in the time of 7.5×10^{-3} s.

5. Conclusions

The 2-D numerical device modelling and simulations were applied to the study of electro-thermal behaviour and reliability of analysed device. The simulation of static breakdown voltage V_{BR} was used for the calibration of model parameters. Very good agreement between experimental and simulation results were obtained. Simulation employing the thermodynamic transport model allows analysis of the influence of structure edge termination profile on the electrical properties of analysed diode. The structure with angle 60° exhibits the best results withstanding the current stresses. Lowering the diode temperature by structure edge termination shape will allow withstanding the higher current pulses and suppressing the damage of the analysed structure by thermal breakdown. Finally, good agreement between simulations, measurements and theoretically calculated critical temperatures for diode structure confirm the validity of our approach very well.

6. References

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