FPGA-BASED PHASE AND MODULE IMPEDANCE METER

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Abstract. A conductance catheter system measures the left ventricle volume by measuring the blood conductance in the cavity. It is known that there are some limitations and errors related to these assumptions. New trends claim that a nonlinear conductance-volume relationship is observed and volume measurement not only has a resistive behavior but also has a capacitive component. It is exclusively due to the myocardial muscle; even further, myocardial impedance varies in both phase and magnitude between end systole and end diastole decreasing the accuracy of volume measurement. The incorporation of an appropriate technology catheter system based on FPGA is proposed allowing measure impedances instead of conductances. Thus, the system can measure impedance module and phase in order to accurately estimate the left ventricle blood volume. The system is digitally designed and evaluated with known pattern impedances with electrical characteristics similar to those presented in the left ventricle (module range of 6.8Ω to 47Ω and phases from 2° to 90°).

1. Introduction

The development of the conductance catheter method has enabled the evaluation of left ventricular function in the human heart in vivo [1-3]. This method allows to measure real time ventricular conductance which becomes, using a conversion equation, in the left ventricular volume; its process includes a series of approximations. The first linear classic conductance-to-volume conversion equation was proposed by Baan et al. in 1989 [1]; this widely used linear equation assumes that the catheter-generated electric field is homogeneous inside the ventricle. Subsequently, a second conversion equation has been presented by Wei *et al* [4] in which a nonlinear conductance-volume relationship is presented in murine hearts using a single catheter section. This research group showed that if the measured chamber is not a symmetric cylinder and/or the catheter is not placed exactly along the central longitudinal axis of the chamber, linear classic equation restricts the accuracy of the volume estimation [5-6]. Furthermore, the accuracy of these equations is also determined by the contribution of the myocardium [7-8], known as the "parallel conductance Gp". Wei's research demonstrated that Gp varies in both phase and magnitude between end systole and end diastole. Using this concept, they proposed that both the capacitive and the resistive properties of the myocardium were substantial and neither should be ignored [9]. Hence, they proposed to measure the left ventricle admittance (magnitude and phase) instead the conductance. However, all these investigations were conducted in mouse hearts using a single section catheter. There is a lack of Gp studies in large or dilated hearts. To elucidate these aspects, it is necessary to build a system able to measure admittance

(magnitude and phase) using a catheter for healthy and/or dilated human hearts. Considering that our research group has recently developed a based-FPGA (Field Programmable Gate Arrays) digital left ventricular volume system [10], this paper proposes to incorporate the phase and magnitude impedance measurement for each of five sections conductance catheter and to evaluate the performance of the system using known resistances and capacitances.

2. Theoretical background

2.1. Ventricular volume measurement
It has been stated that ventricular impedance/admittance is not purely conductive; instead it is in part capacitive. Since blood can be modeled with a resistance (R), the capacitance is a consequence of myocardium, which can be modeled as a parallel R-C impedance. Myocardium contribution can be known by measuring both: ventricular admittance phase (Φ_i [degree]) and module ($|Ymeas_i|$ [S]) [6] The phase values that result from myocardium contribution goes from 5° to 60° approximately, and myocardium admittance (Y_{mi} [Ω^{-1}]) can be calculated as follow:

$$Cm_i = \frac{|Ymeas_i| * \sin\emptyset_i}{2\pi f} \tag{1}$$

$$gm_i = \frac{Cm_i \times \sigma_m}{\varepsilon_m} \tag{2}$$

$$Ym_i = gm_i + j2\pi f Cm_i \tag{3}$$

where Cmi [F], σ_m, ε_m, gm_i [S] represent the myocardium capacitance, conductivity, permittivity and conductance respectively and f [Hz] is the frequency of the signal to be introduced into the body. The index i=1,…,5 belongs to each catheter section.

If myocardium admittance is determined, blood conductance (gb_i [S]) can be obtained using equation (4).

$$gb_i = |Ymeas_i| * cos\emptyset_i - gm_i \tag{4}$$

where gm_i [S] is obtained for each catheter section, ventricular volume can be estimated using any of the two equations that follow: a) Baan traditional equation [1] or b) Wei equation [4].

The first equation assumes that the electric field generated by the catheter system is homogeneous, and ventricular volume can be calculated using equation (5)..

$$Vol_i = \frac{1}{\alpha} * \rho * L^2 * gb_i \tag{5}$$

In this equation Vol_i [V] represents volume instantaneous signal, α is an empirical factor used for calibration, ρ [$\Omega*m$] is the blood resistivity and L [m] is the distance between electrodes.

The second equation solves the problem that emerges from considering a homogeneous electric field inside the ventricle, and ventricular volume can be calculated using equation (6), where $\varUpsilon$ is an empirical factor used for calibration.

$$Vol_i = \frac{\varUpsilon}{\varUpsilon - gb_i} \rho L^2 gb_i \tag{6}$$

The equations (1) to (6) are solved using a commercial software (LabView 2009, National Instruments Inc.), which receives ventricular admittance phase and module measured for each catheter section.

2.2. Signal characteristics
By means of a multi-electrode catheter, a current is injected into the left ventricle cavity, and the voltage between each pair of electrodes is measured (figure 1).
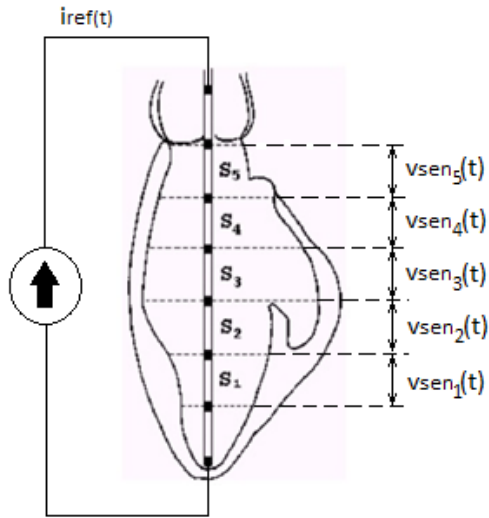
Figure 1. The reference current (*Iref(t)*) is injected between outer electrodes, and a voltage signal is measured between each pair of electrodes (*Vsen$_i$(t)*).
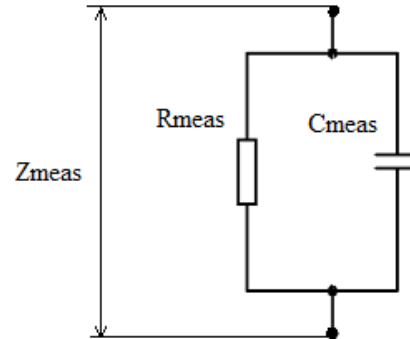
Figure 2. Circuital model of the impedance measured at each catheter section.

The injected current *Iref(t)* can be expressed by means of equation (7), where |*Iref*| is its module and *fref* [Hz] is the working frequency.

$$Iref(t) = |Iref|\cos(2\pi\ fref\ t) \tag{7}$$

Ventricular impedance (Z_{meas}), presented by equation (8), can be modeled as a parallel R-C circuit (figure 2) where the resistive part (R_{meas}) represents the sum of blood and myocardium resistances while the capacitive part (C_{meas}) model the cardiac muscle capacitance. Its reciprocal is the ventricular admittance (Y_{meas}) -equation (9)-. Ventricular impedance module and phase can be calculated using equations (10) and (11), respectively.

$$Z_{meas} = R_{\text{meas}} // \left(\frac{1}{j2\pi f_{ref} C_{meas}} \right) = \frac{R_{\text{meas}}}{j2\pi f_{ref} R_{meas} C_{meas} + 1} \tag{8}$$

$$Y_{\text{meas}} = \frac{1}{Z_{\text{meas}}} = \frac{1}{|Z_{\text{meas}}|} \angle - \emptyset_{meas} \tag{9}$$

$$|Z_{\text{meas}}| = \frac{R_{meas}}{\sqrt[2]{1 + \left(2\pi f_{ref} R_{\text{meas}} C_{meas}\right)^2}} \tag{10}$$

$$\emptyset_{\text{meas}} = -\tan^{-1}\left(2\pi f_{ref} R_{\text{meas}} C_{meas}\right) \tag{11}$$

If R$_{meas}$ and C$_{meas}$ are varying during cardiac cycle; hence, Z_{meas}, |Z_{meas}| and Φ_{meas} are also variable signals.

The current *Iref* flowing through the impedance Z_{meas} produce the voltage V_{sen} represented as a phasor and as function of time in equations (12) and (13), respectively.

$$V_{sen} = I_{ref} Z_{meas} = |I_{ref}||Z_{vent}| \angle \emptyset_{meas} \tag{12}$$

$$v_{sen}(t) = \left|I_{ref}\right|\left|Z_{\mathrm{meas}}\right| \cos\left(2\pi f_{ref}t + \emptyset_{meas}\right) \qquad (13)$$

$|Z_{meas}|$ can be modeled as a periodic signal with a fundamental frequency f_m equal to cardiac frequency, plus a constant value that is never zero. So, $V_{sen}(t)$ is an amplitude modulated signal where *Iref* is the carrier and $|Z_{meas}|$ is the modulating one.

3. System description

3.1. General scheme
The equipment acquires and processes signals from the five sections of the catheter and delivers voltage values that are proportional to the impedance modulus and phases (of each catheter section). Finally, it transmits the data to a PC using a LabView interface where admittances and volumes are calculated (figure 3).
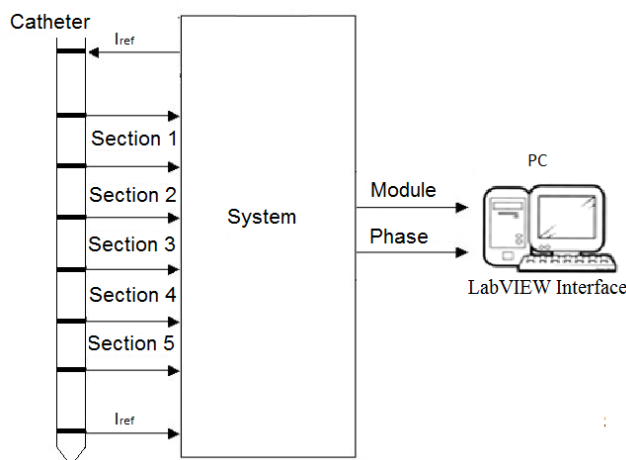

Figure 3. Connection diagrams (multielectrode catheter, FPGA-based system and PC). Iref, current flowing between outer electrodes. Each section voltage is processed and conditioned for transmission to the PC.

3.2. FPGA-based system
Figure 4 shows the schematic of the phase and module meter. It is composed of two parts, a digital one implemented in a FPGA and an analog one which is in contact with the biological element.

FPGA generates the digital reference current Iref(t) using a 12 bits DAC (Digital-to-Analog Converter) and a signal conditioner. Iref(t) is injected into the left ventricular between outer catheter electrodes. The signals at each catheter section are amplitude-modulated (AM) voltage signals, where the carrier is Iref(t) and the modulating signal is the biological signal. The AM signals, prior isolation, are digitized using an ADC (Analog-to-Digital Converter) and then they enter into FPGA for processing. The digital stage is a logical design configured in an Altera FPGA (FLEX 10K 70RC240; Altera Corp.) The logic equations are implemented with Quartus II version 9.0 development system (Web Edition). The design is carried out by combination of schematic and VHDL hardware description language forms. The logical design does the following tasks: 1) generate a 12-bits digital carrier signal using a ROM; 2) perform phase detection by measuring the time difference between the zero-crossing points between Iref(t) and Vsen(t); 3) calculate the phase; 4) demodulate Vsen(t) in order to detect the impedance module, and finally, 5) control the 12-bits ADC and the Analog Multiplexer.

Furthermore, analog stage is composed by: 1) a 12-bits DA R-2R converter (12-bits DAC); 2) a signal conditioner that consists of a 4th order band-pass filter with Sallen-Key structure, a multi-electrode catheter and an integrated 12-bits AD converter (12 bits ADC).

The Instrumentation amplifiers and Analog Multiplexer blocks are part of the previous system developed by Gómez López [2].
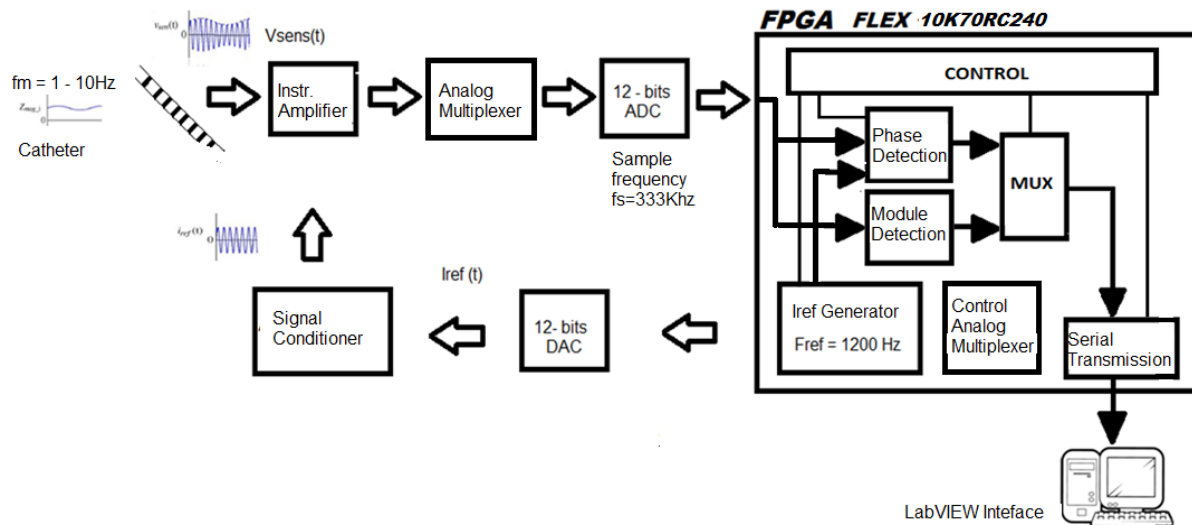
Figure 4. Schematic diagram for phase and module impedance measurement.

3.3. Analog stage

3.3.1. Precision 12 bits digital to analog converter (12 bits-DAC)

The 12-bit DAC is a resistor ladder network that uses only two resistance values (R and 2R). For its implementation three CD4053BC analog multiplexers (Fairchild) and several electronic switches are used. One input is connected to the reference voltage (5V) and the other is grounded (0V). In order to adapt the voltage levels between the FPGA (0V for a '0' logic level and 3.3V for a '1' logic level) and the multiplexers, three CD4071BC gates are used (National Instr.).

12-bit DAC has a 2mV resolution and a 11.8mV offset error. The ladder resistor network consists of several precision resistors of 2KΩ and 1KΩ with a 1% tolerance.

3.3.2. Signal Conditioner

The DAC output is a constant amplitude and 1200Hz frequency signal. It has high frequency harmonics introduced by the switching of the multiplexers and other components that make up the DA converter. So, this signal is entered to a band-pass filter with $fc_{LOW-PASS}$=3600Hz and $fc_{HIGH-PASS}$ = 400Hz.

For the low and high-pass filters design, a 2nd Order Butterworth filter with Sallen-Key structure is chosen, which results in a 4th order band-pass filter. Each filter is implemented using two LF353 operational amplifiers (Fairchild) and a RC resistor network.

3.3.3. Analog to digital converter (ADC)

The analog to digital converter is implemented using a 12 bits ADS7800 (Burr-Brown) integrated circuit and a 3us sampling time. It is a successive approximation AD converter with a sample and hold circuit and two ± 5V or ± 10V analog inputs. The RC (Read / Convert) active-low input signal initiates the conversion. While the conversion is performed, the input lines are disabled, the output data becomes high impedance and BUSY output turns to low. When data is available BUSY output turns to high level which indicates to the control logic that a binary word can be read.

The frequency of the analog signal that enters the converter is fref = 1.2KHz and the sampling rate is 333kHz, therefore the minimum phase that can be measured is:

$$\varnothing_{MIN} = \frac{T_S}{Tref} \times 360° = \frac{3\mu s}{834\mu s} \times 360° \tag{14}$$

$$\varnothing_{MIN} = \frac{3\mu s}{834\mu s} \times 360 \approx 2° \tag{15}$$

3.4. Digital stage

Figure 5 depicts the logic blocks of the digital stage that are implemented on the EPF10K70RC240 device (Altera). The 25.175MHz clock signal (Clock) is provided by a crystal oscillator from an educational board (UP2 Education Board, Altera). Iref [11 ... 0] is a 12-bits output bus that reconstructs a 1.2KHz sinusoidal signal using a 12-bit DA converter and provides the current injected into the catheter. VAM [11 ... 0] is a 12-bit bus coming from the output of the ADS7800 analog to digital converter. VAM represents the sensed and digitized AM signal at each catheter section. BUSY is an input digital signal that comes from the 12-bits ADC and indicates to the control logic that conversion data are ready to be read. RC is the output signal that comes from digital interface and indicates the start of the 12-bits ADC conversion. This signal is synchronized with the clock signal. Cmux [2 ... 0] is a 3-bits bus and it is connected to the CD4097 Analog Multiplexer (Texas Instruments) control inputs. This control inputs allows multiplexing the five channels of the catheter. TX is an output signal needed for RS232 serial transmission.

The ROM MEMORY generates the 12 bits current (carrier). The 333 kHz FREQUENCY DIVIDER generates a 333 KHz synchronic signal using a 25.125 MHz external clock. ADC CONTROL indicates the start of conversion. ANALOG MUX CONTROL commands the control input of a CD4097 analog multiplexer. INPUT stores VAM input signal temporarily, until new data are ready, besides this block works in synchronization with the ADC CONTROL block. PHASE detects the zero-crossing of the reference signal (Iref(t)) and VAM voltage signal, and then this block calculates the phase difference among them. MODULE demodulates VAM by means of positive peak detection. MULTIPLEXING AND TRANSMISSION condition the phase and module signals of the impedances presented at each catheter section for serial transmission to the PC.
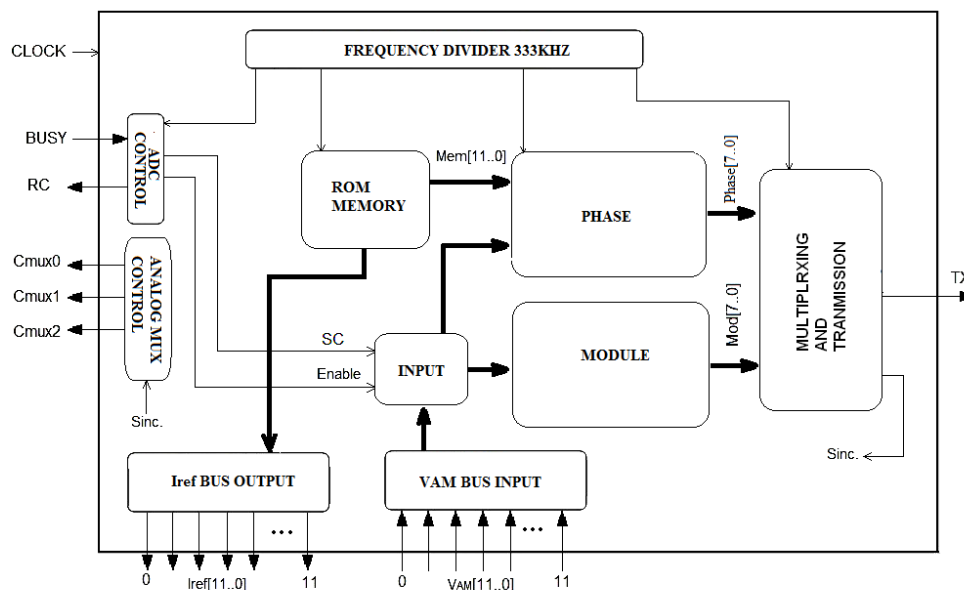

Figure 5. FPGA digital stage.

3.4.1. Phase detection

Phase detection is based in the method of zero-crossing detection. Having determined the zero crossings of the Iref [11 ... 0] reference signal and VAM [11 ... 0] sensed signal, this block is responsible for calculating the phase between the two signals. It consists of a JK flip-flop and a counter, when it detects a zero in Iref is activated the set input of the flip-flop and when it detects a zero in VAM is activated reset input of the flip-flop. The Iref [11 ... 0] signal is taken as a reference to measure the phase. The output of the flip-flop is the enabler of an 8-bits counter with count up. The

account obtained while is enabled is proportional to the time between the zero crossings of the two signals.

3.4.2. Detection Module
Module detection consists in demodulating VAM [11 ... 0] by means of detecting the peaks of the modulated Iref[11 ... 0] signal. An algorithm that compares three VAM consecutive points and stores the larger one is implemented. This comparison is carried out using two magnitude comparators (Library Parameterized Module Quartus) that compare the magnitude of a point with the magnitude of the other two ones. A moving average filter is used to prevent false peaks detections due to noise or interference from other systems.

3.4.3. Multiplexer and transmission
Once the voltage values proportional to module and phase of each of the five catheter sections are determined, they are multiplexed and serially transmitted to the PC. A RS232 serial transmission is used for communication between the FPGA device and PC. This transmission allows asynchronous communication between the two devices, but a previous RS232 to USB conversion is needed. The duration of each bit transmission is determined by the speed at which the data transfer is performed. The digital multiplexer and transmitter were developed in VHDL language and they work synchronously with a 9600Hz frequency.

Transmission sequence is the next one: phase and impedance module of the first section, phase and impedance module of the second section, and this sequence continues until the module and phase values of the five impedances presented at each catheter sections are transmitted. This cycle is continuously repeated.

4. Phase and module impedance meter evaluation
System evaluation is implemented in three parts. First, the phase difference between I_{ref} and VAM is measured. In order to do this a phase shifter circuit is used, phase values are obtained and visualized in the PC by means of the software implemented in LabView and results are compared with others obtained using an digital oscilloscope. Second, the ability of the system to demodulate VAN and to detect signals peaks is evaluated. Besides, a frequency sweep of the modulating signal is carried out in order to assess the system bandwidth by measuring demodulated signal amplitude and frequency. Finally, VAM phase and module obtained, using the system, for known pattern impedances (parallel R-C circuits) are compared with the real values.

4.1. Phase measurement
The measurement is performed using a phase shifter circuit, that consist of a TL081 operational amplifier (Texas Instruments) and a R-C network, in order to obtained phase differences that goes from 2° to 150°. Phase values are obtained and visualized in the PC by means of the software implemented in LabView and they are compared with others obtained by means of observing Lissajous figures on a two channels digital oscilloscope. One channel is connected to the phase shifter input and to Iref(t), while the other is connected to phase shifter output Iref(t+phase) an to Vsen(t). Results are presented in figure 6.
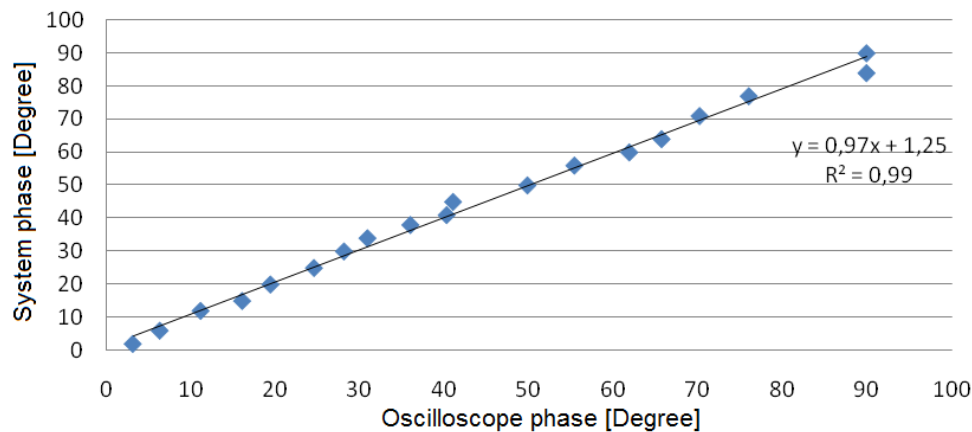
Figure 6. System vs Oscilloscope phase measurement.

The correlation value of 0.99 implies that the system has a linear response regarding to phase measurements made with the oscilloscope.

4.2. Module measurements

Measurement modules are implemented by means of an AM modulator and a phase shifter. Module measurements are carried out using an amplitude modulated signal which is generated with characteristics (amplitude and frequency) similar to those of biological signals. The AM signal is then processed and visualized on the PC. Besides, impedance frequency and module are measured with the system and with the oscilloscope are compared.

The AM modulator consists of an analog multiplier MC1495 (Motorola Semiconductor). Iref(t) is phase shifted and enters the modulator as a carrier signal. A signal generator GWINSTEK GFG – 8219 produces a signal which is similar to a biological one, this signal is used as modulating signal. A frequency sweep of the modulating signal is carried out, and the maximum and minimum frequency at which impedance module can be determined without information loss is determined. The relative error of the obtained module value with regard to the oscilloscope result is less than 6% when frequency goes from 1 to 90Hz; beyond this frequency, the relative error rises to values higher than 13%.

With respect to modulus measurement, minimum and maximum peaks that are measured by the system are similar to those which that are measured by oscilloscope. This situation does not change with frequency variations.

4.3. Bench test using known pattern impedances

Identical pattern impedances are connected to each one of the catheter sections and their phase and module are measured. This pattern impedances are adopted considering that biological conductance goes from $0.022\Omega^{-1}$ to $0.150\Omega^{-1}$, and that the phase shifts that result from myocardium capacity goes from 5° to 60°. Table 1 and table 2 show voltage values that represent pattern impedances phase and module measured at each catheter section. Measurements are performed using a 95mA current and the results are displayed on the PC using the software implemented in LabView.

The 0.99 and 0.91 correlations allow us to affirm that modules and phases are directly proportional to impedance modulus and phase respectively in each section of the catheter.

Table 1. Modules measurement for each one of the five sections

Pattern impedance Zp	Module [Ω]	Section 1 [V]	Section 2 [V]	Section 3 [V]	Section 4 [V]	Section 5 [V]
Zp1	18	1,86	1,86	1,86	1,86	1,86
Zp2	18	1,72	1,72	1,72	1,72	1,72
Zp3	47	4,90	4,90	4,90	4,90	4,90
Zp4	6,8	0,88	0,88	0,88	0,88	0,88
Zp5	33	2,43	2,43	2,43	2,43	2,43

Table 2. Phase measurement for each one of the five sections

Pattern impedance Zp	Phase [degree]	Section 1 [V]	Section 2 [V]	Section 3 [V]	Section 4 [V]	Section 5 [V]
Zp1	-16	-16	-15	-15	-16	-15
Zp2	-30	-31	-31	-31	-32	-32
Zp3	-10	-13	-13	-13	-13	-12
Zp4	-6	-7	-7	-7	-8	-7
Zp5	-49	-48	-48	-48	-49	-48

5. Discussion and conclusions

A FPGA based system that can measure impedance phase and module of each section of a conductance catheter system has been built. The functionality of the digital and analog stage has been evaluated with laboratory tests using 6.8Ω to 47Ω input impedances at each section. These impedances have 6º to 49º phases, although the system detects phases from 2º to 90º. The high correlation values - of 0.97 and 0.91- for phase measurements demonstrates the system linear response. It is concluded that the system is suitable for acquisition and sensing of impedance signals and for processing and calculating the module and phase of them.

For small angles (2° to 5°), the percentage error is greater because the measurement is near of the minimum value that can be measured. This behavior can be improved by increasing the number of samples needed to digitize the sensed input voltage. For low impedance modules, the percentage error is greater because the signal/noise ratio is increased. This behavior can be improved through high quality input digital filters.

A complete system evaluation requires impedance measurements (module and phase) from real biological impedances.

6. References

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