Design, Fabrication and Testing of Silicon-integrated Li-ion Secondary Micro Batteries with Side-by-Side Electrodes

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Abstract. This paper reports the design, fabrication, and testing of silicon-integrated lithium ion secondary micro batteries with a side-by-side electrode setup. Two cavities separated by a narrow silicon spacer served as a containment for the electrodes and were etched into <110>-Si by wet chemical etching using aqueous KOH solution. The etched silicon battery containment was passivated by a stress-compensated layer of SiO_2/Si_3N_4. Ti/Pt-current collectors were applied by E-beam evaporation and lift-off structuring. A volumetric dispenser served to fill the cavities with slurries of the active materials - lithium cobalt oxide ($LiCoO_2$) as the anode and graphite as the cathode material. Encapsulation, electrolyte filling, and electrochemical characterisation of the finished cells took place in an Ar-filled glove box. The fabricated batteries have shown a rate capability of up to 5C and a linear capacity loss rate of <1 % per cycle over 30 full-cycles. Battery containments with different cavity and spacer widths have been fabricated.

1. Introduction

The fabrication of silicon integrated batteries appears to be of interest for applications where a small volume, high capacity energy supply is needed. Examples are small energy autarkic sensors, e.g. implantable sensors for medical applications [1], or miniaturized sensor networks. Such applications cannot be supplied by state of the art solid state batteries due to their limited capacity per area [1].

Previously we have investigated the fabrication of Li-ion batteries with stacked electrodes, separated by a porous polymer separator [2]. In this study, a design with anode and cathode lying side by side, separated by a silicon spacer has been implemented. This design facilitates assembly and encapsulation considerably since no polymer separator is needed and both electrodes can be contacted from downside. The fabricated structures could also be used in materials research, e.g. for high-throughput screening and in-operando electrode surface studies by applying different lid materials.

2. Design

The investigated battery design with a side-by-side electrode setup implies the lithium ions moving laterally from one electrode to the other, crossing a silicon spacer of reduced surface height with respect to the wafer surface. This is expected to result in a different dependency between geometry

and impedance of the cell as compared to a conventional setup with electrodes stacked on top of each other and the lithium ions moving back and forth between the electrodes perpendicularly to the electrode surface (Fig.1).

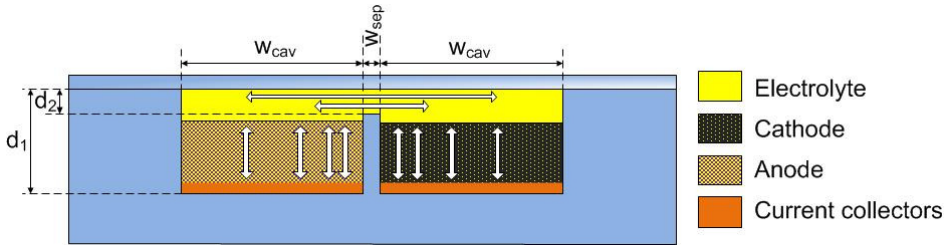

Fig.1: Schematic profile of a battery with side-by-side electrode setup
(arrows indicate paths of Li-ion movement)

We chose to fabricate structures as shown in Fig. 1 from a <110>-silicon substrate by applying two steps of wet chemical etching. The <110>-orientation of the wafer allows for the fabrication of long and narrow cavities bordered by {111} sidewalls that are vertical at the long sides and offer a slope of 35° at the front sides. Such geometry ensures a good utilization of area (i.e. a high specific capacity) as well as an easy patterning of the current collectors leads via the front side slopes. In the first etch step, two cavities separated by a Si-spacer of full height should be formed, whereas the second etch step should give rise to a clearance above the Si-spacer. The unmasked exposure of convex edges to KOH etch solution is known to result in a rounding of these edges. This effect was expected to be of benefit considering cell impedance because sloped edges diminish the dimension of the very thin electrolyte layer above the Si-spacer.

To confirm the feasibility of our concept, we simulated the etching process with the aid of the software ACES (Anisotropic Crystalline Etching Simulation) [3]. ACES works on an algorithm based on the Continuous Cellular Automata method and is available for free download in the internet [4]. The anisotropic ratio between {100} and {110} crystal plane etch rates was adapted to comply with our experimental conditions (33wt% KOH in pure water, 80°C) using the rate law proposed by Seidel et al. [5]. The etch rate of the {311}-planes was set to equal that of the {110} plane as proposed by ACES and the data given in literature [6]. This resulted in etch rate ratios of 1:1.535:1.535:0 for {100}:{110}:{311}:{111}, respectively.

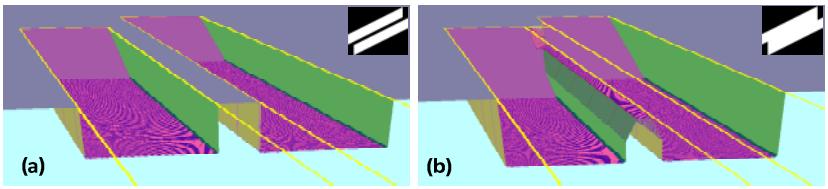

Fig. 2: ACES simulation results for battery containments with w_{cav} = 300 µm and w_{sep} = 100 µm
a) after 1st etch step b) after 2nd etch step (yellow lines: mask outline; insets: mask shape)

The simulation results confirm the build-up of slanted edges during unmasked exposure of the Si-spacer to the etch solution. The slants are forming an angle of 29.5° with the next {111} plane and correspond to the uncovering of {311} crystal planes.

3. Fabrication

Fig. 2 gives a short survey on the fabrication process flow. The starting substrate is a p(B)-doped CZ-grown <110>-Si wafer with a resistivity of 1-30 Ohm cm. In a first step, the exact crystal orientation of the wafer is determined and alignment marks are applied by deep reactive ion etching (DRIE, not shown in Fig. 2). A 1 µm thick oxide layer is grown by wet thermal oxidation and

structured using buffered HF solution (**B**, Fig. 2). Then a thin layer of silicon nitride (Si_3N_4) is deposited by low pressure chemical vapour deposition (LPCVD) and structured selectively by DRIE (step C, Fig. 2). The Si_3N_4 bar for structuring the Si-spacer is deposited directly on the silicon surface. Doing so allows for a two-step wet etch process without deposition or growth of another masking layer for the second step. This helps to prevent contamination of deposition equipment by metal ions.

During the first KOH etch step, two 200 µm deep side-by-side cavities separated by a narrow spacer are formed. After this, the Si_3N_4 masking layer is removed by DRIE (**D**, Fig. 2). A second KOH etch step provides for a further 100 µm deepening of both, the cavities and the spacer (**E**, Fig. 2).

The remaining oxide mask is removed prior to passivation of the substrate by the growth of 100 nm of thermal SiO_2 and the deposition of 180 nm of Si_3N_4 by LPCVD (**F**, Fig. 3). The thickness of the individual layers is adapted to compensate for the CTE mismatch between the different materials. Deposition and patterning of Ti/Pt-current collectors by E-beam evaporation and lift-off conclude the fabrication process of the bottom substrate of the battery housing (**G**, Fig.3).

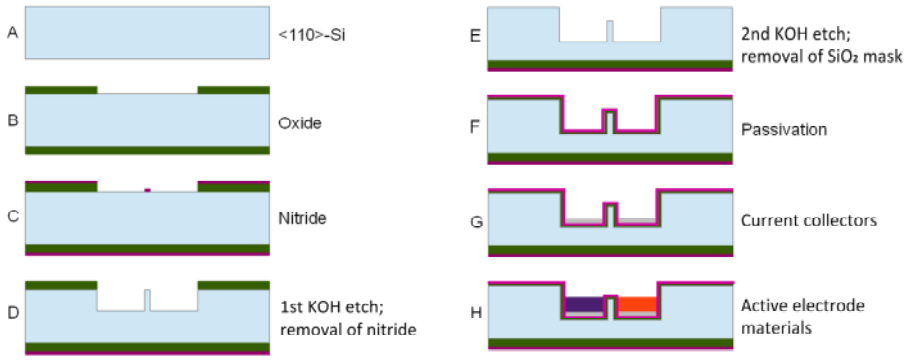

Fig. 3: Main processing steps for the fabrication of the battery containment

Fig. 4 shows cross-section polishes of the etched battery containments. Featuring the simulated effects, the etched substrates basically confirm simulation. There are, however, differences in geometry at the separator region. Firstly, the separator is slightly narrower than simulated due to an undercut at the nitride-on-silicon masking bar. Secondly, the slopes at the separator edges form angles different from 29.5° with the vertical {111} walls. In fig. 4b, also a rounding of the separator edges can be observed. The authors believe these effects to be caused by a step flow etch mechanism as proposed by Horn et al [7] rather than by the etching of high-index crystal planes. Fig. 4d shows the surface quality of the sloped edges of a separator.

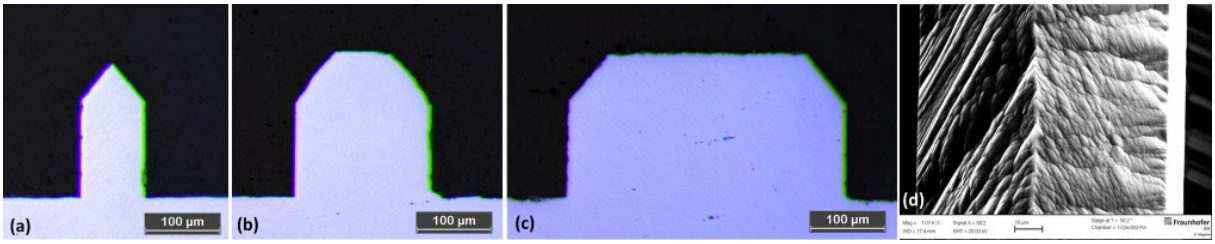

Fig. 4: Cross-section polishes of battery containments with different spacer widths
a) 100 µm b) 200 µm c) 400 µm d) surface of the sloped edges of a 100 µm spacer

3.1. Deposition of active materials and assembly

Prior to the deposition of the active materials, a slurry of conductive carbon, water, and polyvinylpyrrolidone (PVP) as a binder was dispensed on top of the current collectors. Having a final thickness of some 30 µm after solvent removal, this coating provides for a better contact between

current collectors and active electrode materials. The active materials for cathode and anode were prepared form slurries of commercially available powders (lithium cobalt oxide, LCO, for the cathode and graphite for the anode, both from MTI corp. [8]), polyvinylidene difluoride (PVDF) as a binder, and N-methyl-2-pyrrolidone (NMP) as a solvent [9]. The slurries were applied to the cavities by volumetric micro dispensing (Ultimus IV, Nordson) and the solvent removed by appropriate heat treatment. We observed a good separation between the resulting electrodes by measurement of isolation resistance and SEM investigation (Fig. 5a). The filling process provides for an excess capacity on the anode side ranging from 10 to 45% of the nominal capacity of the cathode (Fig. 5b).

The chips with the active electrodes were introduced into an Ar-filled glove box. Hereafter, a heating step of 12 h at 80°C and under vacuum was applied to allow for all materials to dry completely. A glass lid with holes for the deposition of electrolyte was provided with a filled, UV-curable epoxy resin by dispensing. After alignment, lid and bottom substrate were attached to each other and the resin cured by UV-exposure at room temperature (Fig. 5c). The cavities were evacuated and liquid electrolyte was filled in using a home-made holder with a standard GC-septum and a syringe. We applied 1M $LiPF_6$ dissolved in a mixture of ethylene carbonate and dimethylcarbonate (EC:DMC, 1:1wt%) as the electrolyte. To allow for the removal of gas generated during formation, the holes for electrolyte filling were finally sealed not until after formation of the batteries.

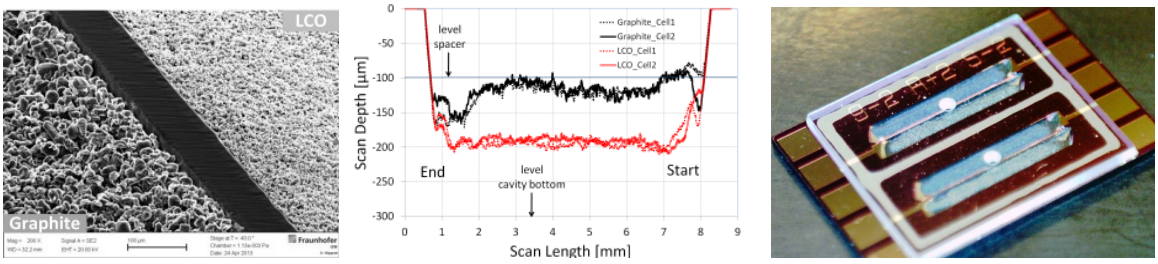

Fig.5 a) Separator region after application of electrodes (w_{sep}=200µm; final electrode distance 75 µm)
b) Height profiles of different cavities filled with active material (black: graphite, red: LCO)
c) Photography of a chip with two sealed cells (chip size: 15x10 mm)

4. Testing

4.1. Cycling behaviour

The fabricated batteries were tested using a multichannel battery test system (CTS-LAB, Basytech GmbH). To investigate the cycling behavior, we applied CC-CV charge and CC discharge steps between 3 and 4.1 V at a rate of 0.1C, respectively. Linear capacity loss rates ranging from 0.5 to 1% per cycle were observed over 30 cycles (fig. 6a).

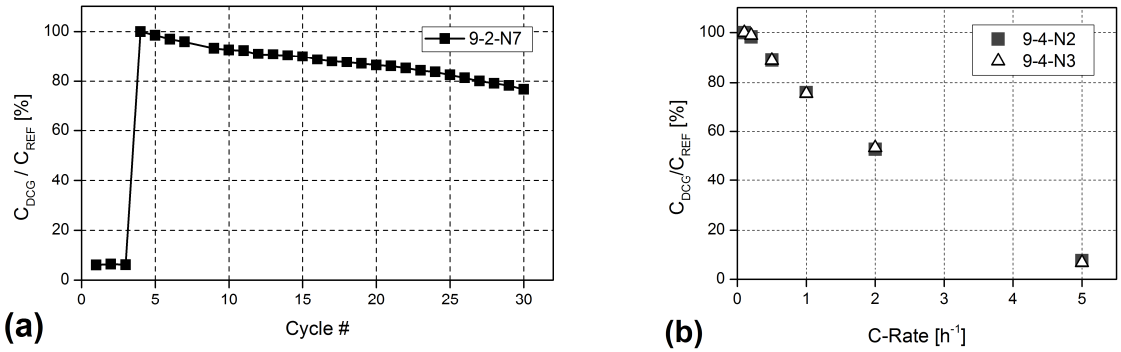

Fig. 6a) Discharge capacity loss over 30 cycles (cycles 1 to 3: formation)
b) Rate capability of two different cells (both w_{sep}=400 µm, w_{cav}=900 µm)

4.2. Rate capability

Different batteries have been tested to determine their rate capability. To do so, we cycled the cells between 3 and 4.1 V with CC/CV-charge steps at a rate of 0.2C and increasing discharge rates ranging from 0.1 to 5 C. The reference capacity for calculating the C-rates was determined during a first cycle at a discharge rate of 0.1C. At this rate the value basically equaled the nominal capacity of the material (145 mAh/g) as given by the supplier. For each discharge rate two complete cycles were run through. Due to the impedance of the cells, only part of the nominal capacity is extractable at higher C-rates. The capacity was found to drop linearly with the C-rate (fig. 6b). We observed a reproducible rate capability behavior for cells of the same geometry and on the same chip.

5. Conclusion

Lithium ion secondary batteries with a side-by-side electrode setup have been fabricated by the anisotropic wet etching of <110>-silicon, the automated dispensing of electrodes from slurries, and room temperature adhesive bonding. First cycling tests have shown that the concept is feasible and results were found to be reproducible for different cells with the same set-up.

The influence of the mask geometry on the final shape of the Si-spacer was investigated. For realizing designs with spacers narrower than 175 µm, the duration of each of the two KOH-etch steps must be adapted in compliance with the geometry-dependent etch behavior at the separator tip.

For cells with a side-by-side electrode setup the capacity drop with discharge rate is more pronounced than for conventional cells with stacked electrodes due to the higher impedance. However, the extractable discharge capacity during pulse load tests is expected to be higher than observed during continuous CC-discharge due to relaxation effects. As the supply of sensors coupled to radio modules is considered an important application for Si-integrated micro batteries, the characterization of the discharge performance of the cells during pulse load tests will be subject of upcoming investigations. To gain insight into the relation between cell set-up and impedance, a more comprehensive testing of cells with different geometry or differently applied electrodes is necessary. Here, the measurement and analysis of impedance spectra at different operation points is considered to be of value to optimize cell performance and intended in the future.

References

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