

Miniature fuel cell with monolithically fabricated Si electrodes - Alloy catalyst formation -

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Abstract. A novel Pd-Pt catalyst formation process was proposed for reduction of Pt usage. In our miniature fuel cells, porous Pt was used as the catalyst, and the Pt usage was quite high. To reduce the Pt usage, we have attempted to deposit Pt on porous Pd by galvanic replacement, and relatively large output was demonstrated. In this study, in order to reduce more Pt usage and explore the alloy catalyst formation process, atomic layer deposition by UPD-SLRR (Under Potential Deposition – Surface Limited Redox Replacement) was applied to the Pd-Pt catalyst formation. The new process was verified at each process steps by EDS elemental analysis, and the expected spectra were obtained. Prototype cells were constructed by the new process, and cell output was raised to 420mW/cm² by the Pd-Pt catalyst from 125mW/cm² with Pd catalyst.

1. Introduction

Miniature fuel cells get a lot of attention for mobile devices, and we proposed a Si based fuel cell that has both fuel channel and catalyst layer on a Si substrate as shown in figure 1. Recent reports at Power MEMSs[1,2] showed that good performance was available by our miniature fuel cells. However, in our prototypes, porous Pt was used as a catalyst and the Pt usage was quite high. We have discussed Pd-Pt alloy catalyst for reduction of the Pt usage in our miniature fuel cells[3]. In the study, we developed the porous Pd layer formation process. Then, Pt was deposited on the porous Pd layer by galvanic replacement reaction, and estimated Pt usage was reduced to 0.16mg/cm². Some prototype fuel cells were constructed, and more than 400mW/cm² peak output was obtained.

In the previous study, the reduction of Pt was successfully demonstrated. However, probably, the Pt was deposited disorderly with the galvanic replacement reaction. In order to achieve further efficient Pt use, controllable atomic layer deposition of Pt on the porous Pd is desired. Besides, alloy catalysts are useful for not only Pt reduction, but application of various fuels, such as Pt-Ru alloy catalyst for methanol. Such alloy catalysts are also useful for biomass-derived hydrogen, because it tends to contain high carbon monoxide.



In order to reduce more Pt usage and explore the alloy catalyst formation process, atomic layer deposition by UPD-SLRR (Under Potential Deposition – Surface Limited Redox Replacement) [4,5] was applied to the Pd-Pt catalyst formation as shown in figure 2.

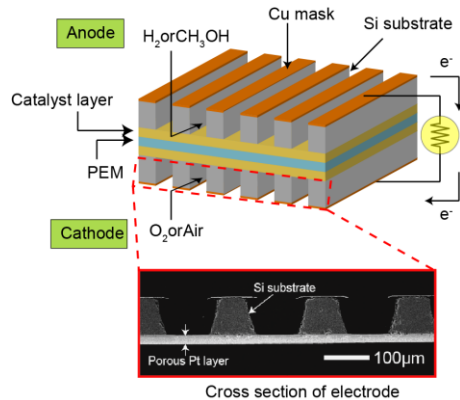


Figure 1. Schematic view of the miniature fuel cell and the cross section of monolithic fuel cell Si electrodes.

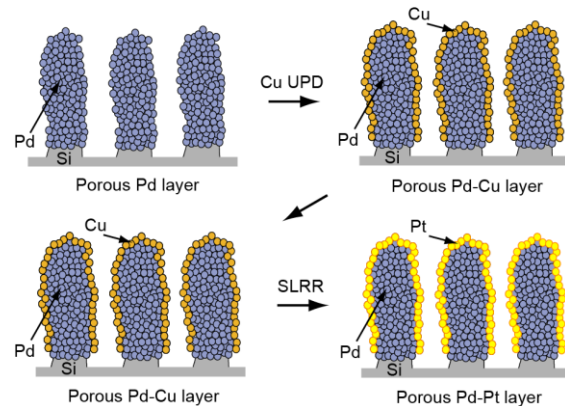


Figure 2. Strategy for atomic layer Pt deposition on porous Pd by UPD-SLRR.

2. Fabrication process

2.1. Si electrode with porous Pd

Figure 3 illustrates the fabrication process of the Si electrode. The electrode chip has quite simple structure, in which a catalyst layer and fuel channels are monolithically fabricated on a Si wafer. The silicon wafers used in this work were N-type (Resistivity 0.004-0.006 Ohm-cm), (100) oriented, double side mirror polished 100μm thick ones. After removing oxide by HF, Cu thin film is deposited on the Si wafer by sputtering. Using usual photolithographic patterning with photoresist and wet etching, fuel channel mask for plasma etching is made with the Cu thin film. Porous Si layer is formed on the opposite side of the Si wafer by anodization in an electrolyte containing HF. The porous Si layer is subsequently immersed into a Pd plating bath, and porous Pd layer is obtained. Process condition for the porous Pd layer formation was reported elsewhere [3]. Fuel channels are opened by applying plasma etching on the backside of the porous Pd layer with the copper thin film mask. The reaction area was 1mm². Conventional parallel plate reactive ion etching system (Samco RIE-10N, Japan) is used and 18sccm of SF₆ and 4sccm of O₂ gases are supplied for the etching. In this plasma etching process, porous Pd layer is supposed to work as a stopping layer of the etching, because the etching rate is low at the porous metal layer, and through-chip porous Pd layer can be relatively easily fabricated. In this way, monolithic Si based electrodes were prepared. Some text.

2.2. UPD-SLRR for Pt deposition on Pd

Process conditions for the UPD-SLRR Pd-Pt catalyst layer formation is shown in Table 1. Dimension of the porous Pd layer formed on a Si chip was about 1 cm in diameter and 10μm in thickness. In the Cu UPD process, as a reference electrode, Cu wire was employed, and Pt wire was used as a counter electrode. An electrolyte solution of 0.1M H₂SO₄+0.1M CuSO₄ was prepared for the Cu UPD, and the solution was bubbled with nitrogen gas for 30 min prior to the experiment to eliminate dissolved oxygen and carbon dioxide. Before the UPD process, the chip with the porous Pd layer was cleaned by a 1M H₂SO₄ solution. Then, the chip was immersed into the electrolyte solution in a vessel filled with nitrogen gas. The electrode potential was varied to determine the appropriate electrode potential for the UPD process.

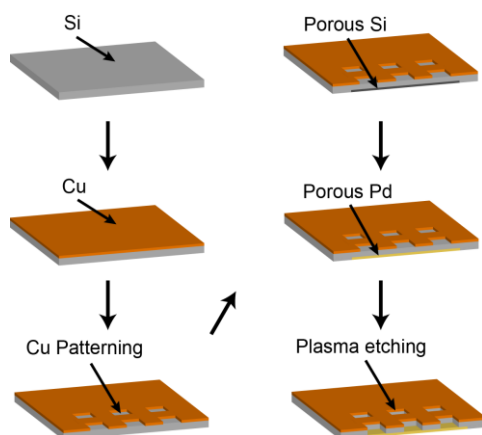


Figure 3. Fabrication process of the Si electrode.

Table 1. Condition for atomic layer Pt deposition on porous Pd layer by UPD-SLRR.

| Copper UPD for the porous Pd layer | |
|--|---|
| Working Electrode | Chip formed porous Pd layer |
| Reference Electrode | Cu wire |
| Counter Electrode | Pt wire |
| Composition of solution | 0.1M H ₂ SO ₄ + 0.1M CuSO ₄ ·5H ₂ O |
| Sampling frequency [Hz] | 40 |
| Scan rate [mV/s] | 5 |
| Scan range [mV] | From 400mV to 0 mV |
| SLRR for the after UPD processed porous Pd layer | |
| Working Electrode | Copper UPD processed chip |
| Reference Electrode | Pt wire |
| Counter Electrode | Pt wire |
| Composition of solution | 2mM H ₂ PtCl ₆ + 0.1M H ₂ SO ₄ |
| Potential [mV] | -273 |
| Plating time [min] | 1 |

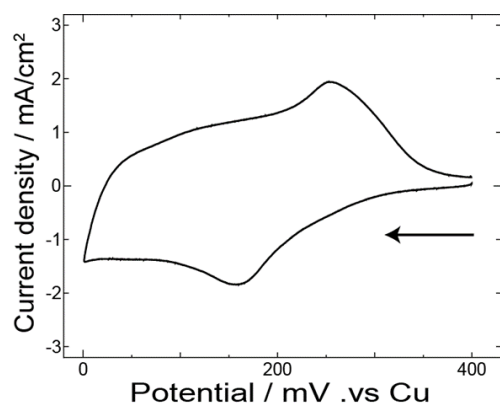


Figure 4. Cyclic voltammogram for Cu UPD on the porous Pd layer.

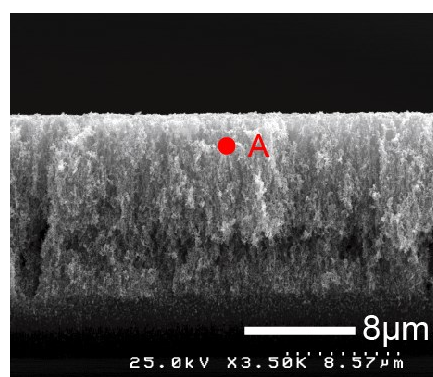


Figure 5. Typical cross sectional SEM image of the porous Pd-Pt catalyst layer. Point A shows the location for the EDS analyses.

After the Cu UPD process, the porous Pd chip was moved to the SLRR process. Since a replacement reaction of Pd to Pt occurs automatically in a Pt plating bath, the electrode potential of porous Pd layer was shifted to cathodic side, and the chip was immersed into the 2mM Pt plating bath for one minute. All electrochemical experiments were controlled by a potentiostat (Hokuto Denko, HA150G) with in house software.

2.3. Prototype assembly

A thin gold film was deposited by sputtering on the edge of the catalyst layer to have electrical contact to the low resistive Si substrate, because direct electrical contact between the porous catalyst layer and Si substrate is poor. Then, two Si electrodes are hot-pressed onto either side of PEM sheets. In order to obtain good contact between the catalyst layer and PEM, the double PEM treatment [6] was employed.

3. Results and discussion

3.1. Cu UPD

Figure 4 shows the cyclic voltammogram of the porous Pd in the Cu UPD bath. Current peak was observed at +160 mV vs. Cu. The electrode potential at the peak was positive to the equilibrium

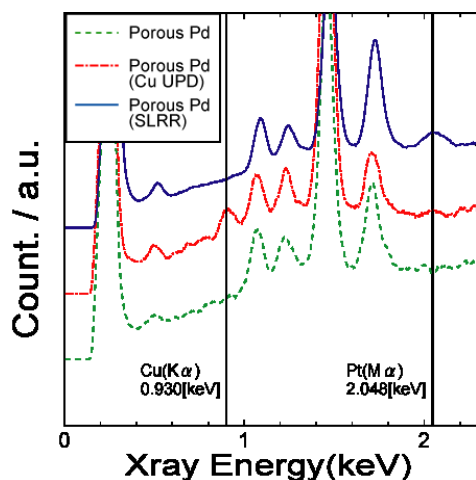


Figure 6. EDS spectra before and after the Cu UPD and after SLRR.

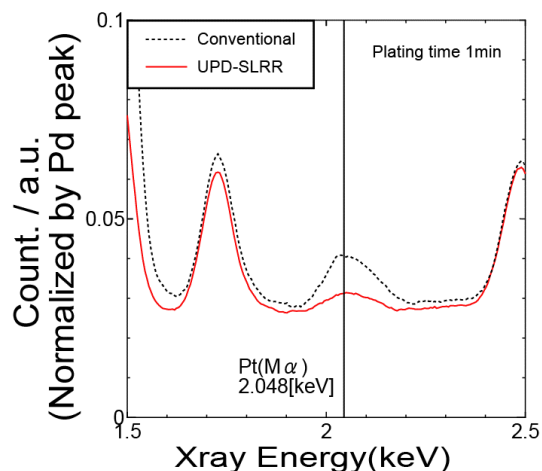


Figure 7. Comparison of the Pt usage between conventional and novel catalyst.

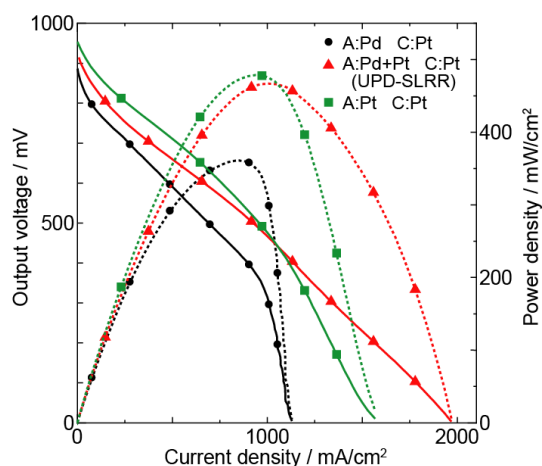


Figure 8. Polarization curve of prototype cells used Pd-Pt as anode at 313K.

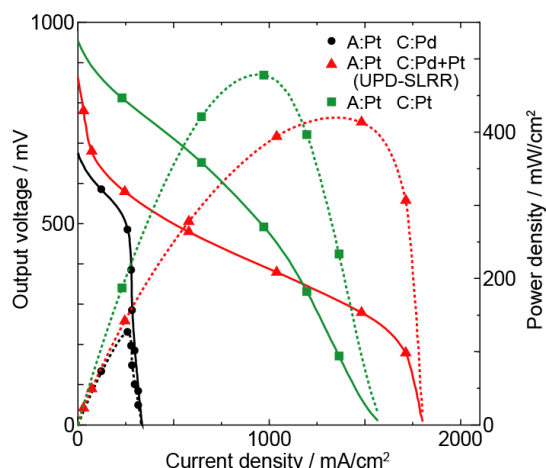


Figure 9. Polarization curve of prototype cells used Pd-Pt as cathode at 313K.

potential, and we assumed that the current peak was caused by the UPD. We decided to perform the UPD process by following potential modulation. The electrode potential was swept from 400mV to 50mV, and was kept constant for 1min until the electric current became enough small.

3.2. EDS elemental analyses

Figure 5 shows the typical cross sectional image of the porous Pd-Pt layer, and EDS elemental analysis was performed around the point A. Figure 6 shows the EDS spectra. Green line shows the spectrum of porous Pd before the Cu UPD process. Red line shows the spectrum after the Cu UPD. Blue line shows the spectrum after the SLRR. As we expected, small Cu peak appeared after the UPD process and disappeared after the SLRR reaction. After the SLRR process, small Pt peak was observed. These results supports that the expected UPD-SLRR reaction occurred. Figure 7 shows the comparison between present Pd-Pt(UPD-SLRR) catalyst and previously proposed Pd-Pt catalyst, in which Pt was deposited by just galvanic replacement reaction for 1 min. Dashed line shows the spectrum of Pd-Pt prepared by previously proposed process, while red line shows the spectrum of Pd-Pt(UPD-SLRR). It

was found that the Pt signal was smaller in the novel UPD-SLRR process than the one observed in previous process. It can be said that Pt deposition was successfully limited by UPD-SLRR.

3.3. Power Generation Test

Finally, prototype cells were produced with the novel UPD-SLRR process, and power generation was tested. Prototype cells were set into the aluminium casing at 313K in a temperature controllable chamber. Pure hydrogen and oxygen were supplied to anode and cathode respectively. Three catalysts, Pt, Pd and Pd-Pt(UPD-SLRR), were prepared. Figures 8 and 9 show the polarization curves. Figure 8 shows the impact of anode catalysts, while figure 9 shows the cathode impact. In both figures, though Pt catalyst showed the best results, Pd-Pt(UPD-SLRR) showed comparable results to pure Pt catalyst. Generally, cathode (oxygen side) needs higher catalytic activity, and the catalyst performance can be demonstrated. In figure 9, Pd catalyst showed only 125mW/cm², while Pd-Pt(UPD-SLRR) showed 420mW/cm². Obvious power increase was observed with Pd-Pt(UPD-SLRR) from simple Pd catalyst, and it was found that Pt deposition by UPD-SLRR was effective in catalyst improvement and Pt usage reduction.

4. Conclusion

In this study, we attempted to deposit Pt atomic layer on porous Pd by UPD-SLRR. From the results of CV and EDS elemental analyses, it was assumed that Pt atomic layer deposition was successfully realized. It was also suggested that the novel process showed more Pt usage reduction compared to previously proposed simple galvanic replacement reaction process. Power generation was examined, and prototype cell with UPD-SLRR Pt showed comparable performance to the simple Pt catalysts, though the Pt usage was significantly reduced. The new process showed promising results, and further study to improve catalyst performance will be performed.

References

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