GaN MOSFET with Boron Trichloride-Based Dry Recess Process

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Abstract The dry recessed-gate GaN metal-oxide-semiconductor field-effect transistors (MOSFETs) on AlGaN/GaN heterostructure using boron trichloride (BCl_3) as etching gas were fabricated and characterized. Etching with different etching power was conducted. Devices with silicon tetrachloride ($SiCl_4$) etching gas were also prepared for comparison. Field-effect mobility and interface state density were extracted from current-voltage (*I-V*) characteristics. GaN MOSFETs on AlGaN/GaN heterostructure with BCl_3 based dry recess achieved a high maximum electron mobility of 141.5 $cm^2V^{-1}s^{-1}$ and a low interface state density.

1. Introduction

Gallium nitride (GaN) has attracted much attention in the field of high-power and high-efficiency applications due to its remarkable material properties such as wide bandgap, high breakdown field, and high electron saturation velocity. For power electronics application, the enhancement-mode (E-mode) plays a vital role of realizing safe operation and reducing power consumption owing to the normally-off operation [1-3]. In order to realize E-mode GaN MOSFET, source and drain ohmic contact must be primarily produced. To avoid activation at high temperature required by the ion-implanted source and drain regions, AlGaN/GaN heterostructure with high electron density of polarization-induced two-dimensional electron gas (2DEG) could be utilized as source and drain contacts. To accomplish this structure, dry recess process is necessary to remove the AlGaN layer for forming the channel region in the GaN layer. The avoidance of etching damage is required to obtain a high-quality channel with high carrier mobility and low interface states. Inductively coupled plasma (ICP) system is used to etch the gate. Low ICP and bias power could decrease the etching rate which is benefit to reduce etching damage [4-6]. Low power might also get an irregular recess profile and even failure in the MOSFETs operation. In our previous work [4, 7], we achieved a precise control of ICP etching rate of 1.2 nm/min and determined the optimum ICP condition of GaN MOSFETs on AlGaN/GaN heterostructure with the etching gas of $SiCl_4$. However, the devices etched with $SiCl_4$ gas had a negative threshold voltage due to the possible silicon (Si) contamination.

In this paper, we tried to use BCl_3 instead of $SiCl_4$ as the gate recess etching gas in order to reduce the influence of Si contamination on threshold voltage. Then we discussed the influence of etching gas and conditions on the performance of dry recessed-gate GaN MOSFETs on AlGaN/GaN hetero-structure, which were characterized by extracting the field-effect mobility and interface state density.

2. Experiments

The device structure is a ring-type MOSFET on AlGaN/GaN heterostructure grown on a sapphire substrate, as shown in Fig. 1. The epitaxial structure includes a buffer layer, a 2 μm i-GaN layer, a 20 nm n-AlGaN layer, and a 10 nm n-GaN layer. The composition ratio of the aluminum in AlGaN layer is 25%. The n-AlGaN layer and n-GaN layer are doped with Si of a concentration of 1.0×10^{19} cm^{-3}. The sheet resistance of the wafer is around 500 Ω/□. To form the MOSFET structure, a 2DEG layer is used as the ohmic contact layer, and a surface etched i-GaN layer is used as the channel layer.

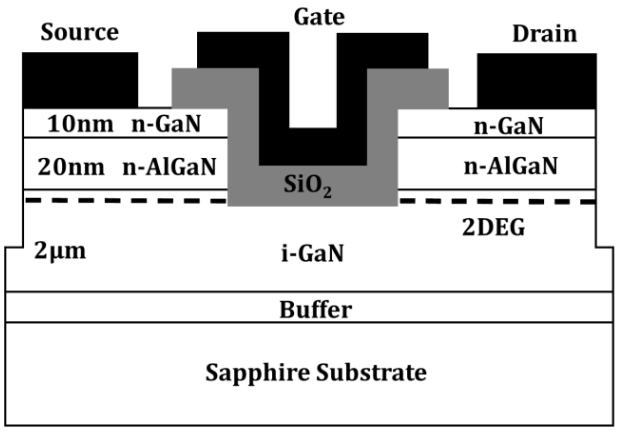

Fig. 1 Schematic cross section of ring-type GaN MOSFET on AlGaN/GaN heterostructure

The device fabrication process was based upon standard photolithography and lift-off technologies. The SiO_2 film of about 500 nm thickness deposited by tetraethylorthosilicate (TEOS) plasma enhanced chemical vapor deposition (PECVD) was used as the etching mask. The gate recess was conducted utilizing ICP system with BCl_3 and $SiCl_4$ gas. The etching conditions of five samples can be divided into three kinds (listed in Table 1).

(1) Sample No. 1 and No. 2 were done with $SiCl_4$ gas, ICP power of 100 W and 50 W, respectively, bias power of 20 W, $SiCl_4$ gas flow rate of 3 sccm and working chamber pressure of 0.25 Pa (termed as: No. 1 $SiCl_4$ 100W/20W and No. 2 $SiCl_4$ 50W/20W, respectively). The etching rates of these two samples were about 1.2 nm/min and 1.0 nm/min, respectively.

(2) Sample No. 3 and No. 4 were etched with mixed BCl_3/Cl_2 gas (20/20 sccm), ICP power of 100 W, bias power of 25 W and at a working chamber pressure of 0.6 Pa. The etching depths were 110 nm and 60 nm respectively (termed as: No. 3 BCl_3/Cl_2, 110 nm and No. 4 BCl_3/Cl_2, 60 nm, respectively), and the etching rates were about 30 nm/min.

(3) Sample No. 5 (termed as: No. 5 $SiCl_4$+Cl_2) was etched by two steps, and the average etching rate was about 20 nm/min. The first step was done by $SiCl_4$ gas with a flow rate of 4 sccm, ICP power of 50 W, bias power of 100 W and at a working chamber pressure of 0.25 Pa. The second step was done by Cl_2 gas with a flow rate of 4 sccm, ICP power of 50 W, bias power of 50 W and at a working chamber pressure of 0.25 Pa.

During the etching processes, the sample stage was cooled by helium gas to keep at the room temperature.

After these dry etching processes, the samples were immersed in HNO_3: BHF = 1:1 solution to remove the possible contamination of Si on the etched surface. As the gate insulator, a 103.5-nm-thick SiO_2 layer was then deposited by PECVD (SAMCO PD-220LC) with silane-based source, followed by annealing at 1000℃ for 10 min in N_2 ambient. After the gate insulator patterning, the source and drain ohmic contacts were formed using Ti/Al/Ti/Au (50/200/40/40 nm) annealed at 850ºC for 1 min in N_2 ambient. Transmission line model (TLM) measurement showed that the contact resistance was approximately 0.15-0.36 Ωmm. A Ni/Au (70/30 nm) bi-layer was deposited as the gate metal.

Table 1 Dry etching process conditions of all the samples

No.	Term	ICP Power (W)	Bias Power (W)	Gas	Flow Rate (sccm)	Chamber Pressure (Pa)	Etching Rate (nm/min)	Recess Depth (nm)
1	$SiCl_4$ 100W/20W	100	20	$SiCl_4$	3	0.25	1.2	60
2	$SiCl_4$ 50W/20W	50	20	$SiCl_4$	3	0.25	1.0	60
3	BCl_3/Cl_2, 60 nm	100	25	BCl_3/Cl_2	20/20	0.6	30	60
4	BCl_3/Cl_2, 110 nm	100	25	BCl_3/Cl_2	20/20	0.6	30	110
5	$SiCl_4$+Cl_2	50	100	$SiCl_4$	4	0.25	20	100
		50	50	Cl_2	4	0.25		

3. Results and Discussion

The device used for evaluation is long channel ring-type MOSFET. It has a channel length L of 94 μm and an effective channel width W of 819 μm which was calculated from

$$W = \frac{2\pi L}{\ln r_{out} - \ln r_{in}},$$

where r_{out} and r_{in} is the outer and inner radius. For all the samples, the gate leakage currents were below 10^{-9} A with gate voltage from -10 V to 10 V and drain voltage of 0.1 V, as shown in Fig. 2. In particular, gate leakage is restrained even at a positive gate bias, which is beneficial to achieve the E-mode operation. To extract the capacitance of gate insulator, measurement of *C-V* characteristics was performed under frequency of 100 kHz and with gate voltage from -10 to 15 V. From Fig. 3, we can observe the hysteresis and the negative threshold voltage from -5.5 to -3.5 V. The difference of threshold voltage by different etching gas is not clear. One reason is the possible positive charges existing in the gate insulator layer leading to a negative shift on the threshold voltage [8], and the other reason may be from the GaN channel layer of this work. Through the evaluation of device isolation, we confirmed that the isolation region had a large leakage current indicating that the GaN buffer layer is slight n-type rather than semi-insulating type.

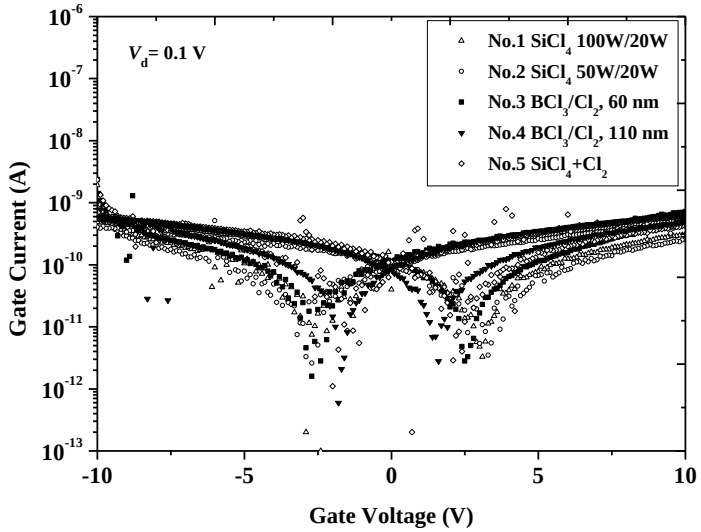

Fig. 2 Gate leakage current of GaN MOSFETs of all the samples with gate voltage from -10 to 10 V.

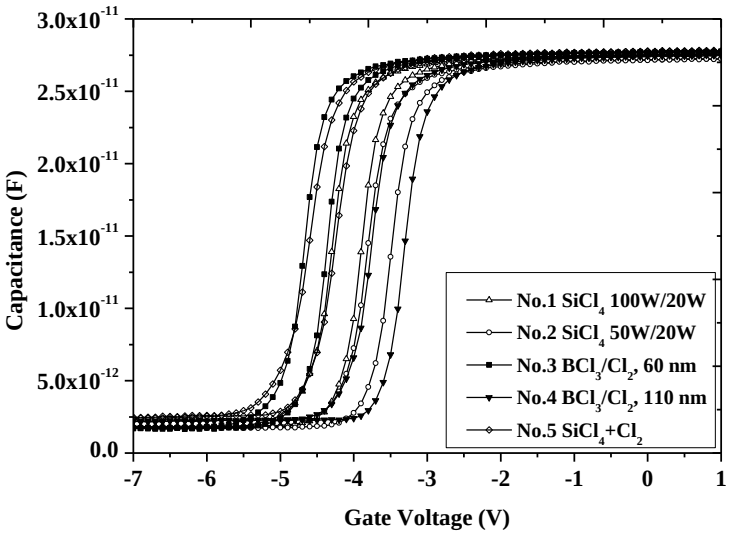

Fig. 3 The segment of *C-V* characteristics curve of GaN MOSFETs of all the samples with gate voltage from -7 to 1 V.

Figure 4 shows the I_d-V_d characteristics of the device etched with BCl_3 gas and low etching rate. Drain voltages range from 0 to 20 V and gate voltage range from 10 to -3 V. Device operation up to gate voltage of 10 V was confirmed. A gate capacitance-transconductance method was adopted to determine the electron field-effect mobility. According to the basis of the gradual channel approximation of MOSFETs, field-effect mobility could be calculated as

$$\mu_{FE} = \frac{G_M L}{C_{OX} W V_d},$$

where L is the gate length, C_{OX} is the oxide capacitance per unit area, and G_M is the transconductance. The field-effect mobility of all the samples is showed in Fig. 5. The electron mobility of two devices etched with BCl_3 gas are 141.5 and 136.0 $cm^2V^{-1}s^{-1}$, respectively, as listed in Table 2. The field-effect mobility of the device with the recess depth of 110 nm is only slightly lower than that of the device with the recess depth of 60 nm. Although the etching condition of these two samples was same, but a larger depth meant longer etching time and produced more surface contamination, which would degrade the mobility. However, for the device No. 5 etched with $SiCl_4$ and Cl_2 gas, the field-effect mobility decreased sharply, probably because of much etching surface damage caused by high bias power. The mobility is almost the same for the devices with 20 W bias power and different ICP power, implying that the mobility is more sensitive to the bias power instead of the ICP power. In reference [7], we have reported the influence of etching conditions on the recess profiles, mobility and interface state density for devices with ICP power from 50 to 100 W, bias power from 20 to 60 W and the etching mask of SiO_2. It showed that higher bias power would bring more interface states and lower mobility. It was considered to be due to the much serious surface damage and silicon contamination occurring at higher bias power.

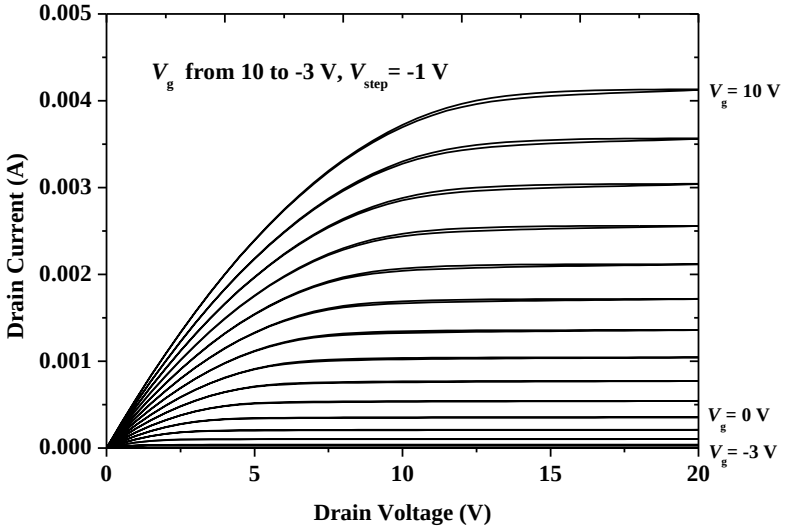

Fig. 4 I_d-V_d characteristics of the device etched with BCl_3 gas and the recess depth of 60 nm.

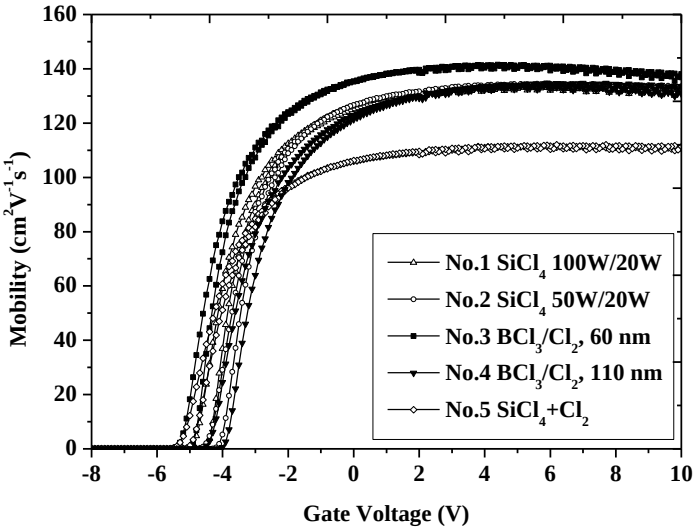

Fig. 5 The field-effect mobility of GaN MOSFETs of all the samples.

Table 2 The measured maximum field-effect mobility and interface state density of all the samples

No	Term	Average of C_{ox} (10^{-8} Fcm^{-2})	Field-effect Mobility μ_{FE} ($cm^2V^{-1}s^{-1}$)		Subthreshold Swing S (mV/dec)		Interface State Density D_{it} (10^{11} $cm^{-2}eV^{-1}$)	
			Forward	Reverse	Forward	Reverse	Forward	Reverse
1	$SiCl_4$ 100W/20W	3.45	133.3	133.9	141.5	137.6	2.96	2.82
2	$SiCl_4$ 50W/20W	3.41	133.9	134.5	177.1	154.9	4.21	3.41
3	BCl_3/Cl_2, 60 nm	3.47	141.1	141.5	112.1	139.7	1.91	2.91
4	BCl_3/Cl_2, 110 nm	3.44	133.7	136.0	169.4	149.4	3.97	3.25
5	$SiCl_4+Cl_2$	3.48	111.6	112.0	138.3	176.0	2.87	4.25

The equivalent circuit of the MOS structure can be presented as the oxide capacitance C_{OX} connected in series with a parallel connection of the depletion capacitance C_D and the interface-related capacitance C_{it}. In this case, based on the definition, the subthreshold swing S could be expressed as

$$S = \frac{dV_g}{d\log I_{ds}} = (\ln 10)\left(\frac{kT}{q}\right)\left(1+\frac{C_D}{C_{OX}}+\frac{C_{it}}{C_{OX}}\right),$$

where k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge. Figure 6 shows the I_d-V_g characteristics of the devices in the subthreshold region. Considering the depletion capacitance is zero, C_{it} can be calculated from the extracted subthreshold swing S. The interface states density D_{it} can then be calculated from C_{it}. The device etched with BCl_3 gas and the recess depth of 60 nm obtained a low interface state density, as listed in Table 2.

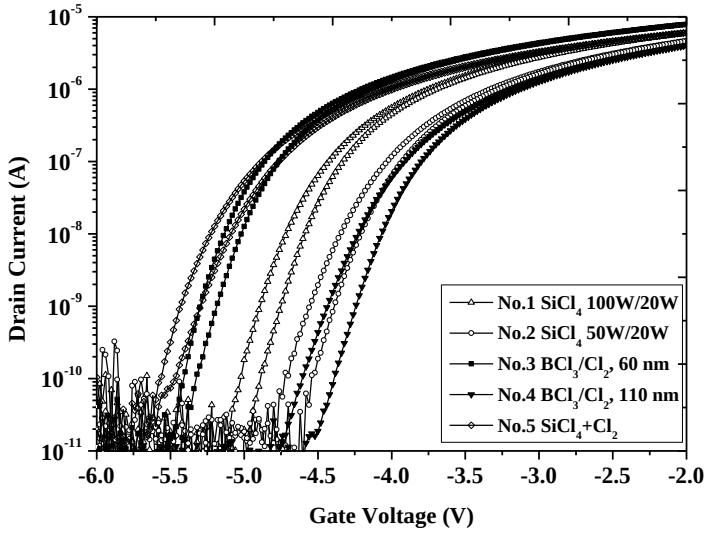

Fig. 6 I_d-V_g characteristics of GaN MOSFETs of all the samples in the subthreshold region

4. Conclusion

The dry recessed-gate GaN MOSFETs on AlGaN/GaN heterostructure etched with BCl_3 gas were fabricated. A high maximum electron mobility of 141.5 $cm^2V^{-1}s^{-1}$ and a low interface state density were obtained. This indicates that BCl_3 is possibly a suitable candidate as an etching gas to fabricate MOSFETs on AlGaN/GaN heterostructure. Further work is necessary to optimize the recess process condition of BCl_3 gas.

References

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