

Analysis of transient current distribution characteristics of Press Pack IGBT

Jinyuan Li¹, Yaosheng Li¹, Peng Wang¹, Zhibin Zhao²

¹ State Key Laboratory of Advanced Power Transmission Technology (Global Energy Interconnection Research Institute of State Grid Corporation of China), Beijing 102209, China

²State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources (North China Electric Power University), Beijing 102206, China

Email of all the authors: lijinyuan@geiri.sgcc.com.cn; liyaosheng@geiri.sgcc.com.cn; wangpeng@geiri.sgcc.com.cn

Corresponding Author: lijinyuan@geiri.sgcc.com.cn

Abstract— In the switching process of Press Pack IGBT (PPI) module, the phenomenon of nonuniform current distribution invariably happens which reduce the reliability and life time of chips and the module. The uneven current distribution would be caused by some physical reasons such as the clamp force, the temperature; and the electrical reasons including the parasitic inductance of the emitter pillars, the parasitic resistance of the gate connector and the difference of the paralleled chips characteristic, etc. Based on the modeling of two disparate module structures, the parasitic parameter of the emitter pillars and gate connector is extracted in this paper. Then the different equivalent circuits of PPI module are built due to the researches in different factors with the Synopsys Saber software. At last, by comparing the influence of two modules indifferent factors, the simulation results prove the relationship between the pillars distribution and the chip switching losses.

Index Terms—Press Pack IGBT (PPI), encapsulation, parasitic parameter, transient current distribution

1. Introduction

Press Pack IGBT(PPI) has been developed for decade years since 1993, when the μ -stack was put forward by Fuji Corporation. Comparing with the traditional IGBT module, PPI has being more attractive due to its advantages like no bonding wire, high reliability, low thermal resistance and high power density. Therefore, the PPI is increasingly preferred in the application in HVDC [1], motor traction [2] and pulse power application, etc.

Up to now, there are two encapsulations of PPI module in manufacture. The first type is so-called PressPack encapsulation (Fig.1) which is applied in product of *WESTCODE* and *TOSHIBA*. This encapsulation have advantage in simple-structure and easily-manufacturing, the IGBT as well as the FRD chips in the encapsulation is stacked on the blocky pillar. However, the structure of the emitter plate pillar causes the rigid stress on the chips which make the equal clamping force distribution on the chip-level easily affected by the working condition, which furtherly affects the current distribution between the paralleled chips.



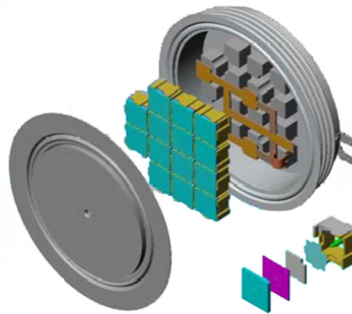


Fig.1 PressPack encapsulation

The second type is StakPak encapsulation (Fig2), which is only manufactured by *ABB* Corporation. Different from the first encapsulation, the structure replaces the blocky rigid pillar by the press-pin consisting of the spring unit and the conductive shrapnel, which optimizes the uneven clamping force distribution on the top of IGBT chips, as well as the current distribution. However, the press-pin structure also increases the complexity of the emitter plate model.

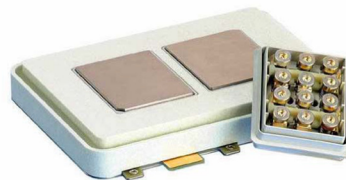


Fig.2 StakPak encapsulation

The researches have been proceeded respectively in [4]-[5] to analyze the clamping force distribution of two encapsulations, aiming at the problem of current distribution of PPI. Moreover, the optimization of force distribution brought by the press-pin structure is particularly illustrated in [5], which is conducive to improve the uniformity of the chips work condition, and guarantee the reliability of the module. In [6]-[7], it is put forwarded that the nonuniformity of force distribution on chip-level furtherly result in the difference of contact electrical resistance, contact thermal resistance and power cycling capability, which affect the equivalent of current distribution in paralleled chips.

In respect of electrical interference, the test platform researching in the current distribution in both the StakPack [8] and PressPack[9] encapsulation are built and optimized and then finish the analysis of the two encapsulations, then, [9] mentions the current distribution can be influenced by the parasitic resistance of gate connector. At last, due to the effect of gate resistance of paralleled IGBT module on the current distribution, it is proved that the switching time of modules depending on the gate resistance easily leads to the switching delay between the IGBT modules, and furtherly influences the current distribution [10]. The result of gate resistance is referencable for the analysis of the gate connector in this paper.

The purpose of this paper is to analyze three electrical effect factors of transient current on the chip-level, which includes: 1) the parasitic inductance of the emitter plate; 2) the parasitic resistance of the gate connector in high frequency condition; 3) the difference of chip characteristic. To research the structural effect to the current distribution, the parasitic parameters of two existing PPI encapsulations are extracted and analyzed. Based on the extraction result, the testing equivalent circuits are built to finish the simulation and comparison of the transient current characteristic of the two encapsulations.

2. overview of Simulation process

To analysis the effect of three factors, the structures of the emitter plate and the gate connector of two encapsulations is modeled in the actual size. Based on the ANSYS Q3D software, the models are furtherly meshed and calculated with the finite element method (FEM). The choice of the boundary condition depends on the current direction in emitter plates and the gate connector. The simulation frequency is decided by the experimental formula of the pulse signal equivalent frequency [11].

$$f = \frac{0.25}{t_r} (\text{Hz}) \quad (1)$$

Where the t_r is the rise time of the square pulse, which, take the typical value of the IGBT dynamic parameters as an example, is defined as the rise process from 10% of the signal amplitude to 90%. Refer to the datasheet of ABB IGBT chip, the rise time of collector current can be valued in 250ns and the simulation frequency is 1MHz based on the formula (1).

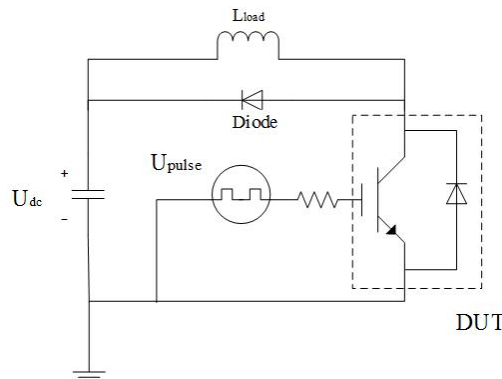


Fig.3 Schematic of test circuit

With the Model Architect (MA) plug-in of Synopsys Saber software, different equivalent circuit of PPI can be built with the parameter-defined component aiming at the simulation for different effect factors. Fig.3 is the test circuit of PPI module with the double-pulse method. Focusing on the oscillation of the second switching time, the peak value of the oscillation is picked to analysis the current distribution between the chips. As shown in Fig.3, the DUT (device under test) shows the position of the module which can be replaced by the equivalent circuits of module in different simulation, and the freewheeling diode is paralleled with the inductive load.

In addition, the result data needs to be normalized to unify the simulation result of different encapsulations, which is convenient to analyze the current characteristic. For this purpose, the simulation waveform of chip n $i(n, t)$ need to be converted into $i'(n, t)$ with formula (2).

$$i'(n, t) = i(n, t) / I_{\max} \quad (2)$$

I_{\max} is the maximum of chips current overshoot.

In order to provide basis for the analysis of transient turn-on current characteristic, the “unbalance degree” β need to be defined and the calculate formula is shown as follow.

$$\begin{aligned} \beta &= (I_{\max} - I_{\min}) / I_{\max} \times 100\% \\ &= (i'_{\max} - i'_{\min}) \times 100\% \end{aligned} \quad (3)$$

Where the i'_{\max} and i'_{\min} is respectively the maximum/ minimum of the current overshoot in all IGBT chips.

3. Effect of parasitic inductance of emitter plate

When PPI is switching on, the effect of parasitic parameter is amplified by the high-frequency switching current, which occurs in both PressPack and StakPak encapsulation. However, compared with the parasitic inductance, the resistance of emitter plate in high frequency is ignorable. Hence, in this part, the attention is only paid on the effect of parasitic inductance of emitter plate.

A. Effect of pillar distribution in PressPack encapsulation

The emitter structure of PressPack encapsulation is commonly used in PPI module. However, the distribution of the pillars with IGBT chips is distinguishing in different product. To reduce the variability of pillars distribution in this research, the distribution form of emitter pillars primarily needs to be confirmed in case of the unrepresentative simulation result.

The definition of GCD (Geometric coincidence degree) of emitter plate which means the number of

the pillars/press-pins being in the same symmetrical position through the axis of symmetry to facilitate the statement of analysis result. Then, the simulation only concern about the emitter structure with symmetrical pillar distribution which is conducive to obtain a regular simulation result. Building on this premise, two emitter structures of PressPack encapsulation are chosen to research the connection between the current distribution and the pillar distribution (as Fig.4).

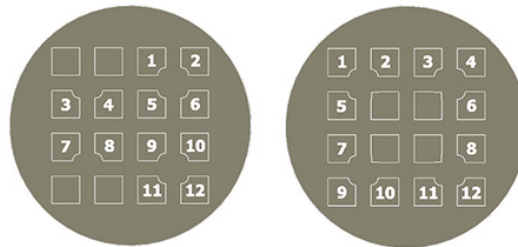


Fig.4 Pillar distribution
model (a) (left) and model (b) (right)

Model (a) is singly symmetrical and the GCD of pillars is 2. While in the model (b), pillar 1, 4, 9, 12 are symmetrical and their GCD is 4; the remaining pillars are symmetrical and the GCD is 8.

Based on the modeling, the parasitic inductance of the two emitter structures is extracted by ANASYS Q3D software, furtherly the equivalent circuit of DUT is built as Fig.5. In this circuit, the parasitic parameter of the main testing circuit, the connector plate and the gate connector are ignored to highlight the only effect of the pillar distribution.

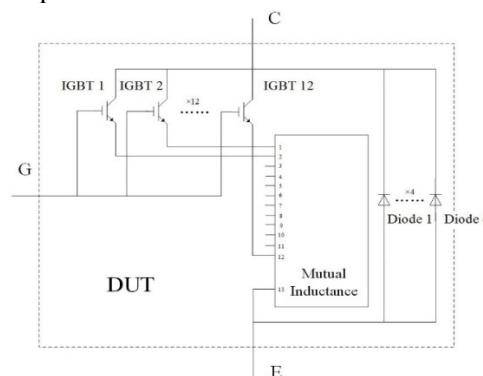
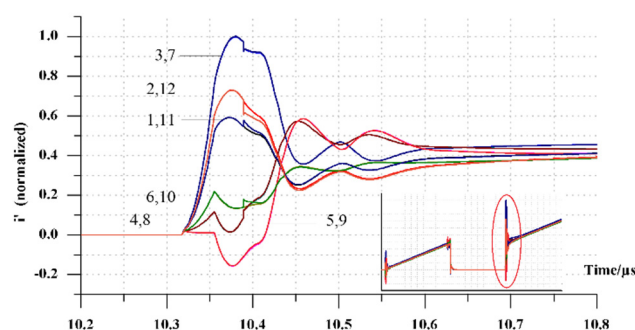


Fig.5 DUT equivalent circuit for emitter plate simulation

Besides, with the MA plug-in, the IGBT chips models are defined uniformly, and the four FRDs of module are replaced by the ideal diodes in the equivalent circuit. The Mutual Inductance is parameter-defined component with the parasitic inductance extracted by the Q3D, which includes the 12 input pins and 1 output pin. The parasitic effect of pillars can be represented by the 12 input pins of component.



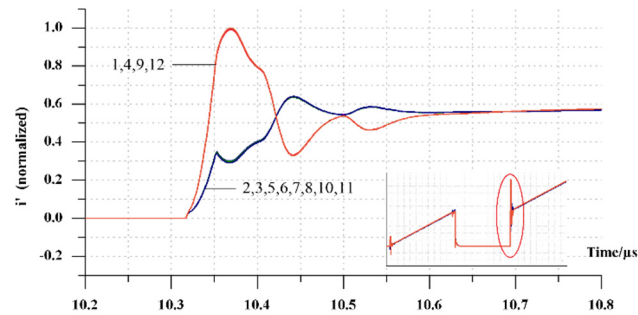


Fig.6 Simulation result of model (a) (up) and model (b) (down)

Based on the test circuit combining with the DUT equivalent circuit, Fig.6 is the simulation current waveforms of the IGBT chips in DUT and the partial enlarged view of the second turn-on current oscillation of double-pulse test. According to the result, the overlap feature of the current waveform is conformed with the characteristic of the pillars geometric coincidence degree, which means the uniformity of chips current can be improved when the distribution of the emitter pillar have a certain GCD, while the current distribution of on state is considerably influenced by the low GCD of the emitter pillar. Based on this comparison of two structures, model (b) is preferred to meet the requirement of reliability and chosen as the model for the analysis. Picking the peak value of the second switching oscillation of pillar n $i'_{\max(n)}$ by the following formula and summarizing the result of current distribution as Tab1.

Tab. 1 Simulation result of model (b)

Number	1	2	3	4
$i'_{\max(n)}$	0.996	0.638	0.638	0.994
Number	5	6	7	8
$i'_{\max(n)}$	0.639	0.638	0.636	0.640
Number	9	10	11	12
$i'_{\max(n)}$	0.992	0.637	0.640	1

$$i'_{\max(n)} = \max\{i'(n, t)\} \quad (4)$$

As the result, the geometry feature of the pillars distribution can be directly reflected in the current distribution. According to the data in Tab1, the unbalance degree of model (b) is 36.4%, while the β of model (a) is 63.6%, which furtherly proves that the current balance between the chips and the reliability of module needs to be guaranteed by the symmetry and a certain GCD of the pillar distribution.

B. Effect of press-pin distribution in StakPak encapsulation

As stated forward, the StakPak encapsulation produced by ABB Corporation is of the optimized technology to improve the reliability of PPI module. A module consists of a number of parallel connected subassemblies, called “submodules” inside a rigid frame, which is to meet the requirement of the power level of the module. In such a condition, the coupling of the submodules and the press-pins are increasingly complicated.

Same as the simulation process above, the effect of press-pin distribution in StakPak encapsulation needs to be analyzed by the current simulation of submodule and the module. Fig.7 is the press-pin-labeled emitter structure of the submodule without the nonconducting part like the spring, spacer and the axis.

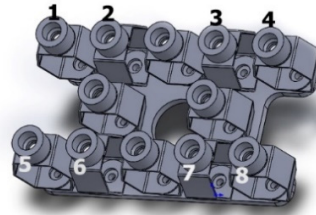


Fig.7 Labeled structure of emitter plate with press-pins

Based on the double-pulse testing circuit, the equivalent circuit of DUT is changed by reduce the number of IGBT branch from 12 to 8, and redefining the Mutual Inductance with the parasitic inductance extracted from the emitter model of submodule.

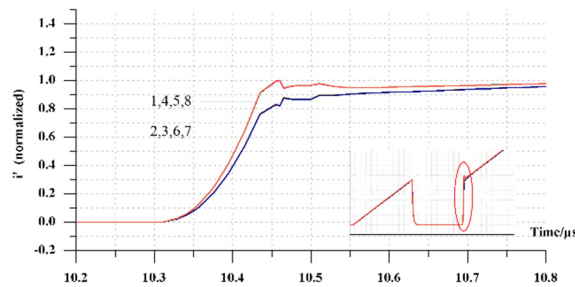


Fig.8 Simulation result of emitter plate of submodule

According to the emitter model, there are two symmetrical relationships of the press-pins: the GCD of the press-pin (1,4,5,8) and (2,3,6,7) are both 4, which can be reflected in the simulation waveform as Fig.8. Then, the peak value of the transient current overcome of the chips is arranged in Tab2 to analysis the current distribution between the paralleled chips.

Tab. 2 Simulation result of submodule

Number	1	2	3	4
$i'_{\max(n)}$	1	0.918	0.918	1
Number	5	6	7	8
$i'_{\max(n)}$	1	0.919	0.918	1

From Tab2, the unbalance degree β of submodule is 8.2%, which reflects that the overshoot of the transient turn-on current is adequately small for the submodule. Because of the relatively high uniformity of submodule, the module can meet the requirement of the reliability if the rigid frame have satisfactory shielding effect.

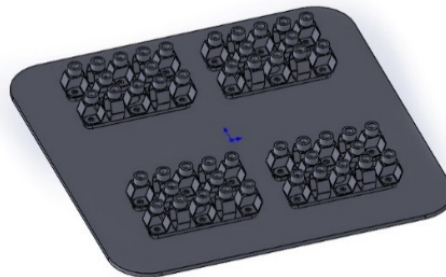


Fig.9 the expanded model

Based on the actual size ABB 5SNA 2000K451300 module, the submodules are expanded to an

emitter model of the PPI module, which increase the number of the press-pin and complicate the coupling of the structure. The emitter module is shown in Fig.9.

After the extension, the equivalent circuit needs to be change similarly with the submodule. The branches of IGBT chip need to be increased to 32. While, the Mutual Inductance needs to be defined as a 33-pin component based on the parasitic inductance extracted from the new emitter module, which includes 32 input pin and 1 output pin.

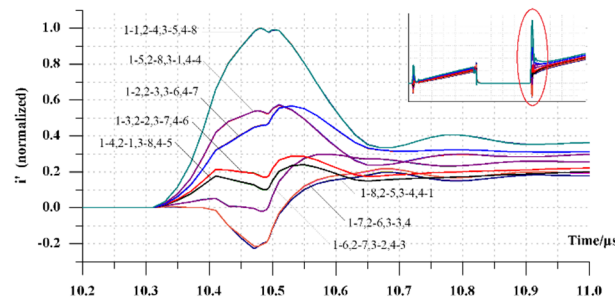


Fig.10 Simulation result of expanded model

The rigid frame between the submodules is ignored which strengthens the coupling between the submodule and the influence on current distribution. The simulation result (Fig.10) and the peak value of transient overshoot (Tab3) are more conducive to research the connection between the press-pin distribution and the current characteristic.

Tab. 3 Simulation result of expanded model

Number	1-1	1-2	1-3	1-4
$i'_{\max(n)}$	0.999	0.565	0.290	0.240
Number	1-5	1-6	1-7	1-8
$i'_{\max(n)}$	0.574	0.299	0.217	0.199
Number	2-1	2-2	2-3	2-4
$i'_{\max(n)}$	0.241	0.290	0.569	1
Number	2-5	2-6	2-7	2-8
$i'_{\max(n)}$	0.199	0.218	0.299	0.573
Number	3-1	3-2	3-3	3-4
$i'_{\max(n)}$	0.575	0.300	0.217	0.199
Number	3-5	3-6	3-7	3-8
$i'_{\max(n)}$	0.999	0.569	0.290	0.240
Number	4-1	4-2	4-3	4-4
$i'_{\max(n)}$	0.198	0.218	0.300	0.574
Number	4-5	4-6	4-7	4-8
$i'_{\max(n)}$	0.241	0.290	0.568	1

From the result above, the external chips support larger current overshoot than the internal chips. Combining with the simulation result of PressPack encapsulation, the rule of the GCD of the press-pins distribution can be reproved. However the unbalance degree in this simulation have no practical significance because the simulation structure is incomplete. So, the unbalance degree of the module is skipped.

4. Effect of parasitic resistance of gate connector

After the gate pulse signal generating, the gate-emitter capacitance C_{ge} and gate-collector capacitance C_{gc} are charged by the gate current i_g before the v_{ge} reaching the threshold voltage. v_{ge} rises by a time constant which is influenced by the gate resistance:

$$v_{GE}(t) = V_{GE} (1 - e^{-\frac{t}{\tau}}) \quad (5)$$

Where the time constant is:

$$\tau = R_G (C_{GE} + C_{GC}) \quad (6)$$

In the high frequency condition, there is mΩ-level parasitic resistance between the external gate board and the gate of IGBT chips, which can influences the turn-on time and, furtherly, the current distribution of chips.

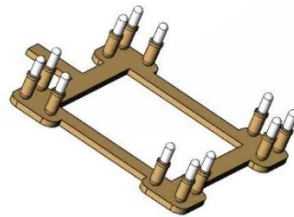


Fig.11 Model of gate connector

Based on model of the PCB gate connector and the gate thimble in PressPack encapsulation (Fig.11), the parasitic resistance can be extracted into Tab4 as follow.

Tab. 4 Parasitic resistance of gate connector

Number	1	2	3	4
parasitic resistance/mΩ	8.7871	1.8034	1.7919	2.0391
Number	5	6	7	8
parasitic resistance/ mΩ	3.5365	3.4978	4.5385	12.405
Number	9	10	11	12
parasitic resistance/ mΩ	4.5385	3.042	10.466	19.035

The parasitic resistance of gate connector is respectively defined in the resistance component in new equivalent circuit of DUT (Fig.12). While the Mutual Inductance is taken out to singularize the effect factor of current distribution.

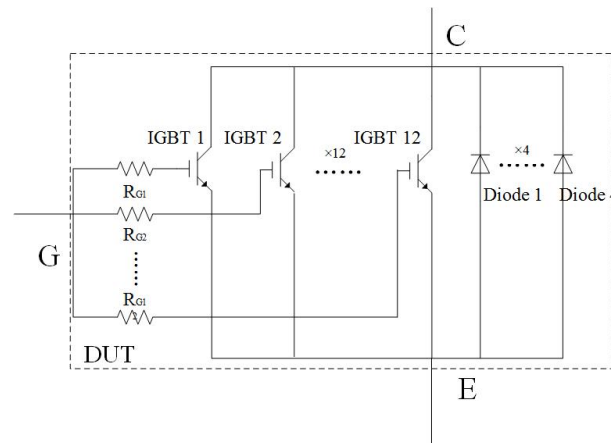


Fig.12 DUT equivalent circuit for gate connector simulation

In Fig.12, the IGBT chips are same-defined component and the gate resistance of IGBT chips R_{gn} is defined with the resistance value extracted in Tab4. The simulation current waveform is shown in Fig.13.

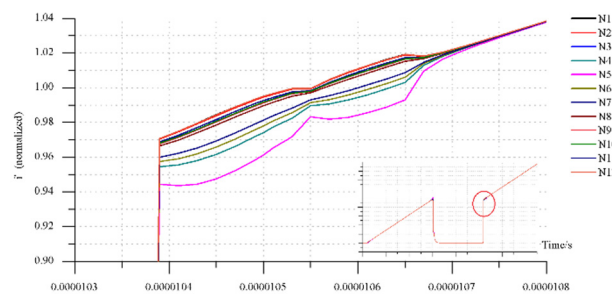


Fig.13 Simulation result of gate connector

Because the oscillation is small, the $i'_{\max(n)}$ is difficult to choose. However, based on the formula (3), the unbalance degree can be figured out into 1.7%~3.4% during the turn-on period. Compared with the effect of parasitic inductance of emitter structure, the interference of gate connector is much smaller than emitter plate which means the effect of the gate connector can be ignored in some research.

5. Effect of nonuniformity of chips' characteristic

Chip junction temperature is different under various pressures, its parameters characteristic cannot remain unchanged and remain consistent with the desired characteristic especially after a certain time of loss. The formula (6) shows that the capacitance characteristics of the chip is also a reason of chip's turn-on delay. Thus, the different characteristics of the chip will also affect the turn-on current characteristics.

In order to study the factors, the plug-in MA is used to complete the precise definition and modification of the IGBT chip characteristics. The simulation will be based on the model of StakPak encapsulation above, building eight-branch DUT equivalent circuit. Then make 1pF fine-tuning in the IGBT chip characteristics of 8th branch, which includes input capacitance C_{ies} , output capacitance C_{oes} , and reverse transfer capacitance C_{res} curves. To study uneven impact of current due to the characteristics of the chip, the trimming process of chips' characteristic is shown in Fig.14.

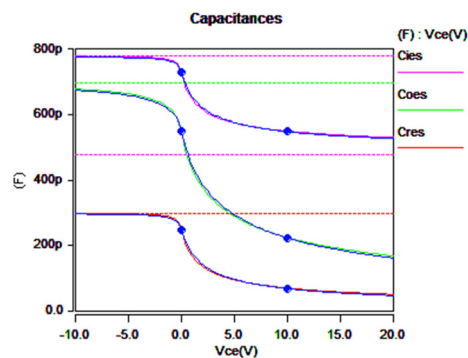


Fig.14 Trimming process of IGBT chip's characteristic

Fig.15 is the DUT equivalent circuit in this simulation. Compared with Fig.5 and Fig.12, the circuit ideal and the parasitic parameter of gate, collector and emitter are ignored to singularize the effect factor.

Then get the simulation results shown in Fig.16. Because of the ideal simulation, the waveform of 1st-7th chips are overlapping with each other, while the overshoot current is complementary on each chip, which means that the current undershoot of the 1st to 7th seven IGBT chip are equal to supply the current overshoot of eighth chips.

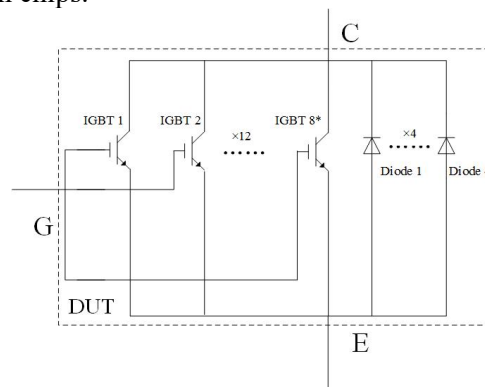


Fig.15 DUT equivalent circuit for nonuniformity of paralleled chips simulation

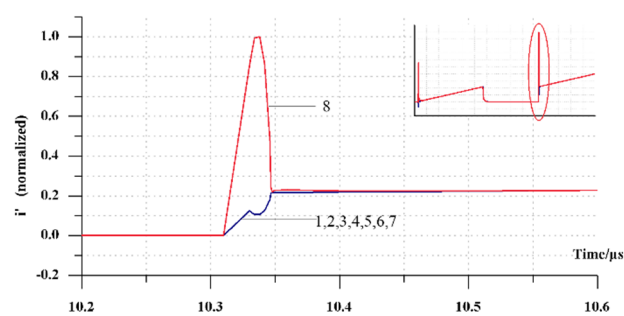


Fig.16 Simulation result of chips characteristic nonuniformity

According to the results, the unbalance degree is 78.1%. However with the change of parameters like the chips number in parallel and the GCD of the emitter plate, this effect may be different. This effect may reduce the current difference in paralleled chips, more likely to destroy the existing current balance. If the uniformity of chips' characteristic cannot meet the requirement, its effect can be inestimable or more serious than the other effect factors mentioned above.

6. Conclusion

In this paper, the electrical effect of the transient turn-on current distribution is summarized in three aspects. After the simulation and analysis of the effect factors based on two PPI encapsulations, the

turn-on current distribution is closely related to the feature of the pillars/press-pins distribution by the rules of GCD and the degree of chips expanding. Then compared with the emitter effect, the parasitic resistance of gate connector have little influence on transient current. At last, the nonuniformity of paralleled chips characteristic plays the inestimable and significant role in the feature of current distribution which can easily reduce the reliability and lifetime of the PPI module.

Acknowledgements

This work presented in this paper has been supported by the National Science and Technology Major Project(2015ZX02301)

References

- [1] H. Shigekane, H. Kiriara, and Y. Uchida, "Developments in modern high power semiconductor devices," in *IEEE Int. Symp. Power Semiconductor Devices and IC's*, 1993, pp. 16-21.
- [2] H. Chen, W. Cao, P. Bordignon, R. Yi, H. Zhang and W. Shi, "Design and testing of the World's first single-level press-pack IGBT based submodule for MMC VSC HVDC applications," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 3359-3366.
- [3] A. Golland and F. Wakeman, "Application of press-pack IGBTs in traction refurbishment," *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005*, Austin, TX, 2005, pp. 2030-2035 Vol. 3.
- [4] A. Hasmasan, C. Busca, R. Teodorescu and L. Helle, "Modelling the clamping force distribution among chips in press-pack IGBTs using the finite element method," *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Aalborg, 2012, pp. 788-793.
- [5] S. Eicher et al., "4.5kV press pack IGBT designed for ruggedness and reliability," *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, pp. 1534-1539 vol.3.
- [6] C. Busca, R. Teodorescu, F. Blaabjerg, L. Helle and T. Abeyasekera, "Dynamic thermal modelling and analysis of press-pack IGBTs both at component-level and chip-level," *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, Vienna, 2013, pp. 677-682.
- [7] F. Wakeman, K. Billett, R. Irons and M. Evans, "Electromechanical characteristics of a bondless pressure contact IGBT," *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, Dallas, TX, 1999, pp. 312-317 vol.1.
- [8] A. Müsing, G. Ortiz and J. W. Kolar, "Optimization of the current distribution in press-pack high power IGBT modules," *Power Electronics Conference (IPEC), 2010 International*, Sapporo, 2010, pp. 1139-1146.
- [9] X. Tang, X. Cui, Z. Zhao, P. Zhang, J. Wen, R. Zhang. "Analysis of Transient Current Distribution Characteristics of Parallel Chips in Press Pack IGBT," *Proceedings of the CSEE*, vol.36, 2016. [Online]. Available: <http://www.cnki.net/kcms/detail/11.2107.TM.20160615.1517.003.html>
- [10] Y. Xiao, "Research on Parallel Connected IGBT Power Modules," Ms. D. dissertation, Dept. Elect. Eng. Zhejiang Univ. Hangzhou, 2015
- [11] K. Zou, "Dynamic Characteristics Testing and Modeling for High Voltage IGBT Module," Ms. D. dissertation, Dept. Elect. Eng. North China Electric Power Univ. Beijing, 2015.