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Design of c-band telecontrol transmitter local oscillator for UAV data link

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Abstract. A C-band local oscillator of an Unmanned Aerial Vehicle (UAV) data link radio frequency (RF) transmitter unit with high-stability, high-precision and lightweight was designed in this paper. Based on the highly integrated broadband phase-locked loop (PLL) chip HMC834LP6GE, the system performed fractional-N control by internal modules programming to achieve low phase noise and small frequency resolution. The simulation and testing methods were combined to optimize and select the loop filter parameters to ensure the high precision and stability of the frequency synthesis output. The theoretical analysis and engineering prototype measurement results showed that the local oscillator had stable output frequency, accurate frequency step, high spurious suppression and low phase noise, and met the design requirements. The proposed design idea and research method have theoretical guiding significance for engineering practice.

1. Introduction

Frequency source is a module that generates a large number of discrete frequencies with the same stability and accuracy as the reference signal through linear operations in the frequency domain by one or more reference sources with high frequency stability and accuracy. It is an important front part of RF communication system. With the development of UAV data link system, the frequency source has also been put forward higher and higher requirements. This is mainly reflected in: fast conversion speed, wide frequency band coverage, small frequency resolution, high stability, low spurious, low phase noise, small size, light weight and multi-function [1][2].

The HMC834LP6GE is a low noise, wide band, fractional-N PLL chip that features an integrated Voltage Controlled Oscillator (VCO) with a fundamental frequency of 2800 MHz - 4200 MHz, and an integrated VCO Output Divider (divide by 1/2/4/6.../60/62) and doubler, that together allow the HMC834LP6GE to generate frequencies from 45 MHz to 1050 MHz, from 1400 MHz to 2100 MHz, from 2800 MHz to 4200 MHz, and from 5600 MHz to 8400 MHz. The integrated Phase Detector (PD) and delta-sigma modulator, capable of operating at up to 100 MHz, permit wider loop-bandwidths with excellent spectral performance. The HMC834LP6GE features industry leading phase noise and spurious performance, across all frequencies, that enable it to minimize blocker effects, and improve receiver sensitivity and transmitter spectral purity [3][4].

High-performance frequency source of UAV data link system based on HMC834LP6GE can be designed by adding simple peripherals, such as power supply circuit, reference circuit and loop filter.

2. System design

The indicators required by an UAV telecontrol transmitter local oscillator are: The output frequency is 5600 ~ 5800MHz, with 8MHz step; the frequency stability is better than 3ppm; the phase noise is better than -80dBc / Hz / 10 KHz; the size of the circuit board is controlled within 120mm × 60mm.

According to the system requirements, the local oscillator of the telecontrol transmitter based on the integrated PLL chip HMC834LP6GE was designed; the block diagram is shown in figure 1. PD, CP (charge pump) and VCO are integrated in the chip HMC834LP6GE. 100MHz temperature compensated crystal oscillator (TCXO) was chosen as the reference source (REF). Considering the phase noise and the frequency interval, we selected 100MHz as the PD frequency, and made the PLL chip operating under the fractional-N mode. The low pass filter (LPF) was designed as a 4-stage passive filter and a 2-stage amplifier was adopted. Power supply consisted of three + 5V and a + 3.3V. The AVR chip ATmega8L was selected as the microcontroller (MCU).

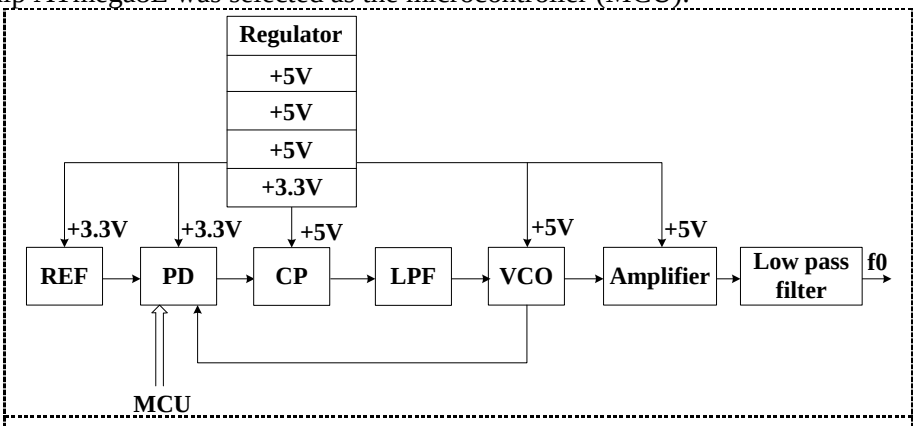


Figure 1. Block diagram of the system.

3. Hardware design

3.1. Reference circuit design

An excellent reference source is important for a frequency source system. Reference source performance is good, and then the choice of synthesis and device will have a larger space [5]. High-performance 100MHz TCXO WTX-503CE57C3.3-100.000MHz was chosen according to performance, cost and volume. The size of the TCXO is 5 * 3.2mm, with 3.3 V power supply, and the current is 10mA. The output waveform is HCMOS and the frequency stability is 0.5ppm. The TCXO has the advantages of high output frequency, high stability, small size and low power consumption, which can satisfy the design requirements. The reference frequency source circuit is shown in figure 2. The reference input pin of synthesizer was connected with a 100Ω resistor which connected to the ground in order to ensure 50Ω matching; an AC coupling capacitor was connected also.

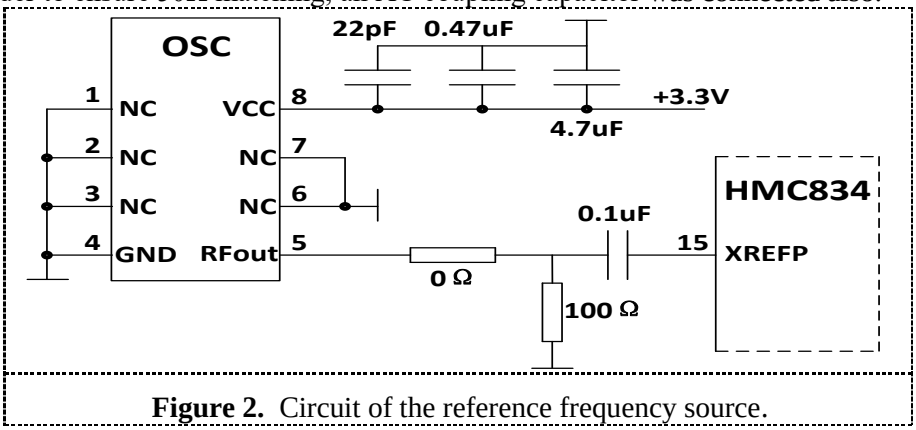


Figure 2. Circuit of the reference frequency source.

3.2. Power supply design

There are a lot of power pins in HMC834 chip. In order to achieve a better anti-interference performance of the circuit, the method of separate power supply was adopted. VCC1 and VCC2 of the chip shared a single 5V linear regulator, which avoid the VCO affecting by interferences. CP power supply pins VPPCP and VDDLS shared a 5V linear regulator. The 2-stage power amplifiers used a 5V

linear regulator. The rest power supply pins, MCU and TCXO shared a 3.3V linear regulator together. The voltage regulators adopted two models: LT1763CS8 with +5V output voltage and LT1963AEST with +3.3V output voltage.

3.3. Loop filter design

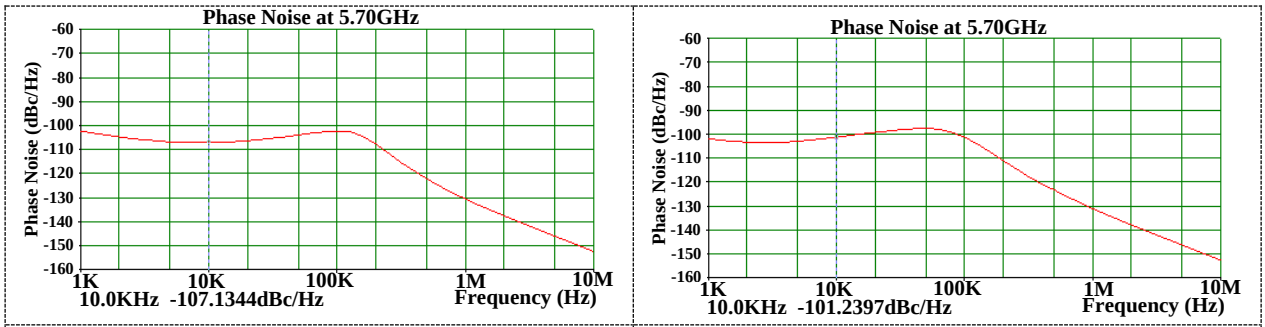
The loop filter is located between CP and VCO, it not only filters out the noise from the crystal, the output noise of the PD itself and the carrier frequency , as well as the leakage of the PD frequency, but also filters out the noise from the VCO [6]. The design of loop filter is the key of the design of a frequency synthesizer, and the technical indicators of the system should be rational considered. The bandwidth of the filter design needs to be compromised, if the bandwidth is narrow, the noise influence from VCO is serious and the loop locking time is extended; if the bandwidth is wide, the noise influence from crystal oscillator and PD is serious [7]. In this design, the TCXO with better phase noise was selected as the reference source, which makes the near-end noise relatively small. For the noise of the far-end, the noise from VCO in HMC834 plays a leading role. Therefore, in order to suppress the high frequency noise of VCO, the loop bandwidth should be set wider [8][9].

ADI Company's ADIsimPLL4.2 software was adopted in this design. PLL circuit can be designed more convenient by using the software through the following operations: chip selection, frequency divider selection, PD frequency selection, reference frequency selection and phase noise model input, loop bandwidth, phase margin setting, loop filter selection, etc. [10]

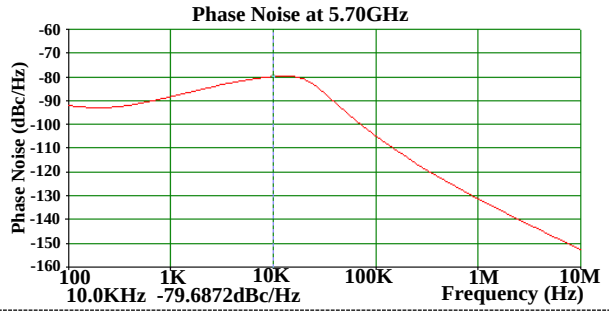
Three loop bandwidth of 125KHz, 75KHz and 18.9KHz were simulated in this design, four-order passive low pass filters were adopted in all the three designs. Figures 3(a), 3(b) and 3(c) are the phase noise curves of frequency 5700MHz of the three kinds of bandwidth, and table 1 is the comparison of the phase noises. It can be seen that the low frequency offset phase noise is poor when the loop bandwidth is very narrow, while the high frequency offset phase noise behaves fairly well under all the three bandwidths. According to the comparison, the best phase noise performance was the bandwidth of 125 KHz, so the final selection of bandwidth was 125KHz. The circuit is shown in figure 4. The ideal value of phase noise is -107.1dBc/Hz/10KHz, which obviously meets the design requirements.

Table 1. Phase noise table.

Frequency	Phase Noise		
	125KHz	75KHz	18.9KHz
100Hz	-92.83	-92.83	-91.93
1.00KHz	-102.3	-101.9	-88.20
10.0KHz	-107.1	-101.2	-79.69
100KHz	-102.2	-101.4	-104.9
1.00MHz	-130.7	-131.1	-131.3



(a) **(b)**



(c)

Figure 3. Simulation results of phase noise curves at different loop bandwidth, (a) bandwidth=125KHz, (b) bandwidth=75KHz, (c) bandwidth=18.9KHz.

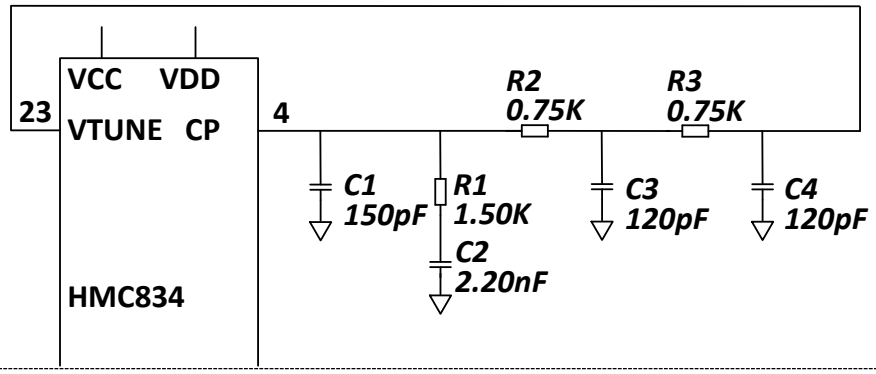


Figure 4. The parameters of loop bandwidth 125KHz.

4. Software design

4.1. Registers configuration

There are a total of 18 PLL registers and 7 VCO subsystem registers in HMC834. PLL registers are from Reg00h to Reg13h, including multiple frequency division coefficient registers, charge pump register, lock detect register, etc. VCO subsystem registers are from VCO_Reg00h to VCO_Reg06h, including VCO frequency division coefficient setting, the output power setting and the signal output setting, etc. The operation of the VCO subsystem registers is achieved by writing the PLL register Reg05h [11]. The default frequency of 5700MHz is configured in the following order shown in table 2.

Table 2. Register configuration.

Order No.	Registers	Value
1	Reg01h	0x000002
2	Reg02h	0x000001
3	Reg03h	0x00001C
4	Reg05h	0x007E28
5	Reg05h	0x00B6A0
6	Reg05h	0x002018
7	Reg05h	0x000000
8	Reg06h	0x030F4A
9	Reg07h	0x00014D
10	Reg08h	0xC1BEFF
11	Reg09h	0x547FFF
12	Reg0Ah	0x002046

Order No.	Registers	Value
13	Reg0Bh	0x07C021
14	Reg0Ch	0x000000
15	Reg0Fh	0x000001
16	Reg04h	0x800000

4.2. Software implementation

Only writing operation is needed when configuring the HMC834 registers in this design. When communicating, the MCU ATmega8L operates as the master device, HMC834 as the slave device. The master and slave devices communicate via the three-wire serial interface SEN (serial enable port), SDI (serial data input) and SCK (serial clock). When SEN is pulled high, communication is effective. SCK as clock trigger signal is generated by the delay program of the MCU, and the whole communication needs 32 clock cycles. The first data is the judgment of reading and writing, when the first clock arrives, the data bit is low to indicate the write command, the following 6 clocks are used to determine the register address, and the next 24 clocks for data transmission. When the SEN cleared, the write cycle is completed. The system software flow chart is shown in figure 5.

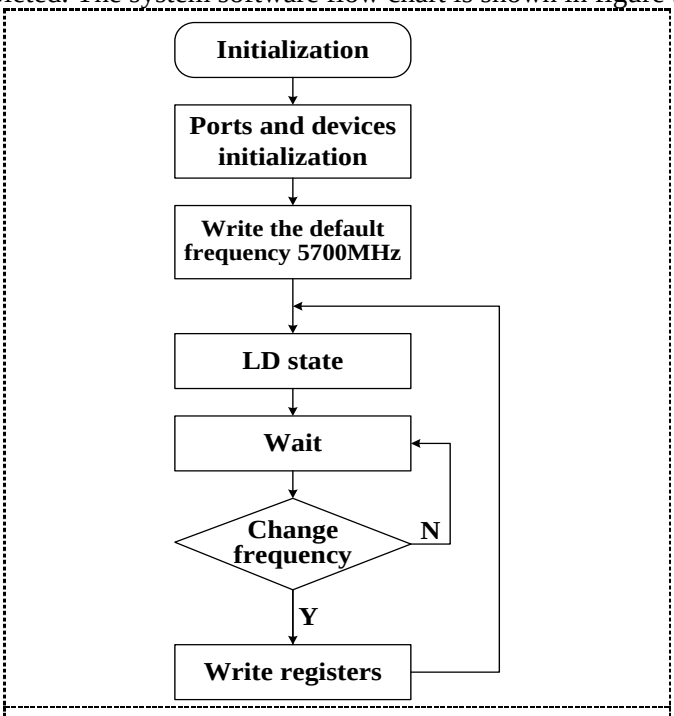


Figure 5. The flow chart of system software.

5. Test result

FSQ26 signal analyzer (RS Company) was adopted for testing. The measured spectrum of the local oscillator is shown in figure 6. Figures 6(a), 6(b) and 6(c) show the spectrum of frequency 5600 MHz, 5608 MHz, and 5800 MHz with the "span" of analyzer set to 200 MHz, 5 MHz, and 5 GHz. It can be seen that synthetic frequency range covers from 5600 MHz to 5800 MHZ, with 8 MHz step. Figure 6(d) shows the spectrum of the frequency 5700 MHz with the analyzer "span" set to 20 kHz, it can be seen that the phase noise is -103.33 dBc/ Hz/ 10 KHz. The local oscillator has been tested by high and low temperature experiments. According to the test results, the frequency stability of frequency 5700MHz is 2.3ppm. The measured size of the circuit board is 115×45 mm. It can be seen that all indicators meet the system requirements.

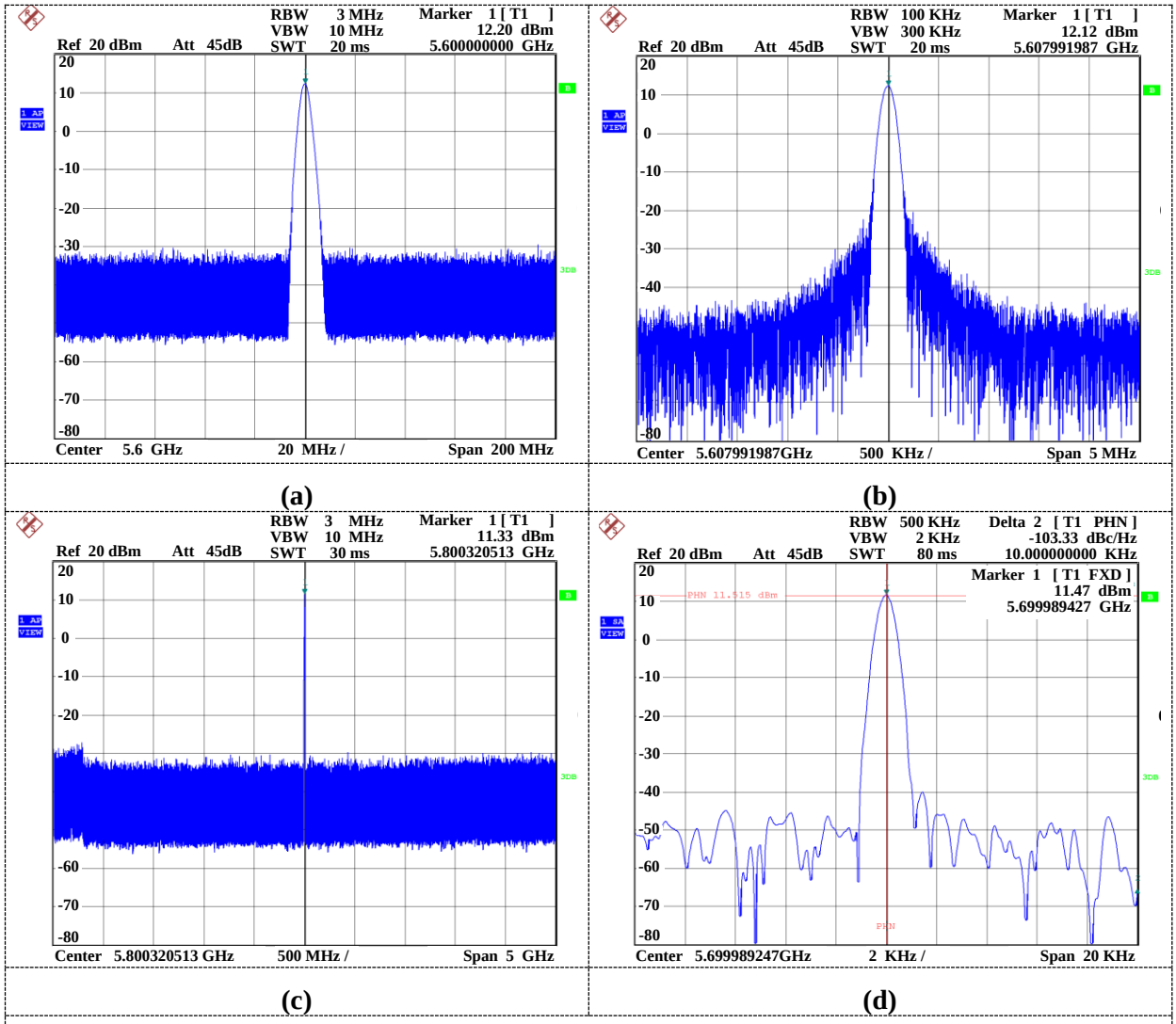


Figure 6. Test spectrum of the local oscillator by FSQ26 signal analyser of different frequency and span, (a) frequency=5600MHz and span=200MHz, (b) frequency=5608MHz and span=5MHz, (c) frequency=5800MHz and span=5GHz, (d) frequency=5700MHz and span=20KHz.

6. Conclusions

The local oscillator has been verified by flight tests. The results show that the design is reasonable, the indicators meet the system requirements, and the work is stable and reliable, which fully meet the requirements of the use of UAV data link telecontrol transmitter. This design can be applied to other related projects, with strong engineering practicability.

7. References

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