

Research on Parallel Three Phase PWM Converters base on RTDS

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Abstract. Converters parallel operation can increase capacity of the system, but it may lead to potential zero-sequence circulating current, so the control of circulating current was an important goal in the design of parallel inverters. In this paper, the Real Time Digital Simulator (RTDS) is used to model the converters parallel system in real time and study the circulating current restraining. The equivalent model of two parallel converters and zero-sequence circulating current(ZSCC) were established and analyzed, then a strategy using variable zero vector control was proposed to suppress the circulating current. For two parallel modular converters, hardware-in-the-loop(HIL) study based on RTDS and practical experiment were implemented, results prove that the proposed control strategy is feasible and effective.

1. Introduction

Modular parallel VSCs have many advantages, such as higher total current capability, lower ratings for the switching devices, unified design, and stronger system stability [1–4]. The problem of converters parallel operation is the circulating current [5–11], which exists in parallel operating converters without galvanic isolation in ac or dc side. Circulating current flows in a circular loop between the parallel converters and does not affect the net current into the power system, decreases the efficiency, distorts current, and may damage converters. The causes of circulating current are different output voltage and impedance discrepancy between the individual converters [5].

There are two approaches generally used to eliminate the circulating current: hardware isolation and control strategy suppress. Isolation approach [5] that separates dc power suppliers or add transformers in the ac side, can eliminate the zero-sequence circulating current ultimately, but increase the cost and weight of system. In addition, impedance in ac side can reduce the high frequency components of circulating current, but have few effect on the low frequency and dc component of it.

Control strategy suppress are mainly based on PWM algorithm [6–11]. [6] controlled two parallel three phase converters as a six-phase converter, so the zero-sequence circulating current (ZSCC) can be suppressed, but its realizing process is complicated and not suitable for modular VSCs. In [7], the zero vectors was removal to avoid the interaction caused by the particular discontinuous SVM, but ZSCC will still exist if there are any mismatches between the parallel converters. Based conventional SVPWM, [8–11] introduced a control scheme that adjusts the duration of zero vectors instead of eliminating the zero vectors.



Based on space vector pulse width modulation and zero vector allocation, this paper presents a strategy of suppressing circulating current. Section 2 presents the mathematical models and expressions of the parallel converters, and equivalent model of the ZSCC is studied. In Section 3, a control strategy using PI controller for zero-sequence inhibition is proposed. In Section 4, the simulation and experimental results shows that the proposed method can effectively suppress circulating current. Section 5 presents the conclusion.

2. Model of circulating current

The proposed parallel three phase converters have been shown in Fig.1. The two parallel converters are connected at both ac and dc sides directly without transformer or high impedance components.

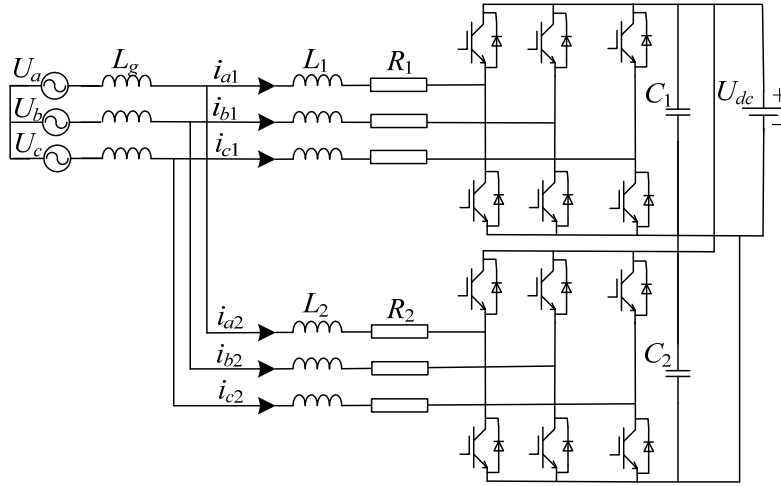


Fig.1 The topology of parallel converter

The circulating current equations of two parallel converters can be obtained [10]:

$$\begin{cases} L_1 \frac{di_{a1}}{dt} + R_1 i_{a1} + s_{a1} \frac{U_{dc}}{2} - L_2 \frac{di_{a2}}{dt} - R_2 i_{a2} - s_{a2} \frac{U_{dc}}{2} = 0 \\ L_1 \frac{di_{b1}}{dt} + R_1 i_{b1} + s_{b1} \frac{U_{dc}}{2} - L_2 \frac{di_{b2}}{dt} - R_2 i_{b2} - s_{b2} \frac{U_{dc}}{2} = 0 \\ L_1 \frac{di_{c1}}{dt} + R_1 i_{c1} + s_{c1} \frac{U_{dc}}{2} - L_2 \frac{di_{c2}}{dt} - R_2 i_{c2} - s_{c2} \frac{U_{dc}}{2} = 0 \end{cases} \quad (1)$$

Where $s_{xn}(x=a, b, c; n=1, 2)$ is the switching function of converters, when $s_{xn}=1$, the upper switches of phase x is on and lower switches off, when $s_{xn}=0$, the upper switches of phase x is off and lower switches on; L_1, L_2 are the filter inductance of converter module 1 and module 2, respectively. Since circulating current only flows between the converters, define zero-sequence circulating current i_0 and zero-sequence switching functions s_{01} and s_{02} as:

$$\begin{cases} i_0 = i_{a1} + i_{b1} + i_{c1} = -(i_{a2} + i_{b2} + i_{c2}) \\ s_{01} = s_{a1} + s_{b1} + s_{c1} \\ s_{02} = s_{a2} + s_{b2} + s_{c2} \end{cases} \quad (2)$$

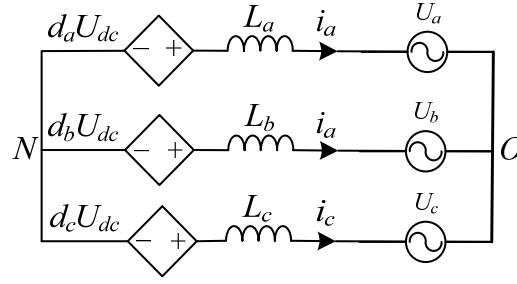


Fig.2 Averaged model of a three phase converter

Fig.2 is the averaged model of three phase converter, d_a , d_b and d_c is duty cycle of the converter upper bridge legs of each phase, respectively. For carrier-based PWM, the duty cycles are sinusoidal in steady state under balanced condition, therefore, the sum of d_a , d_b and d_c is zero. But SVPWM usually has triple harmonics in order to reduce switching losses, increase maximum modulation index, and decrease total harmonic distortion (THD), the sum of the duty cycles is not equal to zero, which can be defined as zero-sequence duty-cycle $d_z = d_a + d_b + d_c$. The following equation can be obtained:

$$\begin{cases} (d_a - \frac{d_z}{3}) + (d_b - \frac{d_z}{3}) + (d_c - \frac{d_z}{3}) = 0 \\ d_a' = d_a - \frac{d_z}{3} \\ d_b' = d_b - \frac{d_z}{3} \\ d_c' = d_c - \frac{d_z}{3} \end{cases} \quad (3)$$

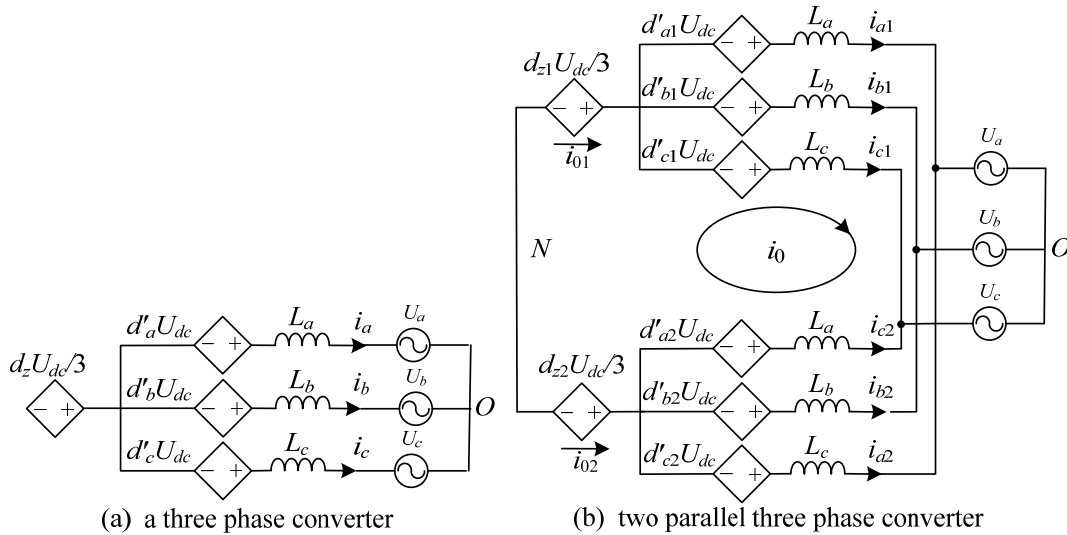


Fig.3 Averaged model of converter with zero-sequence components

Fig.3 (a) shows the averaged model of the three phase converter with zero-sequence components. For a single converter, the sum of i_a , i_b , and i_c is zero. Because of no zero-sequence current path, the zero-sequence voltage $d_z U_{dc}/3$ does not affect output voltage. Fig.3 (b) is averaged model of a three phase converter with zero-sequence components. If two or more inverters are connected in parallel, a

zero sequence current path is formed and may cause a circulating current. Fig. 4 shows the averaged model of the two parallel three phase converters, and the equation of ZSCC can be written as:

$$(L_1 + L_2) \frac{di_0}{dt} + (R_1 + R_2) i_0 = (d_{z1} - d_{z2}) U_{dc} \quad (4)$$

ZSCC has to do with the loop impedance, dc voltage and switching states, but nothing with the load impedance. When different PWM algorithms employed, the instantaneous switching states of the parallel converters are not the same, which will produce high frequency circulating current. If the switching states and filter impedance of the parallel converters are the same, the zero-sequence circulating current i_0 does not appear. Theoretically, when the output voltage and devices parameters of the every single converter in parallel are completely the same, circulating current does not exist.

3. Circulating current inhibition method

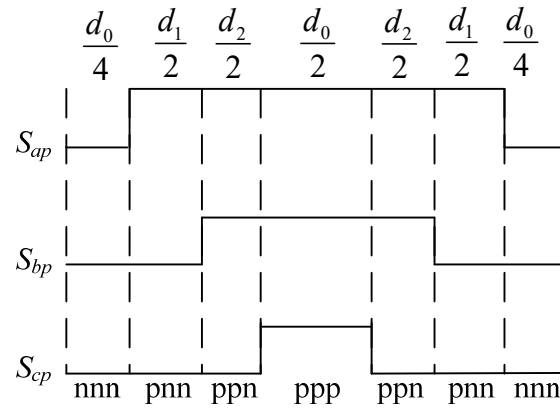


Fig.4 Switch states based on SVPWM

Fig. 4 is switch states based on common SVPWM modulation algorithm with alternative zero vectors, d_1 and d_2 is duty cycle of active voltage vectors pnn and ppn, respectively, d_0 is sum of duty cycle of zero voltage vectors ppp and nnn. By Fig. 4, d_a , d_b and d_c can be expressed as:

$$d_a = \frac{d_0}{2} + d_1 + d_2; d_b = \frac{d_0}{2} + d_2; d_c = \frac{d_0}{2} \quad (5)$$

By Equation (5), d_z can be written as: $d_z = d_a + d_b + d_c = 1.5d_0 + d_1 + 2d_2$. For the same active vectors and reference vectors, the allocation of the zero vectors may vary without affecting the output voltage. Based on this view, d_z can be controlled by the duty cycle of zero vectors, and the zero vector allocation factor k is defined as: $k = d_{ppp} / d_z$, d_{ppp} is duty cycle of zero vector ppp. When $k=0.5$, the Common SVPWM scheme is obtained, as shown in Fig. 4. Now d_z can be rewritten as:

$$d_z = d_a + d_b + d_c = 3kd_0 + d_1 + 2d_2 \quad (6)$$

The difference of d_z of the two converters is expressed as

$$\Delta d_z = d_{z1} - d_{z2} = 3d_0(k_1 - k_2) \quad (7)$$

The zero sequence current control strategy based on zero vector allocation factor k is shown in Fig. 5. The error between measured ZSCC and its reference, which is set to 0, is taken as input of PI controller, which can eliminate the dc component of circulating current.

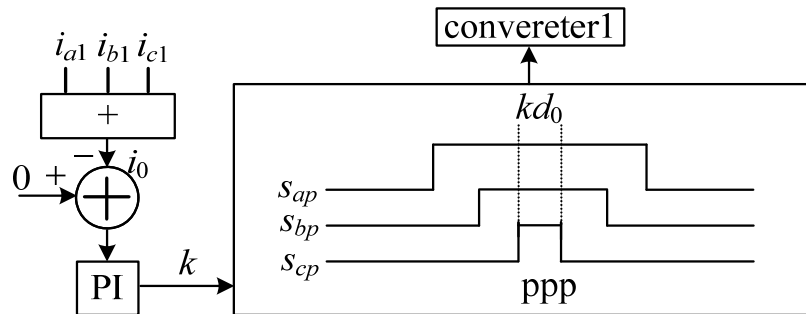


Fig.5 The control block diagram of the ZSCC Inhibition

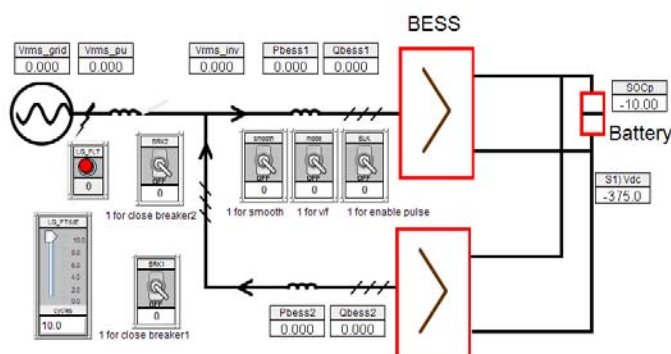
To achieve zero sequence current control, three current sensor is needed to detect the zero sequence current. In a two parallel converter system, it is easy to control one of the two converters since there is only one zero sequence current. For a system of n parallel converters, at least $n-1$ current sensor is needed to control the output power and circulation.

4. Simulation and experiment

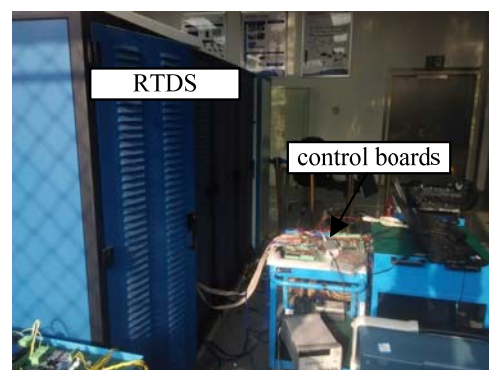
The hardware-in-the-loop HIL simulation and experiment share the same control scheme, control boards and relative parameters. DC bus voltage is 600V, output line voltage (rms) is 270V, output frequency is 50 Hz, switching and sampling frequency is 5 kHz, and the DSP is TMS320F28335 (TI).

The HIL simulation platform is shown in Fig. 6, control boards including the master control board, slave control board 1 and 2. The conventional SVPWM algorithm and the proposed control strategy (Fig. 5) are implemented in slave control boards 1 and 2, respectively. The three control boards are communicated with each other through CAN bus, and the two slave control boards receive pulse signal from master control board every few seconds to synchronize their carrier phase.

The slave board 1 and 2 operate and calculate the reference phase angle required for respective coordinate transformation independently, then produce their own SVPWM signals, which are sent to parallel converters models built in RTDS as gate pulses through the Gigabit Transceiver Digital Input Card (GTDI). The sampling time of RTDS is $50\mu s$.



(a) RTDS Schematic diagram of converters parallel system



(b) HIL simulation platform

Fig.6 Pictures of the simulation platform

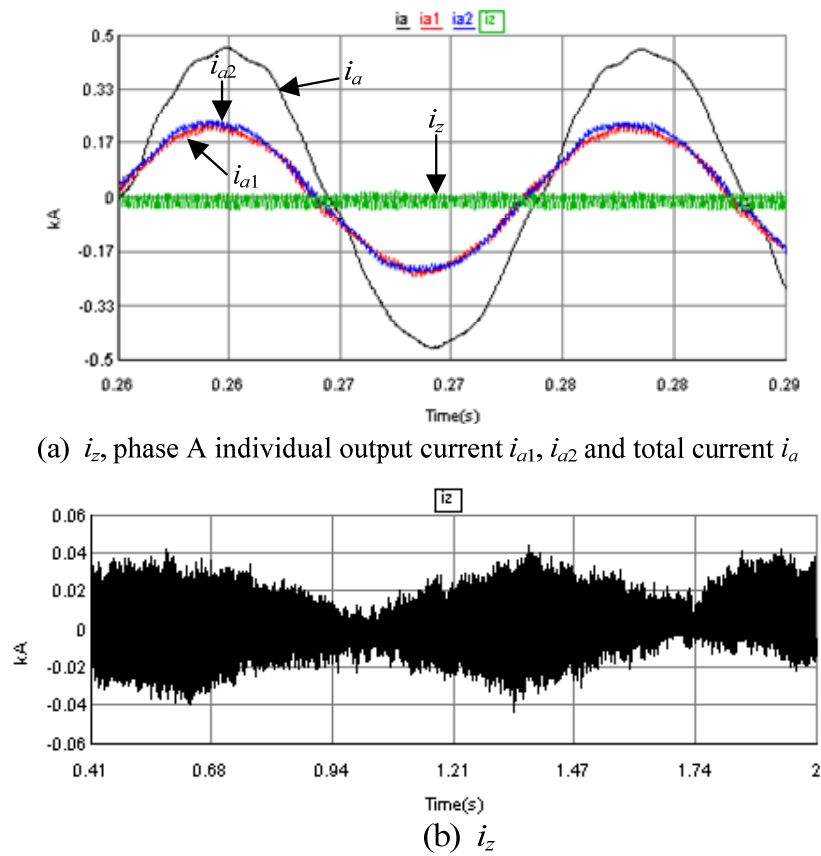
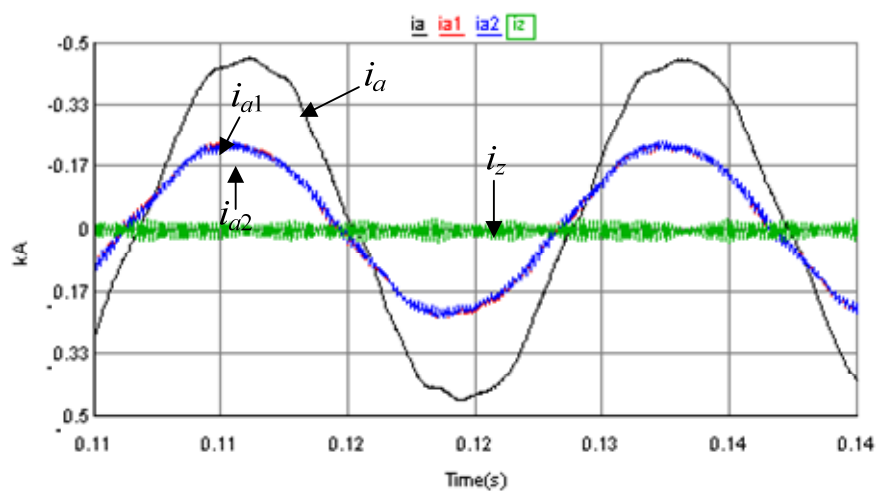


Fig.7 Simulation results of output current and ZSCC without ZSCC inhibition



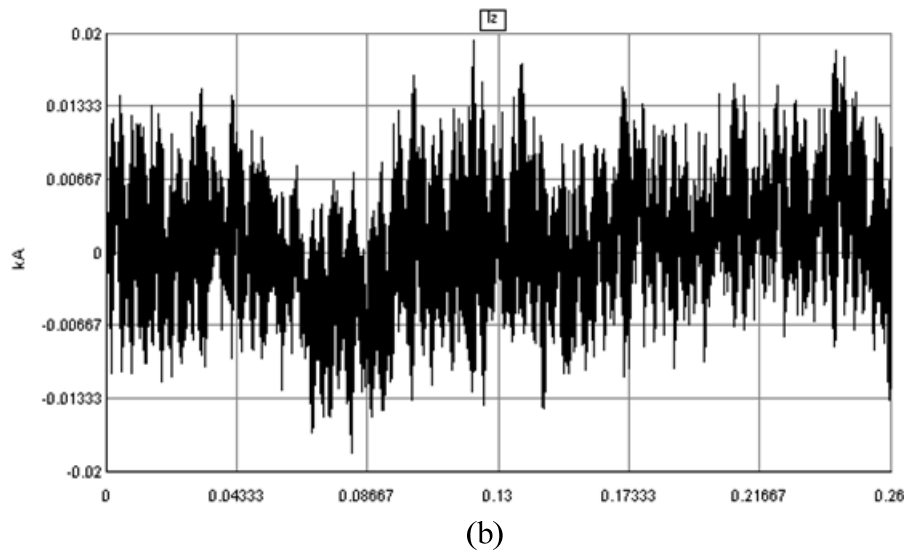
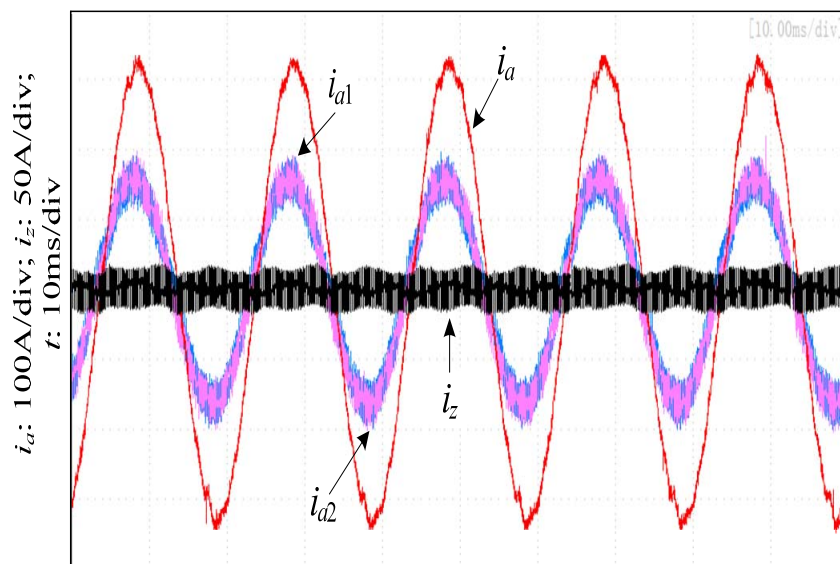


Fig. 8 Simulation results of output current and ZSCC with ZSCC inhibition

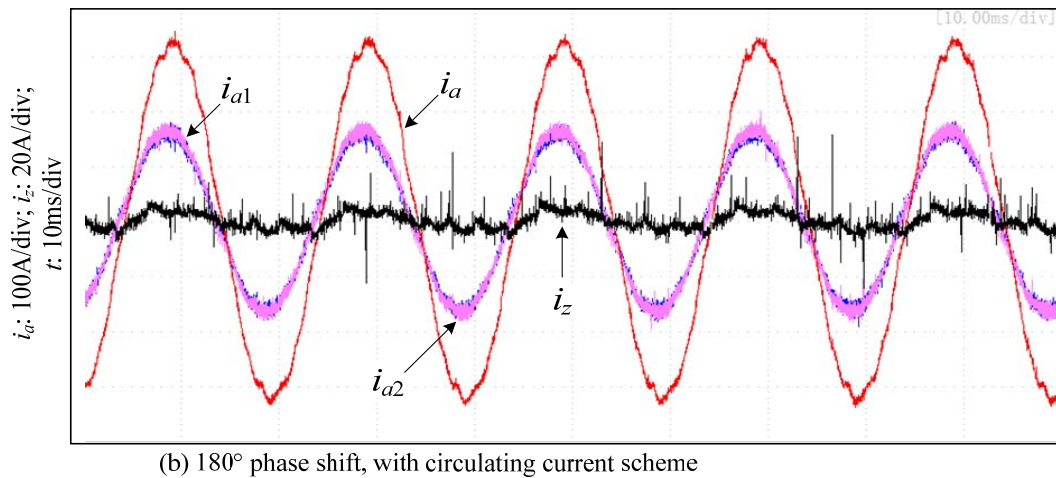
Fig. 7 is simulation results without ZSCC inhibition, and Fig. 8 is with ZSCC inhibition strategy in Fig. 6. The waveform of i_{a1} and i_{a2} is obviously different because of circulating current, as shown in Fig. 8(a). Fig. 8(b) shows that circulating current contains a low-frequency component. In Fig. 8, by applying the ZSCC control, the waveforms of i_{a1} and i_{a2} are basically coincidence, Fig. 10(b) shows that the circulating current is obviously reduced, which mainly contains high frequency components. The simulation results show that the proposed control strategy can suppress ZSCC.

5. Experiment

Fig. 9 is the current waveforms of converters stable parallel operation with 180° phase shift, without circulating current inhibition.



(a) 180° phase shift, without circulating current inhibition



(b) 180° phase shift, with circulating current scheme

Fig. 9 the experimental waveforms of output current and ZSCC

In Fig. 9(a), the rms current of i_{a1} , i_{a2} and i_a is 113.28A, 115.18A, 223.61A, respectively. The rms circulating current i_z is 38A, peak-to-peak value is 53A. Because of i_z , there is phase difference between i_a and i_{a1} (i_{a2}), which is about 1.7°. Fig. 9(b) is the waveforms employed the proposed ZSCC control scheme, the rms current of i_{a1} , i_{a2} and i_a is 117.28A, 119.18A, 234.28A, respectively. It is obvious that the proposed control strategy can suppress ZSCC effectively, the rms current i_z is 4.8A, bounded within 14A. The zero-crossing point of i_{a1} , i_{a2} and i_a are also the same. The proposed control scheme effect of ZSCC inhibition is outstanding.

6. Conclusion

This paper had addressed the issues of ZSCC inhibition for parallel three phase VSCs, and the cause and characteristic of ZSCC were studied. A zero-sequence current control strategy was proposed. The control strategy does not change the topologies of the circuit, it is easy to implement and modular design. The result shows that the proposed scheme successfully suppresses the ZSCC, confirms the good performance and promising features of the parallel system in the high power application.

Acknowledgments

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