Investigation of single-event transient mitigation via pulse quenching in logic circuits

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Abstract. A layout technique which can mitigate single-event effect via pulse quenching is tested in this paper. The new limitation of application of this layout technique is affirmed in 65nm technology. The layout design via pulse quenching has no effects in PMOS, but it can work in NMOS in basic logical circuits. Combinational logic circuits still can use this method to defense single-event effect.

1 Introduction

With the development of integrated circuits (ICs) technology, charge sharing is enhanced by the decreasing distance between devices. It leads to the occurrence of pulse quenching effect which can mitigate single-event effects [1-3].

Figure 1 shows the mechanism of pulse quenching. In this inverter chain, when logic state of Out2 is set to LOW and Out3 is HIGH, the collector junction of PMOS of Inv2 is reverse bias. If an ion strikes on the drain of PMOS of Inv2, the logic state of Out2 will turn to HIGH because the strike of ion can generate many free carriers and the reverse junction of PMOS of Inv2 will collect holes to drive the voltage of Out2 to high, and the logic state of Out3 will turn to LOW. This process is called single-event effect.
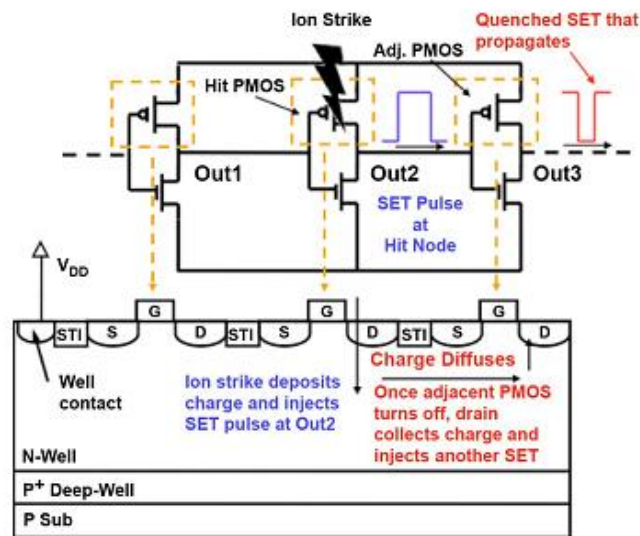
Figure 1: Pulse quenching in Inverter Chain [4]

When Out3 turns to LOW, the collector junction of PMOS of Inv3 will turn to reverse bias. If the distance between Inv2 and Inv3 is close enough, PMOS of Inv3 can collect enough holes and the logic state of Out3 will turn back to HIGH again. This process of the change of Out3 logic state is called pulse quenching effect.
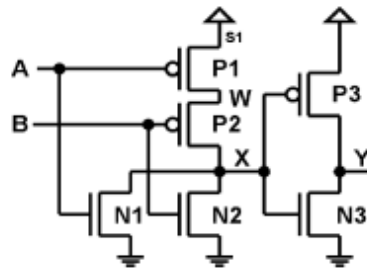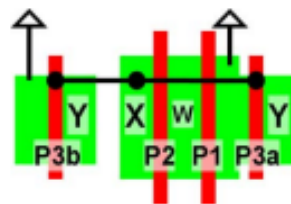

Figure 2: Schematic of OR [5]

Figure 3: Layout of OR gate PMOS that promotes charge sharing between nodes X and Y, i.e.., pulse quenching [5]

According to pulse quenching effect, paper [5] gave a layout technique to mitigate the single-event effect by adding redundant devices which can enhance charge diffusion to trigger pulse quenching in 90nm technology. Table 1 shows that PMOS transistors of OR gate are sensitive to single-event effect because the voltage of PMOS is reverse bias voltage when inputs are at 01, 10, 11 states. Figure 2 is a normal schematic of OR and Figure 3 is the improved layout of PMOS in OR. The structure of P1, P2 and P3a is the conventional PMOS layout of OR gate. P3b is a redundant structure which has the same structure and connection of P3a. The improved layout makes output Y easier to collect holes.

Table 1: Logic Sate in OR gate

Input(P1,P2)	Node X	Node Y
00	HIGH	LOW
01	LOW	HIGH
10	LOW	HIGH
11	LOW	HIGH

Two conditions are needed for this layout technology: (1) an inverting logic state, (2) the number of input states resulting in node voltages favorable to pulse quenching [5]. However, this layout technology can not work in 65nm technology.

2 Experiment of layout technique of basic logic circuits
To research this layout technique, devices are built in 3D TCAD simulations. Both TCAD models and Spice compact models are based on the 65nm CMOS technology. The length of the ion track is 10μm and the radius of ion is 0.05μm. Devices are built on a $10 \times 10 \times 10 \mu m^3$ substrate. The ion strikes at 500ps.

2.1 OR Gate of Conventional Layout
Showing in the Figure 4, the PMOS transistors of OR gate of normal layout are built as 3D model and the other models of transistors in Figure 2 use calibrated compact models. An ion strikes on the drain region (X) with LET = 40MeV·cm²/mg.
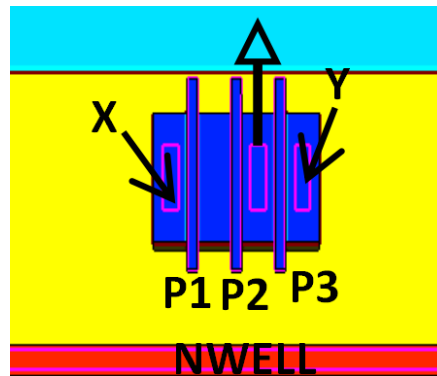

Figure 4: 3-D model of conventional layout of OR gate and nodes correspond to the schematic of Figure 2.
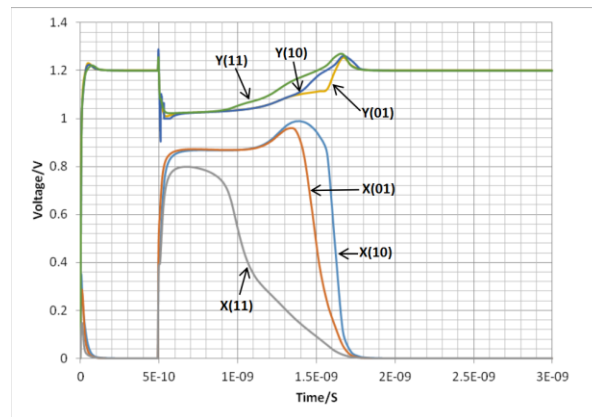

Figure 5: Voltage transients of node X and node Y during node X = LOW in conventional layout.

In the Figure 5, when node X turns from LOW to HIGH because of ion striking, node Y will keep HIGH. The normal OR gate layout shows obvious pulse quenching effect in 65nm technology. With the decreasing of distance between adjacent transistors, charge sharing is enhanced that pulse quenching effect is easier to be triggered.

The layout does not need the improved layout design in PMOS because charge sharing is strong enough to trigger pulse quenching effect. The improved layout design via pulse quenching is not suitable for PMOS in basic logic structure in 65nm technology.

2.2 Implementation of technique in AND Gate

Paper [5] only designed experiments for PMOS because pulse quenching is more sensitive in PMOS which has the isolated n-well. The isolated n-well makes charge sharing stronger because the isolated n-well can limit carriers to stay in n-well that the drain can collect carriers easier. The well of NMOS is connected to substrate, which causes that carriers can diffuse to substrate, so charge sharing is weaker in NMOS.

But in 65nm technology, the layout technology via pulse quenching can be implemented in NMOS because of the decreasing scaling of ICs. Charge diffusion is enhanced that if NMOS uses redundant transistors design, the drain of NMOS can collect enough carriers to trigger pulse quenching even if the well of NMOS is connected to substrate. For NMOS, when the logic of NMOS is HIGH, NMOS is at reverse bias state which can induce single-event effect. Showing in Table 2, NMOS of AND gate can use protective layout design because three quarters of node X states are HIGH. The 3D model of improved layout of NMOS of AND gate is showing in Figure 6.

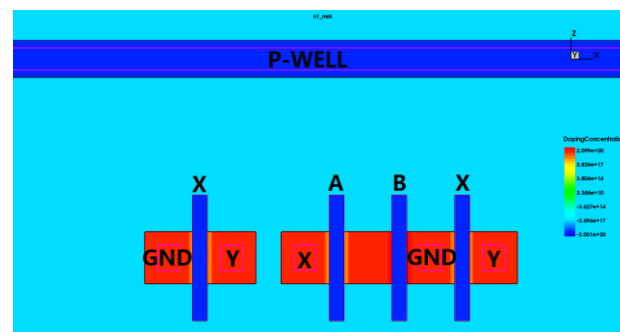| Input(N1,N2)	Node X	Node Y
00	HIGH	LOW
01	HIGH	LOW
10	HIGH	LOW
11	LOW	HIGH

Table 2: Logic State in AND gate

Figure 6: 3-D model of proposed layout of AND gate.

Contrasting conventional layout, Figure 8 shows that the pulse width of node Y of proposed layout has been shortened obviously. The layout technology via pulse quenching can be used in NMOS in 65nm technology because the increasing charge diffusion leads NMOS to collect enough carriers to induce pulse quenching effect.
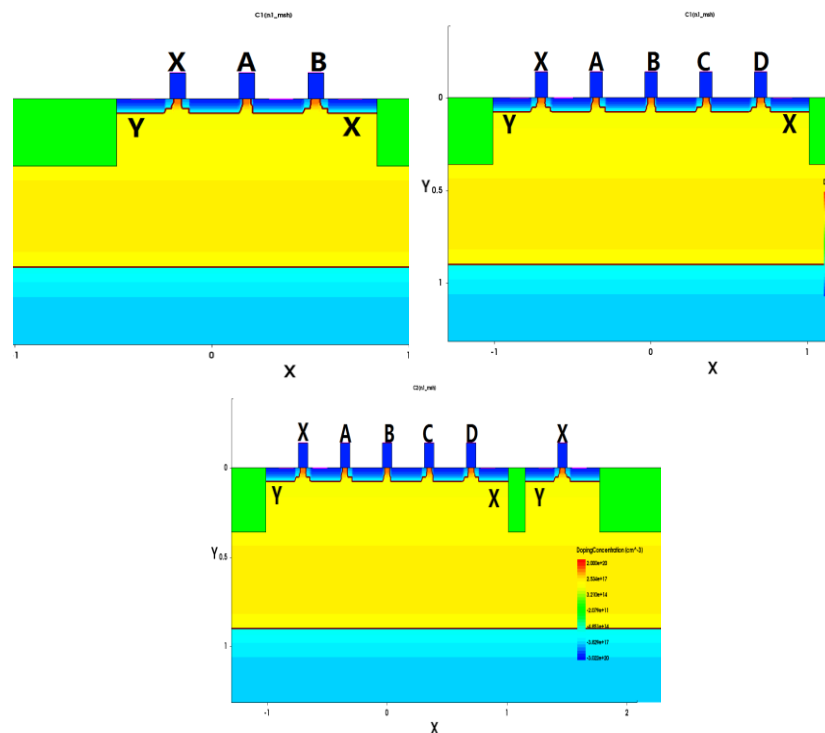
Figure 7: Cross-section view of 3D model of normal 2-input OR gate, 4-input OR gate and proposed 4-input OR gate in PMOS
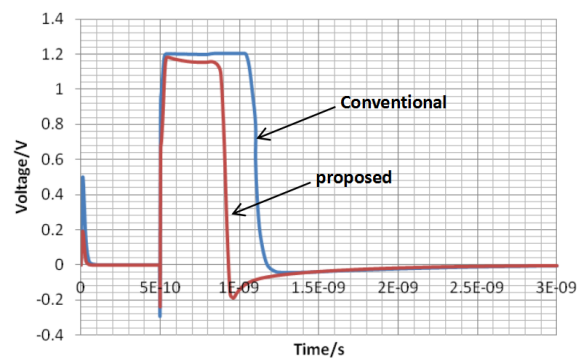

Figure 8: Voltage transients of node Y during input is 01

3 Experiment of layout technique of combinational logic circuits

In section 2, with the decreasing of scaling technology, a conclusion can be known that it does not need to use improved layout in PMOS in basic logic circuits, but this layout technology still can be implemented in combinational logic circuits. Figure 9 shows a 3D model of normal layout of 4-input OR gate in PMOS and the structure of 4-input AND gate in NMOS is similar to Figure 9 in P-WELL.
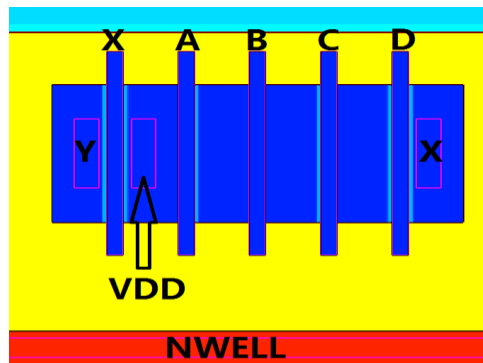
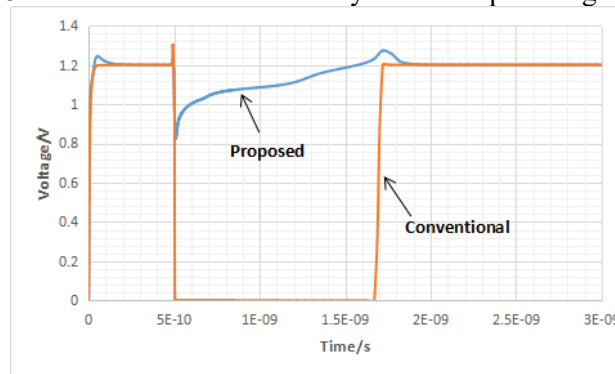Figure 9: 3-D model of conventional layout of 4-input OR gate in PMOS

Figure 10: Voltage transients of node Y during input is 1111 of 4-input OR while ion strikes on X region
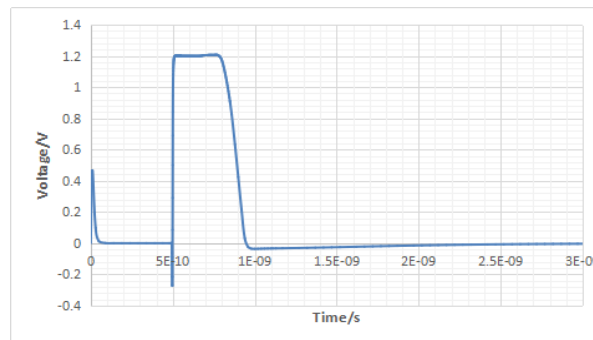

Figure 11: Voltage transients of node Y during input is 0000 of 4-input AND while ion strikes on X region

The voltage of node Y of conventional layout in figure.10 shows that conventional layout of 4-input OR gate can not defense single-event effect and figure.11 shows that 4-input AND gate in NMOS can not defense single-event effect either. Figure.7 can explain this phenomenon. In figure.7, the distance between node X (the drain area) and node Y of the normal layout of 4-input OR gate is longer than 2-input OR gate. Carriers in the node X are difficult to propagate to node Y in 4-input OR gate, so node Y can not collect enough carriers to trigger pulse quenching.

Contrasting to normal layout of 4-input OR gate, the improved layout makes node Y closer to node X (the drain area), so node Y can collect charge easily to trigger pulse quenching.
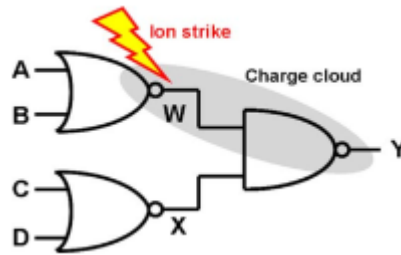
Figure 12: Gate-level implementation of 4-input OR [5]

Paper [5] presented that 4-input OR gate can be significantly hardened to against single-event effect by using NOR-NAND tree.

$$Y = \overline{W \cdot X} = \overline{\overline{(A+B)} \cdot \overline{(C+D)}} = A + B + C + D \quad (1)$$

From the equation, NOR-NAND tree structure is logic equivalent with the four input cascaded structure in PMOS. If Ion strikes on W when X = HIGH, node Y and node W can work as an inverter and the pulse can be quenched, and when X = LOW, node Y is locked at logic HIGH and node W is blocked whether ion strikes or not.

The protective ability of NOR-NAND tree structure is based on two ways. The first way is that one node stays on LOW while another node is struck. The second way is that one node stays on HIGH while another node is struck to trigger pulse quenching.

But the probability of area where is struck by ion is equal. If node W, X = 01 or 10 when the ion strikes on the zero state node, W, X will turn to 11 and node Y will turn to 0. Showing in the Figure 13, although node Y is at the middle of node X and node W, the distance between node Y and node X (or node W) is so long that node Y can not collect enough carriers to trigger pulse quenching and node Y will stay at zero state. From Table 3, the probability of node W, X = 01 or 10 is 6/16.

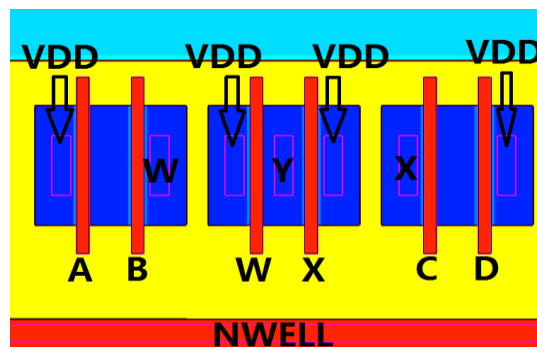| Node X	Node W	Node Y	Probability
0	0	1	9/16
0	1	1	3/16
1	0	1	3/16
1	1	0	1/16

Table 3: Logic State in OR gate

Figure 13: 3-D model of normal layout of NOR-NAND tree of 4-input OR gate

The improved layout of 4-input OR gate is showing in Figure 7. It shows that node Y can trigger pulse quenching easily because of the short distance of adjacent devices and node Y has high probability to trigger pulse quenching because node X has fifteen reverse bias states in all sixteen states. So the combinational logic circuits still need the improved layout technology in PMOS.

4 Summary

In basic logic circuits, the improved layout via pulse quenching is not suitable in PMOS because the conventional layout of PMOS of OR gate has short enough distance between adjacent transistors to collect carriers to induce pulse quenching in 65nm technology. But this technology can be implemented in NMOS in 65nm technology because charge diffusion is enhanced that NMOS can collect enough carriers to trigger pulse quenching even if the well of NMOS is connected to substrate that carriers will diffuse to everywhere not only to drain area. In the combinational logic circuits, the layout technology is still useful in PMOS, so we can implement this technology to induce pulse quenching to defense single-event effect.

Acknowledgments

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