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Modeling and Control of Peak Current Mode Non-ideal Buck Converter

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Modeling and Control of Peak Current Mode Non-ideal Buck Converter

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Abstract. Based on the energy conservation method and the average modeling method of switching elements, considering the non-ideal parameters of the actual circuit, the whole peak current mode control non-ideal Buck converter system model is established. On this basis, for the equivalent power level, there are still some problems such as slow response speed and poor stability. A voltage controller compensation method is proposed and a system model including voltage controller compensation network is established. Through the analysis of the model and the simulation in Matlab, it can be seen that the model is intuitive and clear in physical meaning, which can more accurately reflect the working condition of the actual circuit. The designed voltage controller can improve the performance of the converter and can be DC-DC. The design of the converter system control circuit provides a theoretical basis.

1. Introduction

As DC-DC converter systems are widely used in portable electronic devices, the deviation between the ideal model and the actual circuit is a problem that cannot be ignored in the modeling of DC-DC converters, the complete model of the DC-DC converter and its control system is of great significance for the analysis and design of the switching power supply. Therefore, it is necessary to establish a non-ideal small-signal model closer to the actual circuit to design the stability and dynamic small-signal characteristics of the converter and the compensation network to ensure that the system can meet the performance and reliability design requirements, thus better guide the design of the power management chip.

At present, there are many achievements in the modeling research of peak current mode control DC-DC converter [1-5]. Among them, the reference [1] establishes the AC small signal model of the peak current mode control Buck converter, but does not consider the current loop. The current sampling behavior of the path causes the converter to exhibit double period instability and additional phase delay near the 1/2 switching frequency. The reference [2] considers the effect of the current sampling behavior of the current loop on the circuit, but its modeling of the power stage and voltage loop is not intuitive enough. The reference [3], a complete small-signal model of the peak current mode Buck converter is established, and the stability compensation scheme is designed, but the PID controller is not used. In reference [4] establishes a model at high frequencies. The literature [5] uses the state space average modeling method, and the model is not intuitive enough. At the same time, the reference [1-5] does not consider the influence of non-ideal factors such as the equivalent parasitic

parameters of various components and the inductor current ripple in the actual circuit. The ideal model and its control method are established.

Based on the reference [1-5], considering the effects of non-ideal factors such as equivalent parasitic parameters and inductor current ripple, the energy conservation method [6] and the switching element average model method [1, 7] The combination of ideas and consideration of the effects of output current fluctuations on circuit performance establishes a peak current mode non-ideal Buck converter that includes a complete small-signal model of the power stage and control stage. On the basis of this, for the equivalent power level after the slope compensation is introduced, there are still problems such as slow response speed and poor stability, and the PID controller is designed to compensate. The model built in this paper is universal for the non-ideal Buck converter with peak current mode under continuous conduction mode (CCM). The voltage controller compensation scheme is for single zero and double pole system control.

2. Non-ideal Buck Converter Small Signal Modeling

2.1. Peak current mode control Buck converter
The peak current mode control is a two-loop control system with a current inner loop and a voltage outer loop. It uses the output signal of the voltage outer loop as the control quantity, and uses the peak value of the current flowing through the power switch tube as the feedback amount, and the power level constitutes the current inner loop. A control mode. Figure 1 shows the peak current mode control Buck converter, which is divided into three parts: power stage, peak current control stage and voltage control stage. The power stage and peak current control stage are also collectively referred to as the equivalent power level.
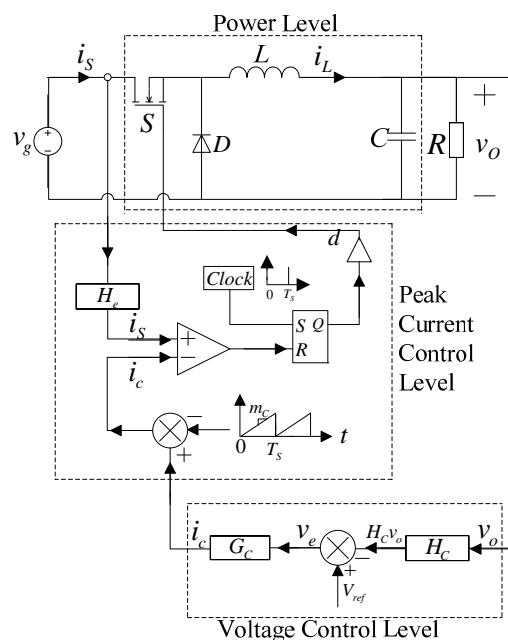

Figure 1. Peak current mode control Buck converter

2.2. Non-ideal Buck converter power level modeling
Figure 2 shows a Buck converter considering non-ideal parasitic parameters. The active switching power MOSFET is equivalent to the series connection of the ideal switch S and the on-resistance R_S. The diode D is equivalent to the ideal switch D, the forward voltage drop V_D and the series connection of the on-resistance R_D, R_L and R_C are the equivalent series resistances of the filter

inductor L and the filter capacitor C, respectively. Assuming that the switching period of the switching element S is T_S and the on-time is T_{on}, the duty ratio $D = T_{on}/T_S$.
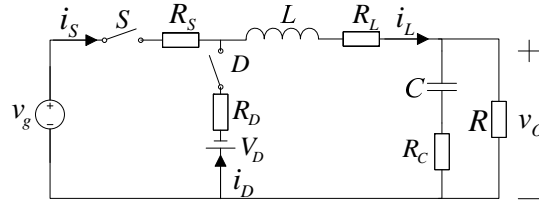

Figure 2. Non-ideal Buck converter considering parasitic parameters

In the CCM mode, considering the influence of the inductor current ripple, according to the energy conservation method, the parasitic parameters V_D, R_D, R_S, R_L of the switching elements in Figure 2 can be equivalent to the inductance branch, and the equivalent average voltage and the resistances are:

$$V_E = (1-D)V_D \tag{1}$$

$$R_E = \left[R_L + DR_S + (1-D)R_D\right]\left(1 + \frac{\Delta i_L^2}{3I_L^2}\right) \tag{2}$$

Therefore, combining the equations (1) and (2), according to the average model method of the switching element, the power switch S is replaced by the controlled current source di_L, and the passive switch D is replaced by the controlled voltage source dv_g, so that the non-ideal Buck converter can be obtained. The large signal average equivalent circuit model under CCM is shown in Figure 3.
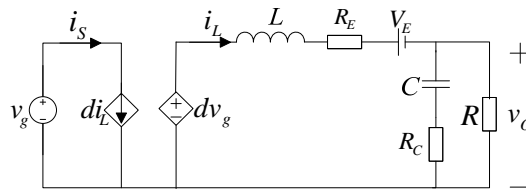
Figure 3. Large-signal average equivalent circuit model of non-ideal Buck converter under CCM

Ignore the small signal disturbance. In Figure 3, let $v_g = V_g = $ Vg, $v_o = V_o$, $d = D$, $di_L = DI_L$, $dv_g = DV_g$, and make the inductor L short, capacitor C is open. Also assume that under ideal conditions, the ideal transformer can convert DC, and the ideal voltage transformer can be used to replace the controlled voltage source and the controlled current source. Therefore, the steady-state value D of the duty cycle d can be expressed as:

$$D = V_O - V_D + (R_L + R_D)I_L \cdot \left(1 + \frac{\Delta i_L^2}{3I_L^2}\right) \Big/ V_g + V_D + (R_D - R_S)I_L \cdot \left(1 + \frac{\Delta i_L^2}{3I_L^2}\right) \tag{3}$$

Where, $I_L = \dfrac{V_O}{R}$.

The parameters in Figure 3 are separated and disturbed to be equal to the sum of the corresponding DC component and the AC small signal component, that is $v_g = V_g + \hat{v}_g$, $i_L = I_L + \hat{i}_L$, $v_o = V_o + \hat{v}_o$ and $d = D + \hat{d}$, and the two nonlinear controlled source parameters are separated and disturbed as:

$$\begin{cases} di_L = \left(D + \hat{d}\right)\left(I_L + \hat{i}_L\right) = DI_L + D\hat{i}_L + I_L\hat{d} + \hat{d}\hat{i}_L \\ dv_g = \left(D + \hat{d}\right)\left(V_g + \hat{v}_g\right) = DV_g + D\hat{v}_g + V_g\hat{d} + \hat{d}\hat{v}_g \end{cases} \tag{4}$$

Let the converter satisfy the small signal hypothesis, that is, $\left|\hat{v}_g\right| << V_g$, $\left|\hat{i}_L\right| << I_L$, $\left|\hat{v}_o\right| << V_o$ and $\left|\hat{d}\right| << D$, the quadratic product terms $\hat{d}\hat{i}_L$ and $\hat{d}\hat{v}_g$ of the AC small signal are second-order micro-quantities, which are negligible and remove the DC component in the above equations. The linearized AC small-signal equivalent circuit of the non-ideal Buck converter in CCM mode as shown in Figure 4 can be obtained.
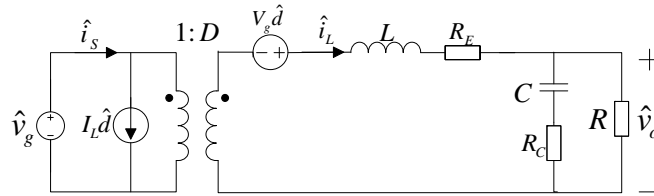
Figure 4. AC small signal equivalent circuit model of non-ideal Buck converter under CCM

It can be seen from Figure 4 that the expressions of the transfer functions of the Buck converter power level under non-ideal conditions are:

$$G_{vg}(s) = \frac{\hat{v}_o(s)}{\hat{v}_g(s)}\Bigg|_{\hat{d}(s)=0} = \frac{DR}{R + R_E} \cdot \left(1 + \frac{s}{\omega_{z1}}\right) \Bigg/ \left[1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right] \tag{5}$$

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}\Bigg|_{\hat{v}_g(s)=0} = \frac{V_g R}{R + R_E} \cdot \left(1 + \frac{s}{\omega_{z1}}\right) \Bigg/ \left[1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right] \tag{6}$$

$$G_{ig}(s) = \frac{\hat{i}_L(s)}{\hat{v}_g(s)}\Bigg|_{\hat{d}(s)=0} = \frac{D}{R + R_E} \cdot \left(1 + \frac{s}{\omega_{z2}}\right) \Bigg/ 1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2 \tag{7}$$

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)}\Bigg|_{\hat{v}_g(s)=0} = \frac{V_g}{R + R_E} \cdot \left(1 + \frac{s}{\omega_{z2}}\right) \Bigg/ \left[1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right] \tag{8}$$

$$Z_o(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)}\Bigg|_{\hat{v}_g(s)=0, \hat{d}(s)=0} = \frac{RR_E}{R + R_E} \cdot \left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z3}}\right) \Bigg/ 1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2 \tag{9}$$

$$G_{iz}(s) = \left.\frac{\hat{i}_L(s)}{\hat{i}_o(s)}\right|_{\hat{v}_g(s)=0,\hat{d}(s)=0} = \frac{R}{R+R_E}\cdot\left(1+\frac{s}{\omega_{z1}}\right)\bigg/ 1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2 \tag{10}$$

In the equations (5)-(10), the free resonance frequency $\omega_0 = \sqrt{\dfrac{R+R_E}{(R+R_C)LC}}$, the quality factor

$Q = \dfrac{\sqrt{(R+R_E)(R+R_C)LC}}{RR_EC+RR_CC+R_ER_CC+L}$, the zero points $\omega_{z1} = \dfrac{1}{R_CC}$, $\omega_{z2} = \dfrac{1}{(R+R_C)C}$, $\omega_{z3} = \dfrac{R_E}{L}$.

$Z_o(s)$ is the open-loop output impedance, $G_{iz}(s)$ is the transfer function of the inductor current $\hat{i}_L(s)$ to the output current $\hat{i}_o(s)$, and equations (9) and (10) reflect the effect of output current ripple on the circuit performance.

Therefore, the expressions of the inductor current average disturbance amount $\hat{i}_L(s)$ and the output voltage average disturbance amount $\hat{v}_o(s)$ are:

$$\hat{i}_L(s) = G_{id}(s)\hat{d}(s) + G_{ig}(s)\hat{v}_g(s) + G_{iz}(s)\hat{i}_o(s) \tag{11}$$

$$\hat{v}_o(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) + Z_o(s)\hat{i}_o(s) \tag{12}$$

2.3. Modeling of peak current control loop for non-ideal Buck converter
During the entire switching cycle, the inductor current average expression [1] is:

$$\bar{i}_L(t) = \bar{i}_C(t) - m_C dT_S - \frac{m_1 d^2 T_S}{2} - \frac{m_2 d'^2 T_S}{2} \tag{13}$$

Where, $\bar{i}_C(t)$ is the average of the output of the voltage control loop as the control signal of the peak current control loop, and m_C is the slope of the peak current control section slope compensation signal. Reference [8] illustrates the necessity of slope compensation for peak current mode control of the Buck converter when the duty cycle D > 0.5.

The small signal separation perturbation of each variable in equation (13) [9-13], and note that after considering the non-ideal factors, the slopes of the inductor current in the rising phase ($t \in [0, dT_S]$) and the falling phase ($t \in [dT_S, T_S]$) are:

$$m_1 = \left[v_g - v_o - \bar{i}_L(R_S + R_D)\right]\big/ L \tag{14}$$

$$m_2 = \left[v_o + V_D + \bar{i}_L(R_D + R_L)\right]\big/ L \tag{15}$$

By performing small signal perturbation [14] on the above slope, the DC component and AC component of the slope of the inductor current can be obtained as follows:

$$\begin{cases} M_1 = \left[V_g - V_O(1+K_1)\right]\big/ L \\ M_2 = \left[V_O(1+K_2) + V_D\right]\big/ L \end{cases} \tag{16}$$

$$\begin{cases} \hat{m}_1 = \left[\hat{v}_g - \hat{v}_o(1+K_1)\right]/L \\ \hat{m}_2 = \hat{v}_o(1+K_2)/L \end{cases} \tag{17}$$

Where: $K_1 = (R_S + R_L)/R$, $K_2 = (R_D + R_L)/R$

Therefore, an expression of the duty cycle $\hat{d}(t)$ can be obtained:

$$\hat{d}(t) = F_m[\hat{i}_c(t) - \hat{i}_L(t) - F_g\hat{v}_g(t) - F_v\hat{v}_o(t)] \tag{18}$$

Where, considering the non-ideal factors of the converter, the correction coefficients are $F_m = \dfrac{1}{(M_1 + M_C)T_S}$, $F_g = \dfrac{D^2 T_S}{2L}$ and $F_v = \dfrac{(1-2D)T_S}{2L} + \dfrac{(1-2D)K_2 + D^2(K_2 - K_1)}{2L}T_S$, $\hat{i}_c(t)$ is the control signal disturbance amount of the current control loop, and F_g and F_v respectively represent the influence coefficients of the input and output voltage disturbance amounts on the duty ratio.

The s-domain expressions of equations (11), (12), and (18) are available:

$$\hat{v}_o(s) = G_{vc}(s)\hat{i}_C(s) + A(s)\hat{v}_g(s) + Z(s)\hat{i}_o(s) \tag{19}$$

Where, $G_{vc}(s)$ is the transfer function of the equivalent current level of the peak current mode control Buck converter.

$$G_{vc}(s) = \left.\frac{\hat{v}_o(s)}{\hat{i}_C(s)}\right|_{\hat{v}_g(s)=0} = \frac{F_m G_{vd}(s)}{1 + F_m[G_{id}(s) + F_v G_{vd}(s)]} \tag{20}$$

Based on the two models represented by the above equations (11), (12) and (18), considering the voltage control loop model of the literature [1] and the current sampling behavior model of the literature [2], it is possible to establish a power level including The peak current control stage and the CCM peak current mode of the voltage control stage control the complete AC small signal model of the non-ideal Buck converter, as shown in Figure 5. Among them, $H_e(s)$ represents the current sampling function; $H_C(s)$ is the output voltage sampling function of the voltage controller, and $G_C(s)$ is the transfer function of the voltage controller compensation network.
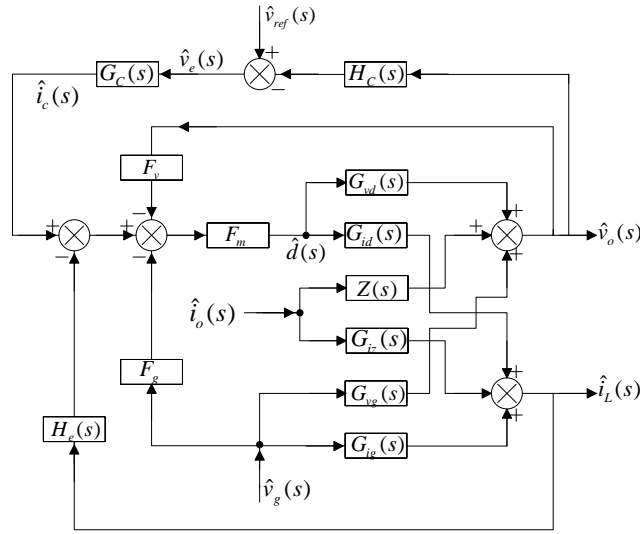
Figure 5. Complete AC small-signal model of non-ideal Buck converter with peak current mode control under CCM

3. Model analysis and voltage controller design

3.1. Current loop analysis

In Figure 5, the voltage loop is turned off, that is, the output voltage disturbance amount $\hat{v}_o(s) = 0$, and the input voltage disturbance amount $\hat{v}_g(s) = 0$, the current loop gain can be obtained as:

$$T_i(s) = F_m G_{id}(s) H_e(s) = \frac{1}{(1 + M_c/M_1)T_s} \cdot \frac{L}{D'R} \cdot \frac{1 + \dfrac{s}{\omega_{z2}}}{1 + \dfrac{s}{Q\omega_0} + \left(\dfrac{s}{\omega_0}\right)^2} \cdot \left(1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}\right) \tag{21}$$

Where, the current sampling function: $H_e(s) = 1 + \dfrac{s}{\omega_n Q_z} + \dfrac{s^2}{\omega_n^2}$, $\omega_n = \dfrac{\pi}{T_s}$, $Q_z = -\dfrac{2}{\pi}$.

The current loop gain of equation (21) consists of three zeros and two poles, where the two zero points provided by the current sampling function are the right half-plane conjugate complex zero near the 1/2 switching frequency, which is the two zero points. It is verified that the current loop gain exhibits period-doubling instability and phase delay near the 1/2 switching frequency. It can be seen from the analysis of equation (21) that even in the case of $D < 1/2$, if the gain of the current loop is relatively large, there is still the possibility of instability, and by introducing slope compensation, the current loop can be reduced. The gain, so that the 1/2 switching frequency is outside the crossing frequency of the loop gain $T_i(s)$ of the current loop, stabilizes the current loop. It can also be seen that the variation of the load R also affects the stability of the current loop. The gain of the current loop is very small under no-load or light-load conditions.

3.2. Voltage loop analysis

In Figure 5, the current loop is turned off, that is, the inductor current disturbance amount $\hat{i}_L(s) = 0$, the loop gain of the voltage loop can be obtained, that is, the open-loop transfer function of the system is:

$$T_V(s) = H_C(s) G_C(s) G_{vc}(s) \tag{22}$$

By taking equations (6) and (8) into equation (20), the expression of the transfer function of the equivalent power level can be found as:

$$G_{vc}(s) = G_{vc0}\left(1+\frac{s}{\omega_{z1}}\right)\bigg/\left[1+\frac{s}{Q_c\omega_c}+\left(\frac{s}{\omega_c}\right)^2\right] \tag{23}$$

Where, $G_{vc0} = F_m V_g R/(R+R_E+F_m V_g+F_m F_v V_g R)$, $\omega_c = \omega_0 \cdot \sqrt{R+R_E+F_m V_g+F_m F_v V_g R}\big/\sqrt{R+R_E}$,

$Q_c = \sqrt{(R+R_E)(R+R_E+F_m V_g+F_m F_v V_g R)}\bigg/\left(\dfrac{R+R_E}{Q}+\dfrac{F_m V_g \omega_0}{\omega_{z2}}+\dfrac{F_m F_v V_g R\omega_0}{\omega_{z1}}\right)$, $\omega_{z1}=\dfrac{1}{R_C C}$.

In general, the peak current mode control Buck converter satisfies $Q_c \le 0.5$, the transfer function $G_{vc}(s)$ has two real poles, the low frequency pole angle frequency is defined as ω_{pl}, and the high frequency pole angle frequency is ω_{ph}.

$$\begin{cases} \omega_{pl} = (\omega_c/Q_c)\cdot\left(1-\sqrt{1-4Q_c^2}\right)\big/2 \\ \omega_{ph} = (\omega_c/Q_c)\cdot\left(1+\sqrt{1-4Q_c^2}\right)\big/2 \end{cases} \tag{24}$$

Therefore, the peak current mode control Buck converter equivalent power level transfer function expression can be rewritten as:

$$G_{vc}(s) = G_{vc0}\left(1+\frac{s}{\omega_{z1}}\right)\bigg/\left[\left(1+\frac{s}{\omega_{pl}}\right)\left(1+\frac{s}{\omega_{ph}}\right)\right] \tag{25}$$

It can be seen from equation (25) that the peak current mode control Buck converter equivalent power level transfer function contains a zero point and two real poles, and the system dynamic response is slow and the stability is poor, a suitable voltage controller must be designed to compensate for improved converter performance.

3.3. Voltage Controller Structure Design

According to the peak current mode shown in equation (25), the characteristic of the equivalent power stage transfer function $G_{vc}(s)$ of the Buck converter is controlled. It includes two poles and one zero. Assuming $\omega_{pl} < \omega_{z1} < \omega_{ph}$, The typical amplitude-frequency characteristic and phase-frequency characteristic of GS are shown in Figure 8:
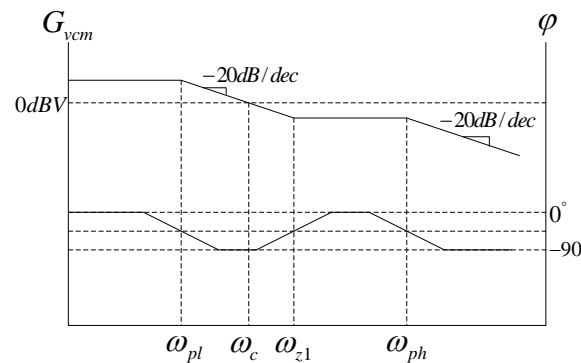
Figure 6. Schematic diagrams of $G_{vc}(s)$ amplitude-frequency characteristics and phase-frequency characteristics

It can be seen from Figure 6 that the curve in the low frequency band of the amplitude-frequency characteristic is flat, and the closed-loop system has a steady-state error. It is necessary to add an integral link in the voltage controller to reduce the amplitude-frequency characteristic of the low-frequency band by a slope of $-20dB/dec$. Thus, the steady-state error of the system is equal to zero; after increasing the integral link, the phase lag is 90°. In order to cancel the phase of the lag, a zero point ω_{z-1} needs to be introduced in the middle of the middle frequency band; in order to offset the zero point ω_{z1}, need to set a pole ω_{p-1} in the voltage controller; the high frequency pole f_{ph} of the equivalent power stage transfer function $G_{vc}(s)$ of the Buck converter is generally larger based on the peak current mode. If the f_{ph} is greater than the compensated crossing frequency, the amplitude frequency characteristic of the high frequency band of the system decreases by a slope of $-40dB/dec$. It can guarantee the high frequency anti-interference ability of the system. Therefore, a voltage controller as shown in Figure 7 can be designed, which is a PID controller.
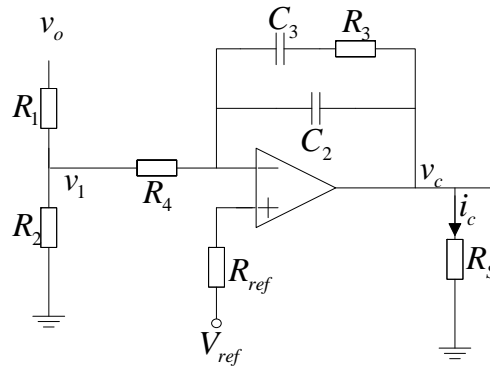
Figure 7. Voltage controller

In Figure 7, R_1 and R_2 form the output voltage sampling network and the remaining part constitutes the voltage compensation network. The transfer function of the voltage controller can be obtained as follows:

$$G_v(s) = H_C(s) \cdot G_C(s) = G_{v0}\left(1 + \frac{s}{\omega_{z-1}}\right) \bigg/ \left[s\left(1 + \frac{s}{\omega_{p-1}}\right)\right] \tag{26}$$

Where, $G_{v0} = \dfrac{R_2}{(R_1 + R_2)R_S R_4 (C_2 + C_3)}$, $\omega_{z-1} = \dfrac{1}{R_3 C_3}$, $\omega_{p-1} = \dfrac{C_2 + C_3}{R_3 C_2 C_3}$. At this point, combined with equations (25) and (26), the system open-loop transfer function can be obtained as:

$$T_V(s) = G_{v0}G_{vc0} \cdot \frac{1 + \dfrac{s}{\omega_{z-1}}}{s \cdot \left(1 + \dfrac{s}{\omega_{pl}}\right)} \cdot \frac{1 + \dfrac{s}{\omega_{z1}}}{1 + \dfrac{s}{\omega_{p-1}}} \cdot \frac{1}{1 + \dfrac{s}{\omega_{ph}}} \tag{27}$$

3.4. Voltage Controller Parameter Design

The parameters of the Buck converter in the design example chosen in this paper are: $V_g = 15V$, $V_o = 10V$, $R = 10\Omega$, $L = 127\mu H$, $R_L = 0.72\Omega$, $C = 247\mu F$, $R_C = 20m\Omega$, $R_S = 10m\Omega$,

$R_D = 30m\Omega$, $V_D = 0.45V$, inductor current ripple $\Delta i_L = 0.06A$, switching frequency $f_S = 200kH_Z$.

Therefore, the parameters of the model can be calculated as: $I_L = 1A$, $D = 0.7240$, $R_E = 0.7364\Omega$, $M_1 = 3.362 \times 10^4$, $M_2 = 8.819 \times 10^4$, $F_m = 2.005$, $F_v = -0.0473$, $F_g = 0.0103$, $Q_C = 0.3818$.

Since $D = 0.7240 > 0.5$, the slope compensation slope $M_C = 0.75M_2 = 6.614 \times 10^4$ is taken. The equivalent power level transfer function $G_{vc}(s)$ satisfies $Q_C = 0.3818 < 0.5$, which verifies that the derivation from equation (23) to equation (25) is reasonable.

According to the above parameters, and equations (23)-(25), the $G_{vc}(s)$ can be obtained as:

$$G_{vc}(s) = 11.31 \times \frac{1 + \dfrac{s}{2.024 \times 10^5}}{\left(1 + \dfrac{s}{351.6}\right) \cdot \left(1 + \dfrac{s}{2.405 \times 10^5}\right)} \tag{28}$$

It can be obtained by equation (28), low frequency pole $f_{pl} = \omega_{pl}/2\pi = 55.96H_Z$, high frequency pole $f_{ph} = 0.3828 \times 10^5 H_Z = 0.1914 f_S$, crossing frequency $\omega_c = 3.962 \times 10^3 \, rad/s$, $f_c = \omega_c/2\pi = 630.6H_Z$, and phase margin $\varphi_m = 95.25°$. Therefore, there are problems such as too low crossing frequency, slow system response speed, excessive phase margin, and affecting system dynamic performance. It is verified that the voltage controller must be set to compensate.

After adding the voltage controller, the crossover frequency f_c of the open loop transfer function $T_V(s)$ is designed to be $1/20$ of the switching frequency f_S , namely:

$$f_c = f_S/20 = 10kH_Z \tag{29}$$

$$\omega_c = 2\pi f_c = 6.283 \times 10^4 \, rad/s \tag{30}$$

At this time, the crossing frequency satisfies $f_c = f_S/20 < 0.1914 f_S = f_{ph}$, and the crossing frequency is much smaller than the high-frequency pole f_{ph} of the transfer function $G_{vc}(s)$ of the equivalent power level, so the design of Figure 7 is reasonable. In Figure 7, the reference voltage $V_{ref} = 5V$ is passed. The steady-state current of the voltage sampling network is $1m$A, then:

$$R_1 = R_2 = 5k\Omega \tag{31}$$

At this point, the system open loop transfer function is:

$$T_V(s) = G_{v0}G_{vc0} \cdot \frac{(1 + \dfrac{s}{\omega_{z-1}})}{s(1 + \dfrac{s}{\omega_{pl}})} \cdot \frac{(1 + \dfrac{s}{\omega_{z1}})}{(1 + \dfrac{s}{\omega_{p-1}})} \cdot \frac{1}{(1 + \dfrac{s}{\omega_{ph}})} \tag{32}$$

Where, $\omega_{pl} \le \omega_{z-1} < \omega_c < \omega_{p-1} \le \omega_{z1} < \omega_{ph}$.

Assuming the compensated phase margin $\varphi_m = 55^\circ$, the zero and pole frequencies of the voltage controller are:

$$\begin{cases} f_{z-1} = f_c\sqrt{\dfrac{1-\sin\varphi_m}{1+\sin\varphi_m}} = 3.153kH_Z \Rightarrow \omega_{z-1} = 1.981\times10^4\, rad\,/\,s \\[4mm] f_{p-1} = f_c\sqrt{\dfrac{1+\sin\varphi_m}{1-\sin\varphi_m}} = 31.76kH_Z \Rightarrow \omega_{p-1} = 1.993\times10^5\, rad\,/\,s \end{cases} \tag{33}$$

When the frequency is the crossing frequency ω_c , the amplitude-frequency characteristic of the open-loop transfer function $T_V(s)$ is $0dB$. According to the equation (32), the parameters in the equations (28), (30), and (33) are brought in:

$$G_{v0} = 3.089\times10^5 \tag{34}$$

Therefore, the system open loop transfer function is:

$$T_V(s) = 3.494\times10^6 \times \frac{(1+\dfrac{s}{1.981\times10^4})}{s(1+\dfrac{s}{351.6})} \cdot \frac{(1+\dfrac{s}{2.024\times10^5})}{(1+\dfrac{s}{1.993\times10^5})} \cdot \frac{1}{(1+\dfrac{s}{2.405\times10^5})} \tag{35}$$

Combining equation (26), the parameters in Figure 7 can be taken as: $R_3 = 50k\Omega$, $C_3 = 1nF$, $C_2 = 0.11nF$, $R_4 = 1.5k\Omega$, $R_S = 1\Omega$, When the voltage controller adopts the above parameters, the transfer function of the actual voltage controller is:

$$G_v(s) = 3.089\times10^5 \times \frac{1+\dfrac{s}{20000}}{s(1+\dfrac{s}{2.018\times10^5})} \tag{36}$$

The actual system open loop transfer function is:

$$T_V(s) = 3.396\times10^6 \times \frac{(1+\dfrac{s}{20000})}{s(1+\dfrac{s}{351.6})} \cdot \frac{(1+\dfrac{s}{2.024\times10^5})}{(1+\dfrac{s}{2.018\times10^5})} \cdot \frac{1}{(1+\dfrac{s}{2.405\times10^5})} \tag{37}$$

It can be found that the crossover frequency $\omega_c = 6.090\times10^4\, rad\,/\,s$, $f_c = \dfrac{\omega_c}{2\pi} = 9.693kH_Z$, phase margin $\varphi_m = 57.89^\circ$, crossover frequency and phase margin of the open-loop transfer function of the system reach a satisfactory value, which basically meets the design requirements. It should also be noted that, at this time, the zero point of the voltage controller is $\omega_{z-1} = 2\times10^4\, rad\,/\,s \ll \omega_c = 6.090\times10^4\, rad\,/\,s$, which can offset the phase lag caused by increasing

the integral link; the pole of the voltage controller is $\omega_{p-1} = 2.018 \times 10^5 \, rad/s \approx \omega_{z1} = 2.024 \times 10^5 \, rad/s$, which can cancel the equivalent series connection of the power stage filter capacitor C. The zero point ω_{z1} caused by the resistor, so the design of the voltage controller and its parameters used in this paper is reasonable.

4. Model simulation

In this paper, Matlab software is selected to simulate and analyze the model. According to the above parameters of the actual circuit, Figure 8 shows the Bode plot of the current loop gain $T_i(s)$ of the peak current mode control system. The solid line is a non-ideal model and the dotted line is an ideal model. The non-ideal model greatly reduces the gain peak at the resonant frequency, and the frequency characteristic curve is excessively gentle near the resonant frequency. It can be seen that when modeling the DC-DC converter, if only idealized Assume that the equivalent model of the DC-DC converter will be greatly deviated from the actual circuit, which will affect the design of the control circuit. Therefore, it is necessary to consider the non-ideal factors of the DC-DC converter in the modeling process.
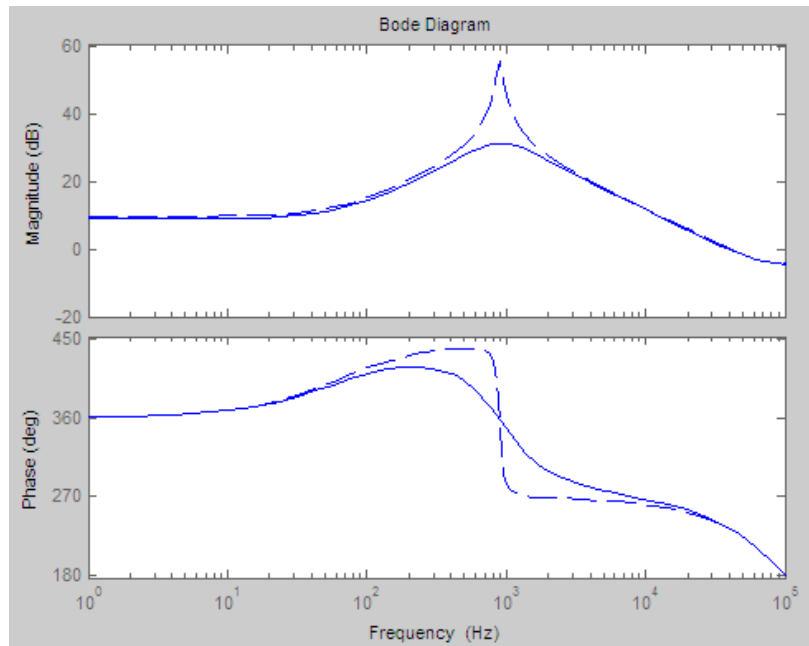

Figure 8. Bode plot of current loop gain $T_i(s)$ of peak current mode control system (solid line is non-ideal model, dashed line is ideal model)

Figure 9 is a comparison of the duty cycle control of the non-ideal Buck converter under CCM with the peak current mode control Bode diagram, where the solid line represents the peak current mode control Buck converter control-output transfer function Bode diagram, the dashed line is the duty cycle control Buck converter control-output transfer function Bode diagram. It can be seen that the peak current mode control greatly reduces the low frequency pole of the equivalent power level transfer function and is separated from the high frequency pole, and the high frequency pole is large. The falling slope of the amplitude frequency characteristic in the middle frequency band is controlled by the duty ratio. The $-40dB/dec$ becomes $-20dB/dec$ of peak current mode control, making the equivalent power stage transfer function $G_{vc}(s)$ an approximate single-pole system with a phase margin of $< 45^\circ$ to $> 90^\circ$.
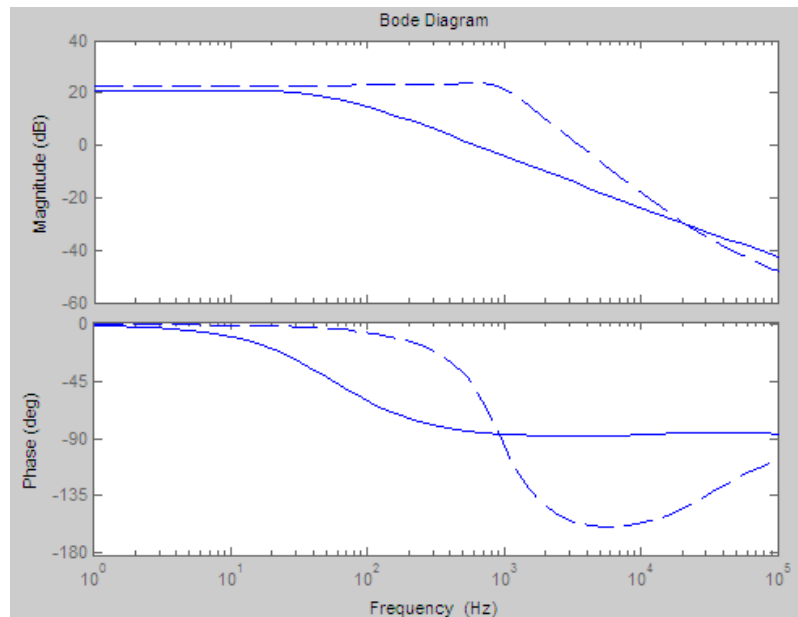
Figure 9. Control - output transfer function Bode diagram (solid line is the peak current mode control, dashed line is the duty cycle control)

Figure 10 is a comparison of the TVS Bode diagram of the open-loop transfer function before and after the compensation of the peak current mode control system with the voltage controller. The solid line represents the compensated Bode diagram, and the dashed line is the Bode diagram before compensation. It can be seen that after adding the voltage controller compensation, the system open-loop transfer function has a reasonable crossover frequency and phase margin, and greatly reduces the steady-state error of the low frequency band, and the system suppresses the disturbance, and the transient response speed and stability of the system are improved.
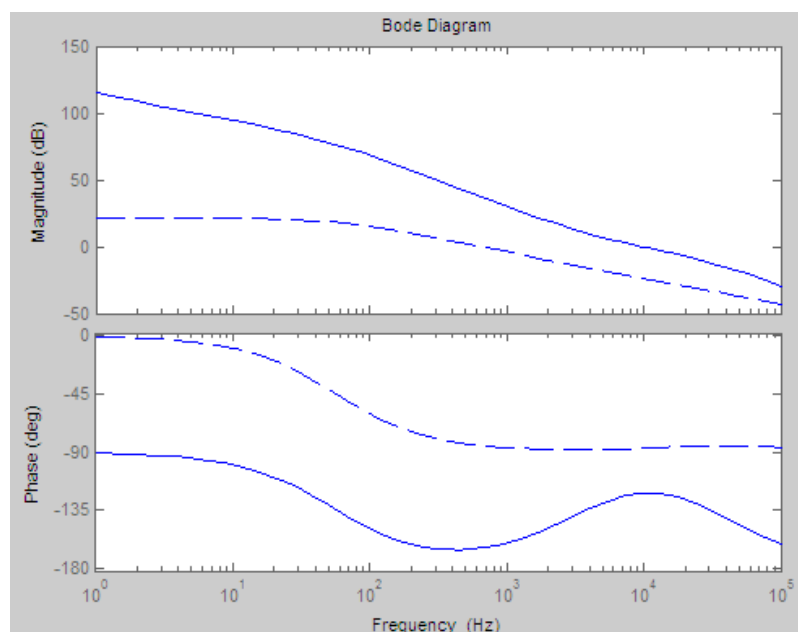
Figure 10. Bode diagram of the open-loop transfer function of the system before and after compensation by the voltage controller (after the solid line is compensated, the dotted line is before compensation)

5. Conclusion

In this paper, a complete AC small-signal model of the peak current mode control Buck converter system under CCM considering the influence of actual circuit non-ideal factors is established. The model is intuitive and physical, and can accurately reflect the actual circuit operation. Then, by analyzing the small signal transfer function, the equivalent power level considering non-ideal factors still has problems such as slow response speed and poor stability. On this basis, the voltage controller is designed to compensate, and the actual circuit parameters are taken as an example to simulate and analyze from the time domain and the frequency domain. It is proved that the designed voltage controller can improve the performance of the converter. The modeling method and voltage controller design of this paper provide a theoretical basis for the modeling and control circuit design of DC-DC converter system.

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