Method for Adjusting Single-Plate Code Synchronizer under Dynamic Conditions

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Yang Liu, Huizhi Zou, Kai Chen

China Satellite Maritime Tracking and Control Department, Jiangyin, 214431, China

Abstract. This paper is aimed at the single function of detecting and debugging single-board code synchronizer. It is difficult to meet the problem of dynamic reception of various types of arrow televisors. A new type of arrow telemetry solution can be proposed. Tuned single board code synchronizer adjustment method. On the basis of in-depth analysis of YH4 series code synchronizer frequency discrimination and phase discrimination principle, the key links affecting its dynamic performance - code ring reference clock, matched filter output passband voltage, symbol decision level, input signal The detection and debugging methods and working mechanism of the flat and baseline positions are described in detail.

1. Introduction

The single-board code synchronizer refers to the digital logic circuit that realizes the telemetry symbol timing with a single printed board. It belongs to the old generation product, but it still exists in a large number and participates in the model task. Since each functional circuit is implemented by a discrete digital chip, the time-shifting device operating point drift or critical instability factors are more prominent. At the same time, there are only a few whole-machine or sub-system test methods, such as bit error rate and sliding step, which are lack of single board detection and debugging means, especially for A very serious problem that has arisen at present - the whole machine or extension test is normal under normal static conditions, but under the dynamic condition of the arrow televisor task, the code synchronizer has multiple locking abnormalities, which cannot be ignored. It is necessary to analyze the causes in depth and find solutions. In particular, under the premise that the state of the arrow cannot be completely separated, the method of detecting and debugging the code synchronizer board is actively explored to achieve the optimal integrated state of the device performance, which can improve the work adaptability. To the obvious compensation effect.

2. Frequency discrimination-phase discrimination principle of YH4-26 code synchronizer

At present, the ship station uses YH4 series code synchronizer, including two generations of products: analog frequency discrimination-phase-detection code synchronizer (YH4-26) and all-digital data conversion tracking ring code synchronizer (YH4-29). The main difference between the two is the extraction method of the code loop phase error and the phase adjustment actuator - the integral link is different, and the key link affecting the performance of the board is the code ring clock, the matched filter output passband voltage and the symbol decision level. The secondary link is the input signal level and the baseline position. For the two types of code synchronizers, although the implementation is different, the specific adjustment parts and the test points are different, the working principle is the

same, so the adjustment methods are basically the same. The board debugging method is described by using the YH4-26 code synchronizer as an example.

The YH4-26 code synchronizer extracts the phase information of the symbol hopping from the received interfered PCM serial data stream, and uses the phase locked loop to complete the symbol synchronization of the local clock and the input signal, and performs symbol on the basis of the symbol. Decisions and pattern changes, eventually recovering clean PCM data and 00, 900 clocks to the frame synchronizer. The input circuit completes the AGC control before A/D sampling to stabilize the loop damping coefficient and loop gain, improve the code loop tracking characteristics, and ensure optimal symbol synchronization. The integral clearing matched filter circuit completes the optimal symbol energy estimation after symbol synchronization, so that the symbol decision circuit can fully utilize the result of single symbol integration to perform 0, 1 decision, and a single code due to the irrelevance of noise voltage The integral in the element interval is approximately 0, and the signal is unique in the single symbol interval. The result of the integration makes the signal stronger, thereby effectively improving the symbol-to-noise ratio of the symbol to ensure the maximum decision detection probability.

The most important part of the code synchronizer is the extraction of the symbol phase information and the adjustment of the local code clock frequency according to the setting of the code rate. In these two links, the implementation of the two single-board code synchronizers is different - the full digital loop uses the in-phase-phase phase integration circuit to complete the code phase extraction, and the up-and-down counter can directly adjust the code clock; and the analog code synchronization The frequency discriminating circuit and the VCO are used to extract the code phase and adjust the code clock. The system flow is shown in Figure 1.

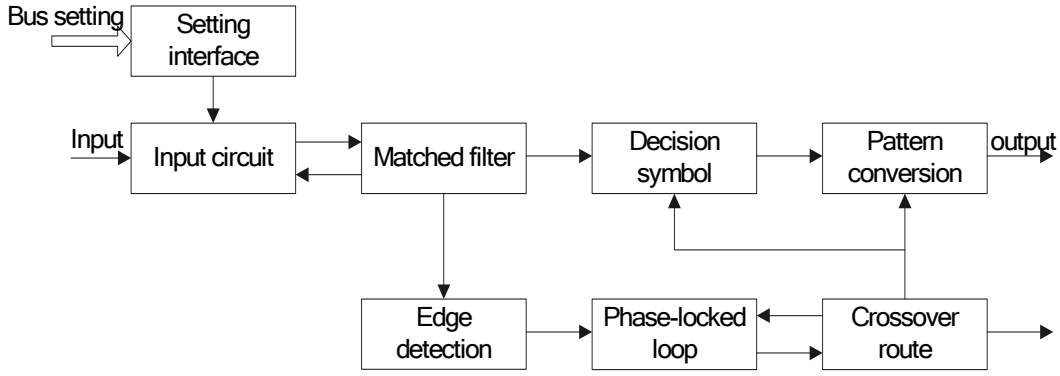

Figure 1. YH4-26 code synchronizer system flow chart

The phase-correcting principle of the analog code synchronizer is to sample the input PCM signal with the falling edge of the 8-bit clock 8HBIT of the locally generated code synchronization clock HBIT, since the symbol phase information of the input PCM signal is included in the symbol level transition. The instant, so as long as the shift register is registered for each sample value and the difference between the next sample value and the latter sample value (only if the XOR value of the symbol jump is 1 and the rest is 0), the specific jump of the symbol can be obtained. Position, thereby obtaining the phase error between the local clock HBIT and the input PCM signal symbol, as shown in FIG 2.

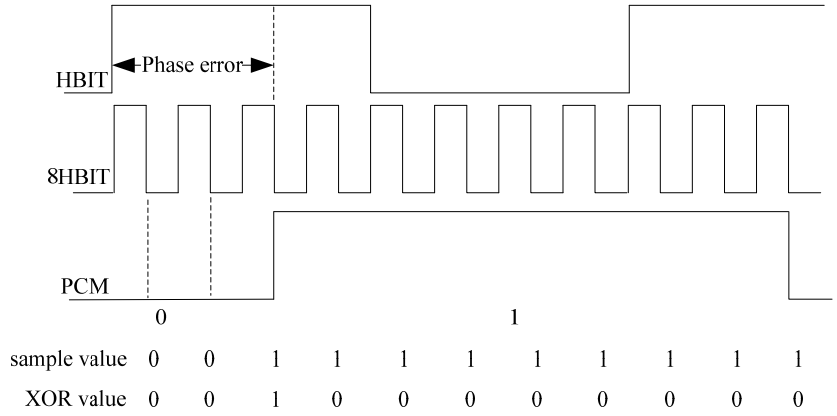

Figure 2. Analog code synchronizer phase detection timing diagram

The frequency discrimination principle of the analog code synchronizer is to compare the local code clock frequency of the four reference frequencies CK1, CK2, CK3, and CK4 generated by the frequency measurement clock generation circuit by the frequency division link with the set code rate, The frequency difference control reversible counter is added or subtracted, and the digital quantity of the voltage control voltage of the control VCO is obtained. After the D/A change, the VCO is pushed to lock at the set code rate clock frequency. The VCO is controlled by both the frequency discrimination and phase discrimination circuits, and is the common actuator of the two, as shown in Figure 3.

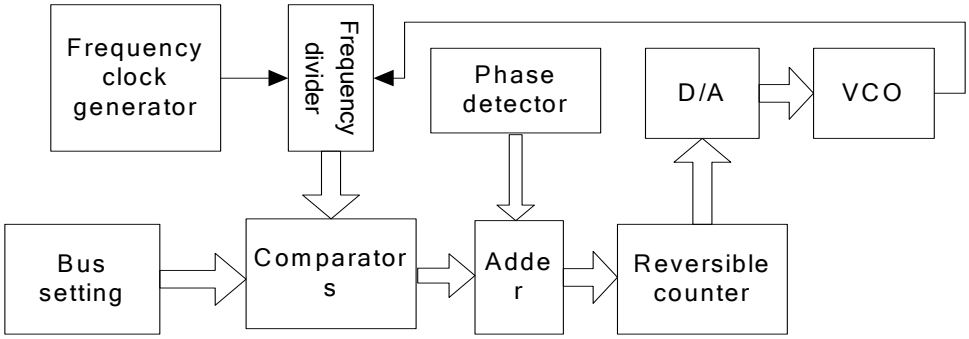

Figure 3. Analog code synchronizer frequency discrimination principle block diagram

The code rate R_b of the YH4-26 code synchronizer ranges from 40 to 2.621 Mbps, the step is 1 bps, and the working range is 100 to 2 Mbps. For such a large setting range, the frequency division link of the frequency discrimination unit can only be segmented. The mode is adjusted by frequency, which is divided into 4 ranges, and the range factor X is expressed as shown in Table 1.

Table 1. YH4-26 frequency setting range

Range factor	Corresponding code rate(bps)	Range reference frequency CK (Hz)
0	40.00～639.0	40.00(CK1)
1	639.0～10.23K	640.0(CK2)
2	10.23K～163.84K	10.23K(CK3)
3	163.84K～2.621M	163.84K(CK4)

The frequency division link adjusts the frequency division ratio of the range reference frequency CK according to the set code rate to obtain a required code rate, and the division ratio $N=R_b\times16^{3-X}/160$.

3. Method for adjusting code ring reference clock CK

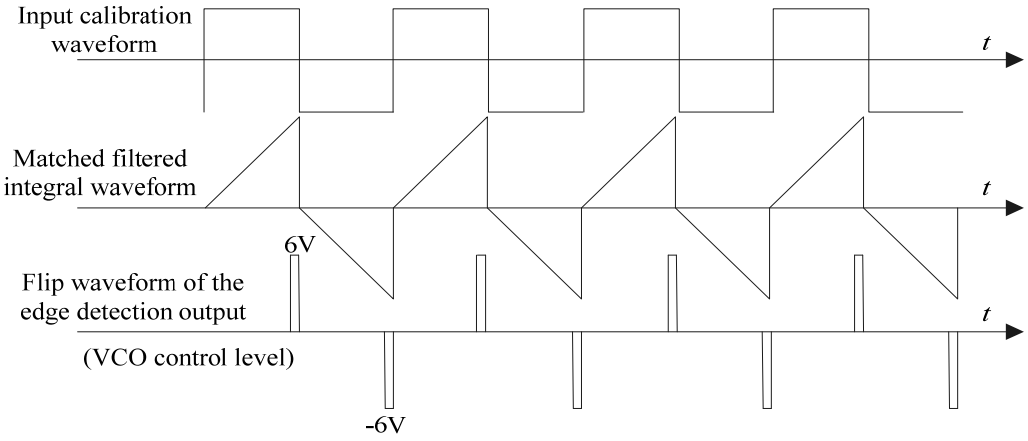

Figure 4. VCO control level leveling state calibration diagram

Before the code ring reference clock is adjusted, the VCO must be calibrated to control the correct pulsed state of the narrow pulse level. The VCO of the YH4-26 code synchronizer uses the integrated chip MC14046. The chip needs a starting level when it is working, so that the VCO is at the working zero point of the oscillation when no input voltage is applied. The specific calibration method is to short-circuit the 1-2 short-circuiting of the S2 on the board (the switching of the working and calibration is realized by S2) when the input signal is not applied, so that the input circuit generates a square wave self-calibration signal, and the matching filter circuit is matched with the wave. After the calibration signal is integrated, the sawtooth waveform of the up and down fly is obtained, and after the jump edge detection circuit, it becomes the narrow pulse flies level controlled by the VCO, as shown in FIG. At this time, the RS8 potentiometer on the palette makes the base position of the 13th pin (starting level input terminal) of the MC14046 0V, and the RS10 potentiometer adjusts the amplitude of the tumbling narrow pulse to ±6V. After the level is calibrated, short-circuit 2-3 of S2 to make the VCO work. The adjustment of the on-board code ring reference clock should be set according to different code rates. For example, the code rate is set to 2 Mbps. It is in the frequency range with a range factor of 3. The reference clock is CK4, and the test exit point of CK4 is TP2. The RS9 potentiometer makes TP2 a proportional pulse of about 163.84K. The code ring reference clock is the most important factor affecting the normal lock of the code synchronizer, so its adjustment is also the most critical part of the code synchronizer board debugging, especially when the code synchronizer VCO works zero and the reference clock drifts after long-term use. And the narrowing of the code loop tracking bandwidth is common, causing synchronization anomalies. This phenomenon is particularly prone to real-time tasks under dynamic conditions or the state of the task tape after playback. Due to the lack of single board detection and debugging means, under static conditions. It is normal to use the demodulation chassis analog source to go to the RF or IF closed-loop self-test. It is difficult to find the device performance degradation or critical state. Under dynamic conditions, the received signal quality is degraded, the on-board clock jitter and the data 0, 1 are unbalanced. The influence of other factors causes the receiving signal clock to deviate from the set state. At this time, the adjustment of the reference clock cannot be based on the normal situation, but must be adjusted according to the task state to adapt to the clock offset. Specifically, the playback task tape is used to adjust the RS9. The playback signal is synchronized properly.

4. Matching filter output passband voltage adjustment

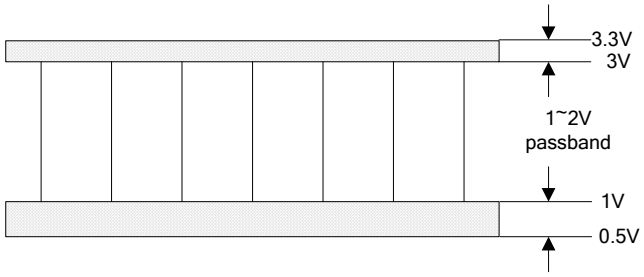

Figure 5. Matching filter passband voltage adjustment diagram

The matched filter output passband voltage reflects the matched filter integration time, ie the size of the window, which directly affects the symbol energy estimate at the time of the symbol decision. If the passband voltage of the filter does not reach the required magnitude, when the signal-to-noise ratio is low, the result of the symbol energy integration may be lower than the noise voltage, and the probability of misjudgement of the symbol is increased. Generally, the required filter integration time is 60%-80% of the single symbol interval, and the corresponding filter passband voltage is about 1~2V. When the signal-to-noise ratio of the dynamic signal is low, the passband voltage can be appropriately increased. In order to increase the integration time, but the maximum can not exceed one symbol interval, the integration time should not be too large, too much influence the dynamic response time, and extend the lock time of the code synchronization, so the dynamics with strong signal-to-noise and large level fluctuations The fading signal can appropriately reduce the passband voltage. The specific adjustment method is: adjust RS4 to make TP5 3~3.3V, adjust RS6 to make TP7 0.5~1V, adjust RS5 to make TP6 1~2V, and finally observe TP8 as 0.5~3.3V sampling waveform, 1~ in the middle of the waveform 2V clear passband, as shown in Figure 5, otherwise adjustable RS4, RS5, RS6 potentiometer.

5. Adjustment of symbol decision level

The symbol decision level can be adjusted based on the passband voltage adjustment. The symbol decision is completed by the chip NE529. Observe the P3 pin of the NE529, which should be a sampling triangle wave, as shown in Figure 6. The position of the waveform center line is V1 (triangular wave intersection position). At this time, RS5 should be adjusted so that the baseline level of the matched filter passband voltage is equal to V1, that is, the waveform baseline position at TP6 is equal to V1.

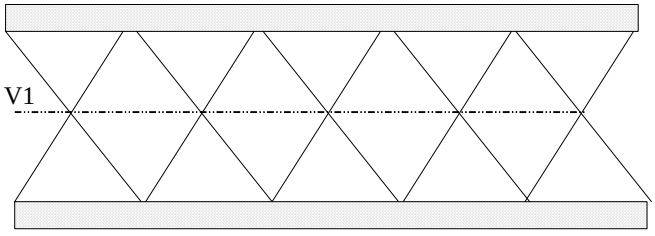

Figure 6. Symbol decision level sampling triangle wave waveform

6. Input signal baseline and level amplitude adjustment

The telemetry bipolar PCM code is unbalanced in 0 and 1 - in the state where 0, 1 appears in the data is not equal probability, the energy of the positive and negative frequency offset of PCM-FM will be inconsistent, and the downlink spectrum will be observed. The frequency offset energy is high, the

right shoulder of the spectrum envelope is higher than the left shoulder, and if the left shoulder is higher than the right shoulder, the telemetry receiving channel unit demodulates and restores the PCM code, and the zero-baseline position deviates from the zero potential, so that The symbol energy estimation starting position of the code synchronization matching filter is offset, and in severe cases, a symbol decision error is caused. The baseline position and signal level amplitude can be achieved by the oscilloscope observation code synchronization pre-stage - the eye diagram of the telemetry receiving channel unit demodulation, which can be adjusted by the baseline and gain adjustment potentiometer in the telemetry receiving channel unit. The position is adjusted to 0. Since the code synchronizer has a wide adaptability to the signal level amplitude - 1 to 10 V_{P-P}, the gain adjustment is not very high, and is usually adjusted to 2.8 V_{P-P}.

Conclusion

The above refers to all the single board adjustment methods of the YH4-26 code synchronizer, which can be called the unified adjustment. The dynamic state of the code synchronizer can generally achieve the required effect, and the overall effect of the adjustment is verified. It can be realized by testing the size of the code rate offset setting range of the demodulation chassis. The larger the offset range, the better the adjustment state. The performance verification of the board under dynamic conditions can be observed by playing back multiple disks of the same type of arrow televised tape. Generally, the state in which all the same types of tapes can be synchronized normally is the optimal state of code synchronization adjustment.

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