Design of Multi-Bus Adaptive Information Acquisition System

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Abstract. The active equipment uses a variety of bus technologies, and the research on multi-bus information acquisition system is carried out for the problem of bus-based information acquisition equipment and waste of resources. The paper bus designed a multi-bus adaptive detection module around CAN, RS232, RS485 and RS422 bus, and introduced the software and hardware design method and implementation. Through experiments, the module can realize the adaptive detection function of different equipment buses, and improve the generalization and intelligence level of the bus-based equipment information collection equipment.

1. Preface

In the information warfare,the strength of the equipment state monitoring capability directly affects the generation of combat capability and support power of the equipment.Real-time mastery of the state of the warfare equipment is an important part of the combat command and equipment support "confidence",and it is also guaranteed to "not blame" Prerequisite [1].The basis for the improvement of equipment status monitoring capability is the collection of equipment information [2].In the design of modern weapon equipment, the system control usually adopts the serial bus-based distributed design [3], so the equipment status and operation information collection can be conveniently realized through the serial control bus.The domestic active army equipment adopts bus technologies such as CAN, RS485, RS232, and RS422.Scholars have conducted extensive research on equipment information acquisition based on single bus, but the research on adapting to multi-bus information acquisition system is not deep enough, and there is bus-based equipment.The problem of a lot of information collection equipment and waste of resources [4-7].

2. Design Principle

The main functions of the multi-serial bus adaptive information acquisition module are: adaptive detection of different equipment buses, and correct reception and analysis of data. After connecting to the system, after adaptive detection, the system automatically recognizes the interface type and implements data collection and processing. The module has its own interface protection circuit and anti-interference circuit, which can be plugged in and out without powering up.

The principle of multi-serial bus adaptive information acquisition module is shown in Figure 1. The signal connected to the external interface is first protected by the interface protection circuit unit, and the interface level is divided to meet the input range of AD, and then the high speed is adopted. The AD scan collects the voltage value, inputs it to the CPU processing unit to determine what type of

interface, and enables the corresponding switch according to the judgment result, and the cut-through interface enters the CPU processing unit through the corresponding interface conversion circuit to perform data analysis communication, and communicate with the computer through the RS232 interface.

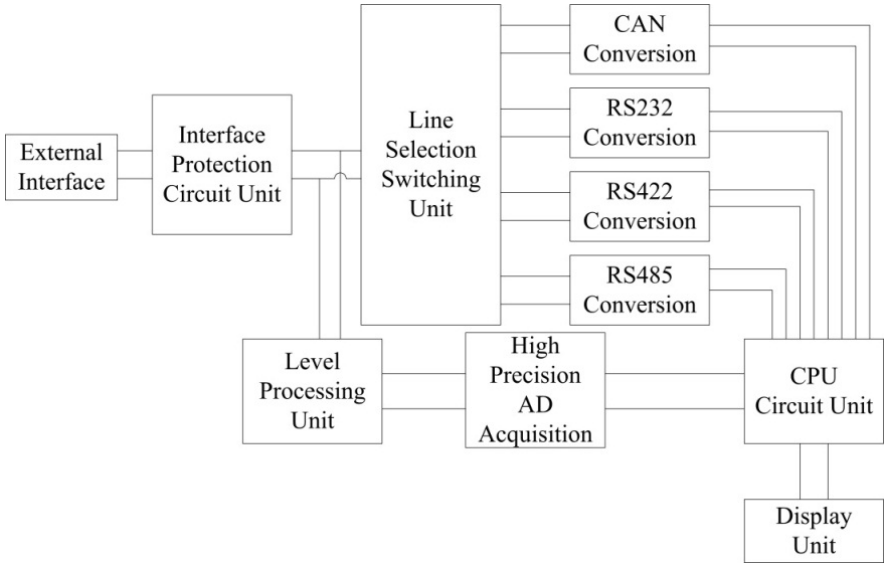

Figure 1. Block diagram of multi-serial bus adaptive information acquisition module

The interface protection circuit performs electrostatic protection and surge protection on the input four interface signals; the level processing unit divides the input interface signal levels to adapt to the input voltage range of the back-end isolated operational amplifier, and then passes The isolated operational amplifier is isolated; the high-accuracy AD acquisition circuit collects and processes the voltage signal for AD processing; the line selection switching unit enables the corresponding channel according to the judgment result of the CPU, and connects the identified interface signal to the subsequent stage circuit for processing. The interface conversion circuit is used to realize the conversion of the CAN, RS232, RS485 and RS422 voltage ranges to the TTL voltage or CMOS voltage range of the single chip microcomputer; the CPU processing unit is used to implement AD data processing, interface judgment, interface switching selection control, communication data reception analysis, Core control tasks such as data uploading; the upper computer display unit is used to communicate with the display unit to upload and display related data.

The interface between the adaptive bus detection module and the upper computer display unit is an RS232 interface, which communicates with the upper computer to realize display of communication data. The interface of the adaptive bus detection module and the equipment connection is a fixed five-core interface, including a CAN interface, an RS232 interface, an RS485 interface, and an RS422 interface. The signals of the four interfaces are multiplexed with four signal lines, and the other line is GND, five. The interface definition of the core interface is shown in Table 1.

Table 1. External Connection Interface Definition

Interface pin	RS232	RS485	RS422	CAN
1	TX	----	TX+	CAN_H
2	RX	----	RX+	CAN_L
3	----	485_A	TX-	----
4	GND	485_B	RX-	----
5	GND	GND	GND	GND

3. System Hardware Design

The system is mainly composed of interface protection circuit unit, level processing unit, AD acquisition circuit, interface conversion circuit, interface conversion circuit, CPU processing unit, host computer display unit, power supply module, etc. The isolation process is fully considered in the design process.

The external communication interface generates interference signals when the power-on state is plugged and unplugged, and the communication device also generates radiation interference when performing high-speed signal transmission. To prevent external signals from causing signal crosstalk to the module or the voltage leakage of the module, the device is burned out. The TVS protection circuit is used to suppress the effects of electrostatic discharge and surge pulses, and the isolation chip is used to isolate the input signal from the board signal in multiple places to prevent signal crosstalk and improve stability.

The level processing unit divides the acquired levels into voltages to ensure that the levels are within the range of the downstream isolation op amps and AD acquisition. The maximum input range of the external input signal is -15~+15V (when RS232 signal is input). Since the rear-stage isolated op amp can only input positive level, the input signal series diode 1N5822 filters out the negative level, because the rear-stage isolated op amp The voltage input range is 0~2V, so when the maximum level of the external signal is 15V input, the level of the connected isolation op amp should be no more than 2V. In the design, the voltage divider is used for level processing to make the voltage control. In the range of 0 ~ 2V. The four bus signals are divided by 100KΩ and 15KΩ resistors. The voltage range between different interfaces can still be separated after voltage division. When the input signal is at a maximum of 15V, the level of the access isolation op amp is 15*15/ (100+15) =1.96V<2V, which satisfies the requirement.

After the module is powered on, the CPU controls the AD acquisition circuit to cyclically collect the voltage value of each channel. When the external interface is connected, the current interface type is determined according to the collected voltage value. The D chip adopts AD7606BSTZ, which is a 16-bit, 8-channel synchronous sampling analog-digital data acquisition system, and selects serial interface communication mode. In this design, 5V analog power supply is used, 3.3V drive voltage, channels 1~4 are used to collect the level after the four-way signal resistor is divided, and channel 5 is used to collect the level after 5V power supply voltage divider for debugging. The remaining unused channels are grounded through a 0 ohm resistor.

The external interface type is confirmed according to the level value collected by the AD acquisition unit, and the external interface is switched to the corresponding interface conversion circuit by the CPU control switching unit to realize level conversion and communication identification. The relay is used for level isolation and selection switching, RS232 two signal lines, RS485 two signal lines, RS422 four signal lines, and CAN two signal lines. A total of 10 relays are used for line selection switching. When the interface type is judged, the MCU outputs a corresponding enable signal, and controls the corresponding relay to be closed, thereby turning on the road signal. The relay uses SRD-05VDC, which is powered by 5V and supports DC voltage up to 110V.

RS232, RS485, RS422, CAN conversion circuit is used to realize the conversion of each transmission level to TTL level. After conversion, it is 3 UART and 1 channel CAN. The converted signal uses ADUM1201ARZ-RL7 chip for isolation and level conversion.

4. System Software Design

In order to prevent the program from flying into an endless loop when the system is subjected to external interference, the program uses an internal independent watchdog function. The role of the watchdog is to feed the dog within a specified period of time (by configuration), and the program resets when the program runs out of time. The STM32F4's internal independent watchdog IWDG clock source uses an internal independent 32kHz low-speed clock, independent of the system clock master clock, which can still be reset in the event of a system failure. The independent watchdog settings are primarily implemented through three registered configurations. The key register

IWDG_KR enables the independent watchdog function by writing 0xCCCC to this register. After the watchdog is started, the counter generates a reset signal (IWDG_RESET) from the reset value 0xFFF to 0x000 to enable the system reset and restart. The prescaler register IWDG_PR and the reload register IWDG_RLR have write protection. The divide counter and the reload register can be configured by writing 0x5555 to the IWDG_KR register to disable protection. Prescaler register IWDG_PR, the length of this register is 32 bits. Only the lower three bits are used in configuration. The other bits are reserved to configure the division ratio of the watchdog clock. The reload register IWDG_RLR, a 32-bit register, is valid for the lower 12 bits. This register is used to hold the value reloaded into the counter. By configuring the above three registers, the watchdog function can be enabled. Note that once the IWDG is enabled, the dog will be fed within the set interval. Otherwise, the program will fall into the non-stop reset, and the IWDG cannot be closed midway and can only be restarted. Can be closed.

The program divides three execution tasks. The StartDefaultTask task initializes the IWDG watchdog register and enables the watchdog function. At the same time, the timer function is enabled to feed the dog at 1s and the system indicator is turned on.

The StartTask1 task turns on the external port voltage acquisition function, performs data analysis and comparison, and determines that the port type switching channel relay introduces an external port signal to the corresponding bus interface for bus data acquisition.

StartTask2 is responsible for communication with the host computer interface, and uploads the communication data transmitted from the multi-interface by serial port. The program includes serial port initialization, data transmission and analysis. In order to facilitate data analysis, data transmission is adopted, which is compatible with various equipment-specific protocols.

5. Experimental Verification

When the external interface input is the corresponding bus signal, the adaptive module performs the communication port level and pin judgment. After the data is parsed, it is uploaded to the host computer through the serial port/Usb to realize data transparent transmission, thereby judging whether the interface signal is correct.

6. Conclusion

The multi-bus adaptive acquisition system of the subject research realizes the adaptive detection of different equipment buses and correctly receives and parses the data. This system effectively solves the problem of single mess of current bus-based information collection equipment, and improves the generalization and intelligence level of bus-based information collection equipment.

Acknowledgments

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