

PAPER • OPEN ACCESS

Effect of Loss Distributions on the Balance of Capacitor Voltages in MMC Using Full Bridge Sub-Modules

To cite this article: Chujiao Wang *et al* 2019 *IOP Conf. Ser.: Earth Environ. Sci.* **252** 032189

View the [article online](#) for updates and enhancements.

Effect of Loss Distributions on the Balance of Capacitor Voltages in MMC Using Full Bridge Sub-Modules

Chujiao Wang^{*}, Qin Wang^a, Chuyang Wang^b, Jiajie Chang^c and Lan Xiao^d

School of Nanjing University of Aeronautics and Astronautics, Nanjing, China

^{*}Corresponding author e-mail: 1573779077@qq.com, ^awangqin@nuaa.edu.cn, ^b792246001@qq.com, ^c845206432@qq.com, ^dxiaolan@nuaa.edu.cn

Abstract. With the development of power electronics technology, modular multilevel converter (MMC) has become a popular converter due to its high modularity and good output characteristics. In recent years, half-bridge MMC has been widely studied. Compared with half-bridge MMC, MMC using full bridge sub-modules is more competitive because of its excellent DC short-circuit fault ride-through capability. Furthermore, the balance of capacitor voltages of sub-modules has a crucial influence on the working performance of MMC. To figure out the influence of non-ideal factors on the balance of capacitor voltages, this paper analyses the difference of the capacitor voltages and compares the unbalanced degree of capacitor voltages under different conditions. Firstly, in an ideal situation, the analytical expressions of bridge arm current and capacitor voltage increments are obtained, revealing the dynamic balance process of capacitor voltages. Secondly, expressions in a non-ideal condition reveal the effect of on-resistances of switching devices on the capacitor voltages. Finally, the influence of loss distributions in sub-modules on the balance of the capacitor voltages is analysed theoretically. Simulation models are built in PLECS to verify the theoretical analysis.

1. Introduction

With the improvement of modern transmission and distribution networks, HVDC (High Voltage Direct Current Transmission) has gradually become a powerful complement to AC transmission and is widely used worldwide. In the field of DC transmission, flexible DC transmission is rapidly developed due to its independent adjustment of active and reactive power and the ability to supply power to passive networks, etc. [1]. And MMC is very suitable for the application of flexible DC transmission because of its high modularity, good waveform quality, fault tolerance capability and many other advantages.

Right now, most of the existing MMC projects use MMC with half bridge sub-modules (HBSMs). Although it has the advantages of simple structure and low cost, when a short-circuit fault occurs on the DC side, the converter will change into an uncontrolled rectifier bridge due to some freewheeling diodes in the converter. Even if turning off all the switching devices to make the converter locked, the short-circuit current will still feed current to the short-circuit point through the freewheeling diodes, resulting in the inability to extinguish the arc. If the short-circuit current cannot be quickly cut off in a



short time, the freewheeling diodes will be damaged by overcurrent, and the safety and stability of the system will be seriously affected.

In MMC using full bridge sub-modules (FBSMs), Each SM can output positive, negative, and zero levels. When a short-circuit fault occurs on the DC side, the switches in sub-modules are all turned off. Regardless of the direction of the short-circuit current, it flows through the capacitors in sub-modules, and the voltages of these capacitors provide back-electromotive forces. Because of the reverse interruption capability, freewheeling diodes can force the fault current to drop to zero or minimum rapidly, thus guaranteeing the rapid recovery of the system [2]. Due to this characteristic, the full-bridge MMC has gradually gained more and more attention.

In an MMC system, inserting in different numbers of SMs results in different levels of bridge arm voltages, which in turn produce varying AC side voltages and bridge arm currents. And capacitances in SMs will be charged or discharged according to the working states of corresponding SMs and bridge arm current, which will cause the capacitor voltages gradually become different, resulting in the imbalance of capacitor voltages. And the unbalanced degree will be more serious without control, which may cause excessive stress on some devices and thus affect the safety and reliability of the system.

At present, most full-bridge MMC adopts a similar operation mode as the half-bridge MMC. That is, the switching devices of one of the bridge arms in the FBSM are respectively in a constant conduction or constant off state, and on the other bridge arm switching devices are alternately turned on, thereby the FBSM output a positive level or a zero level. In this mode, there are great differences in the loss and temperature of switching devices [3], which will affect the bridge arm current and the balance of capacitor voltages. In paper [4], the loss distribution in a FBSM is studied, and the redundant switching states of FBSMs are used to optimize the loss distribution inside the sub-module. However, the influence of switches' on-resistances on the balance of capacitor voltages almost no literature involved. Therefore, this paper first analyzes the difference of capacitor voltages under ideal conditions and non-ideal conditions through an analytical method, and reveals the influence of the on-resistances of switches. Basing on these analyses, the PLECS software is used to establish the simulation models.

2. A traditional operation mode of the FBSM

A FBSM can output three kinds of levels: positive, zero, and negative levels. In normal operation, a FBSM usually operates as similar as a HBSM, in which only two states are used to output positive or zero levels, inserted or bypassed. As shown in Fig. 1, S_3 on the right arm of the FBSM is always off, correspondingly S_4 is always on, while S_1 and S_2 on the left arm are alternately turned on to realize positive and zero outputs [5]. For the convenience of discussion, this paper defines this operation mode as the traditional operation mode.

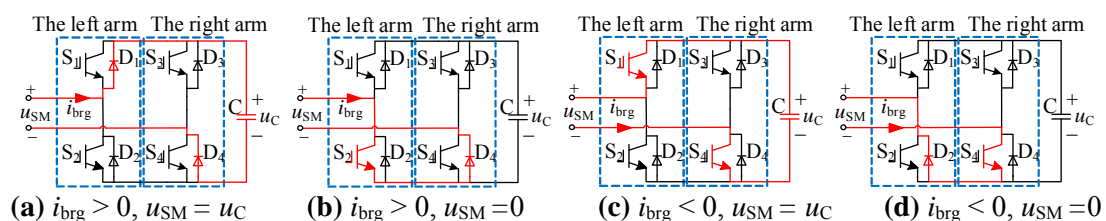


Figure 1. The traditional working mode of the FBSM

3. The difference of capacitor voltages in SMs under an ideal condition

The difference of the capacitor voltages of SMs indicates the unbalanced degree of the capacitor voltages in MMC. In this section, the variation of capacitor voltage U_C in a SM and the difference of U_C of adjacent SMs in one switching period T_s are derived by an analytical method. To simplify the analysis, only the upper arm is discussed. When a SM is inserted, the bridge arm current i_p flows

through the capacitor in the SM and charges or discharges it, thereby changing its voltage. Therefore, to analyze the variation of U_C , the bridge arm current i_p must be first analyzed [6].

The single-phase topology of MMC is shown in Fig. 2. The upper and lower arms are respectively composed of N SMs and an inductance. In a full-bridge MMC, each SM is a full bridge converter which can output $+U_C$ (inserted) and 0 (bypassed) in the traditional operation mode.

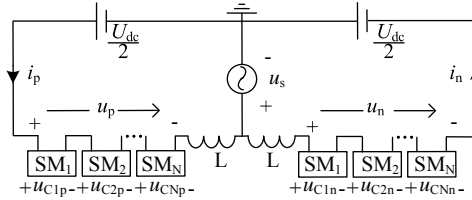


Figure 2. Single-phase MMC topology

In an ideal case, ignoring the on-resistances and other non-ideal parameters, the relationship of DC-side voltage $U_{dc}/2$, output voltage u_s , and voltage of the inductance can be expressed according to the Kirchhoff's voltage law:

$$L \frac{di_p}{dt} = \frac{1}{2} U_{dc} - u_s - \sum_{i=1}^{i=N} U_{ci} \quad (1)$$

Using the carrier phase-shifted PWM (CPS-PWM) modulation strategy, when the carrier frequency ratio (the ratio of the carrier frequency to the modulation wave frequency) is large, the output voltage u_s can be approximated as a constant U_s in a switching period T_s . For ease of analysis, small changes of capacitor voltages during one switching cycle are ignored, capacitor voltages remain at the initial value U_{dc}/N . Therefore, equation (1) can be expressed as equation (2), where n is the number of inserted SMs.

$$L \frac{di_p}{dt} \approx \frac{1}{2} U_{dc} - U_s - \frac{U_{dc}}{N} \cdot n \quad (2)$$

During one switching cycle T_s , n alternates between N_k ($N_k=1,2,3$) and N_k-1 , and the bridge arm current i_p changes accordingly, as shown in Fig. 3. To analyze the change of i_p , T_s is divided into N segments, and the time of each segment is $T_i = T_s/N$ ($i=1, 2, \dots, N$). In Sect i , the time when n is equal to N_k and N_k-1 is T_{i-} and T_{i+} , respectively, and the change rates of i_p are K_{i-} and K_{i+} [7], respectively.

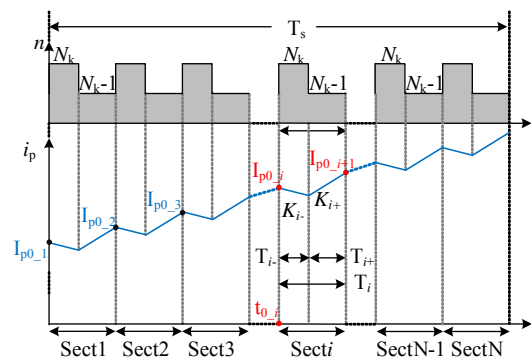


Figure 3. Changes of the inserted number of SMs and the bridge arm current

It can be seen from equation (2) that, in an ideal case, the change rates of i_p in T_{i-} and T_{i+} are constant, respectively expressed by:

$$K_{i-} = \frac{\frac{1}{2}U_{dc} - U_s - \frac{U_{dc}}{N} \cdot (N_k + 1)}{L} \quad (3)$$

$$K_{i+} = \frac{\frac{1}{2}U_{dc} - U_s - \frac{U_{dc}}{N} \cdot N_k}{L} \quad (4)$$

Assuming at the start time of Secti t_{0_i} , i_p is I_{p0_i} , then i_{pi-} in T_{i-} and i_{pi+} in T_{i+} can be expressed as:

$$i_{pi-} = I_{p0_i} + K_{i-} \cdot t \quad (5)$$

$$i_{pi+} = I_{p0_i} + K_{i-} \cdot T_{i-} + K_{i+} \cdot t \quad (6)$$

And the expression of the voltage increment of the capacitor in SM_i is:

$$\Delta U_{Ci} = \frac{1}{C} \int_{t_{0_i}}^{t_{0_i} + \Delta t} i_c dt = \frac{1}{C} \int_{t_{0_i}}^{t_{0_i} + \Delta t} i_p dt \quad (7)$$

Therefore, the capacitor voltage increments in T_{i-} and T_{i+} are respectively expressed by:

$$\Delta U_{Ci-} = \frac{1}{C} \cdot (I_{p0_i} \cdot T_{i-} + K_{i-} \cdot T_{i-} \cdot t_{0_i} + \frac{1}{2} K_{i-} \cdot T_{i-}^2) \quad (8)$$

$$\Delta U_{Ci+} = \frac{1}{C} \cdot [(I_{p0_i} + K_{i-} \cdot T_{i-}) \cdot T_{i+} + K_{i+} \cdot (t_{0_i} + T_{i-}) \cdot T_{i+} + \frac{1}{2} K_{i+} \cdot T_{i+}^2] \quad (9)$$

In a switching cycle T_s , the inserted time of each SM on the upper arm is the same, which can be expresses as $(N_k-1) \cdot T_i + T_{i-}$. Taking $N_k=1$ as an example, the inserted time of each SM is T_{i-} . It is assumed that SM_i starts to be inserted from t_{0_i} , i_p is greater than 0. At the time $t_{0_i} + T_{i-}$, SM_i is bypassed and the capacitor stops charging. Therefore, the increment of U_{Ci} in one T_s can be obtained by:

$$\Delta U_{Ci} = \frac{1}{C} \cdot (I_{p0_i} \cdot T_{i-} + K_{i-} \cdot T_{i-} \cdot t_{0_i} + \frac{1}{2} K_{i-} \cdot T_{i-}^2) \quad (10)$$

The SM_{i+1} starts to be inserted at t_{0_i+1} , the voltage increment of its capacitor in a T_s is:

$$\Delta U_{Ci+1} = \frac{1}{C} \cdot (I_{p0_i+1} \cdot T_{i-} + K_{i-} \cdot T_{i-} \cdot t_{0_i+1} + \frac{1}{2} K_{i-} \cdot T_{i-}^2) \quad (11)$$

And the value of i_p at the time t_{0_i+1} can be calculated as:

$$I_{p0_i+1} = I_{p0_i} + K_{i-} \cdot T_{i-} + K_{i+} \cdot T_{i+} \quad (12)$$

$$t_{0_i+1} = t_{0_i} + T_i \quad (13)$$

Then the difference of capacitor voltages of SM_{i+1} and SM_i in one switching cycle can be obtained as:

$$\Delta U_{Ci+1} - \Delta U_{Ci} = \frac{1}{C} \cdot (K_{i-} \cdot T_{i+} \cdot T_{i-} + K_{i+} \cdot T_{i+}^2 + K_{i-} \cdot T_{i-} \cdot T_i) = C_{onst} \quad (14)$$

Obviously, C_{onst} in the formula (14) is a constant. Similarly, in the case of $N_k=2, 3, \dots, N$, there is:

$$\Delta U_{Ci+1} - \Delta U_{Ci} = C_{onst} \quad (15)$$

It can be seen from formula (15), under the ideal condition, although the capacitor voltages are different in each switching cycle, the difference values of their increments are the same. And the difference can be positive or negative, so the capacitor voltages can reach the same value at a certain point. Therefore, in the ideal case, the capacitor voltages are dynamically balanced. The trend is shown in Fig. 4.

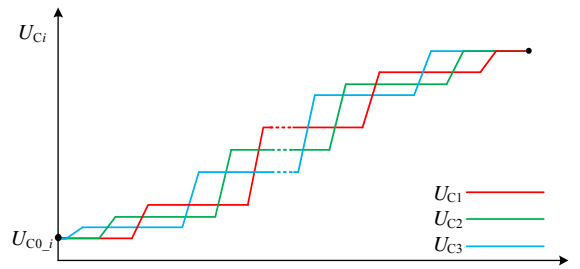


Figure 4. Capacitor voltage difference under the ideal condition

4. The difference of capacitor voltages in SMs under a non-ideal condition

In a non-ideal case, due to the presence of the on-resistances of the switches, according to Kirchhoff's law, the KVL equation of the upper-arm loop becomes:

$$L \frac{di_p}{dt} = \frac{1}{2} U_{dc} - u_s - \sum_{i=1}^{i=n} U_{ci} - \sum_{i=1}^{i=N} R_i \cdot i_p \approx \frac{1}{2} U_{dc} - U_s - \frac{U_{dc}}{N} \cdot n - \sum_{i=1}^{i=N} R_i \cdot i_p \quad (16)$$

The sum of R_i is the sum of the on-resistances of switching devices which the bridge arm current flows through. In different time periods T_{i-} and T_{i+} , the bridge arm current flows through different switching devices, so the sum of on-resistances is different. It can be seen from (16) that the change rate of i_p is no longer a constant due to the sum of the R_i . The expression of i_p can be obtained by solving the differential equation (16):

$$i_p(t) = \frac{1}{\sum_{i=1}^{i=N} R_i} \cdot \left(\frac{1}{2} U_{dc} - n \cdot \frac{U_{dc}}{N} - U_s \right) + C_{onst} \cdot e^{\frac{\sum_{i=1}^{i=N} R_i}{L} (t-t_0)} \quad (17)$$

And,

$$i_p(t_0) = I_{p0} \quad (18)$$

So, the C_{onst} can be calculated by:

$$C_{onst} = I_{p0} - \frac{1}{\sum_{i=1}^{i=N} R_i} \cdot \left(\frac{1}{2} U_{dc} - n \cdot \frac{U_{dc}}{N} - U_s \right) \quad (19)$$

Therefore, i_{p-} and i_{p+} during T_{i-} and T_{i+} can be obtained respectively by:

$$i_{pi-}(t) = A + (I_{p0-i-} - A) \cdot e^{-\frac{\sum_{i=1}^{i=N} R_i}{L} (t - t_{0-i-})} \quad (20)$$

$$i_{pi+}(t) = B + (I_{p0-i+} - B) \cdot e^{-\frac{\sum_{i=1}^{i=N} R_i'}{L} (t - t_{0-i+})} \quad (21)$$

Among (20) and (21):

$$A = \frac{1}{\sum_{i=1}^{i=N} R_i} \cdot \left(\frac{1}{2} U_{dc} - (N_k + 1) \frac{U_{dc}}{N} - U_s \right) \quad (22)$$

$$B = \frac{1}{\sum_{i=1}^{i=N} R_i'} \cdot \left(\frac{1}{2} U_{dc} - N_k \cdot \frac{U_{dc}}{N} - U_s \right) \quad (23)$$

Different SMs have the same constant A and B, but different initial bridge arm current I_{p0-i} . Taking $N_k=1$ as an example, supposing that SM_i starts to be inserted at t_{0-i} , SM_{i+1} starts to be inserted at t_{0-i+1} , and i_p is greater than 0.

In the T_{i-} period, the voltage increments of capacitors in SM_i and SM_{i+1} can be obtained respectively by:

$$\Delta U_{Ci} = \frac{1}{C} \left[A \cdot T_{i-} - \frac{(I_{p0-i} - A) \cdot L}{\sum_{i=1}^{i=N} R_i} \cdot \left(e^{-\frac{\sum_{i=1}^{i=N} R_i}{L} T_{i-}} - 1 \right) \right] \quad (24)$$

$$\Delta U_{C(i+1)} = \frac{1}{C} \left[A \cdot T_{i-} - \frac{(I_{p0-i+1} - B) \cdot L}{\sum_{i=1}^{i=N} R_i'} \cdot \left(e^{-\frac{\sum_{i=1}^{i=N} R_i'}{L} T_{i-}} - 1 \right) \right] \quad (25)$$

Therefore, the difference of the capacitor voltage increments of adjacent SMs is:

$$\Delta U_{CSM(i+1)} - \Delta U_{CSMi} \approx \frac{L}{C \cdot \sum_{i=1}^{i=N} R_i} \cdot \left(1 - e^{-\frac{\sum_{i=1}^{i=N} R_i}{L} T_{i-}} \right)^2 \cdot (A - I_{p0-i}) \quad (26)$$

It can be seen from (26) that, in the non-ideal situation, the difference of the capacitor voltage increments of SM_i and SM_{i+1} in a switching period is related to I_{p0-i} which is the value of i_p at the time t_{0-i} . As different SMs are inserted at different time, the bridge arm current I_{p0-i} is different. Therefore,

in the non-ideal case, due to the existence of the on-resistances of switching devices, the difference of the capacitor voltage increments of adjacent SMs in a switching cycle is no longer a constant. Capacitor voltages cannot reach the same value at a certain point, and the original dynamic balance process of the system is broken, as shown in Fig. 5.

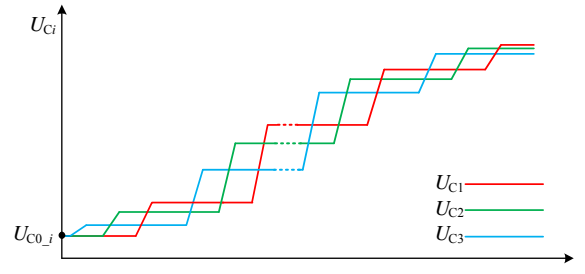


Figure 5. Capacitor voltage difference under the non-ideal condition

5. Influence of loss distribution in SMs on unbalanced degree of capacitor voltages

It can be seen from the above analysis that in the non-ideal case, the presence of the on-resistances of switches will destroy the dynamic balance process, and the magnitude of the on-resistances is related to the difference of the capacitor voltage increments of adjacent SMs. The greater the sum of the on-resistances is, the larger the capacitor voltage difference of adjacent SMs will be. In conclusion, the on-resistances affect the unbalanced degree of capacitor voltages.

When the full-bridge MMC works in the traditional operation mode, since there are constant-on and constant-off switching devices in SMs, the losses of the switches in a SM are different [8], so the temperature changes of them are not the same [9], which is inconvenient for the design of the heat dissipation system. In addition, the on-resistances change as the temperature changes, which in turn affect the difference of capacitor voltages.

To optimize the loss distribution in SMs and make the temperature of each switching device closer, another operation mode is proposed. That is, all the switching devices working at the alternating conduction state [10]. For the convenience of discussion, this paper defines this mode as the full operation mode. CPS-PWM is used as shown in Fig. 6.

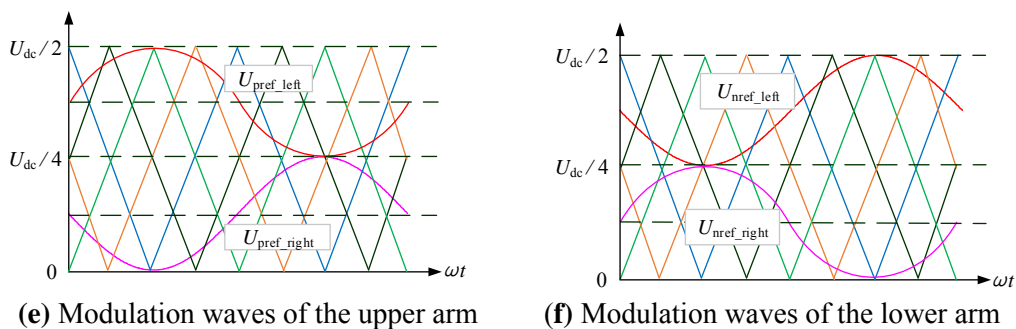
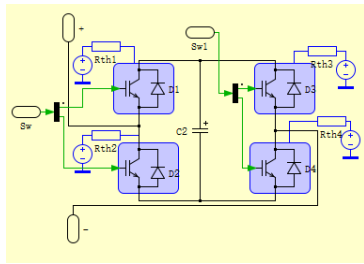


Figure 6. CPS-PWM of the full operation mode

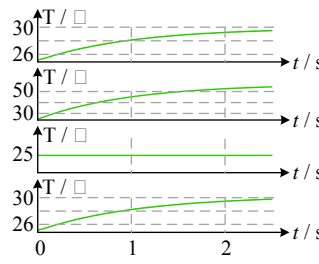
The modulation waves' expressions in SMs of the upper and lower arms are:

$$\begin{cases} u_{\text{pref_left}} = \frac{3}{8}U_{\text{dc}} + \frac{1}{8}U_{\text{dc}}\sin(\omega t) \\ u_{\text{pref_right}} = \frac{1}{8}U_{\text{dc}} + \frac{1}{8}U_{\text{dc}}\sin(\omega t + \pi) \\ u_{\text{nref_left}} = \frac{3}{8}U_{\text{dc}} + \frac{1}{8}U_{\text{dc}}\sin(\omega t + \pi) \\ u_{\text{nref_right}} = \frac{1}{8}U_{\text{dc}} + \frac{1}{8}U_{\text{dc}}\sin(\omega t) \end{cases} \quad (27)$$

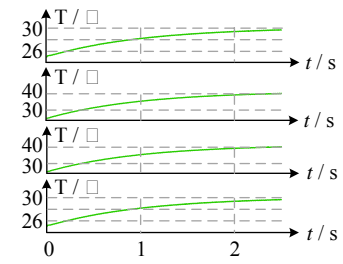
To clarify the temperature increment of each switch under different operation modes, a thermal model is built in the PLECS software for observation as shown in Fig. g. Fig. h and Fig. i shows the temperature simulation results of the switches in the traditional operation mode and full operation mode, respectively. In the traditional operation mode, the temperature of S_2 is the highest, the temperature of the S_4 and S_1 is close, and S_3 maintains the initial temperature due to its constant-off working state. In the full operation mode, the temperature of each switch is relatively close, which reduces the degree of uneven heating inside SMs to a certain extent.



(g) thermal model of the FBSM



(h) Temperature of switches in the traditional operation mode



(i) Temperature of switches in full operation mode

Figure 7. Temperature of the switches in different operation modes

The temperature variation will change the on-resistances of switching devices. In the traditional operation mode, S_2 is severely heated, so its on-resistance is bigger than others. Therefore, the fewer the number of SMs being inserted, the larger the sum of on-resistances and the capacitor voltage difference of adjacent SMs are, which is unfavorable for the balance of the capacitor voltages.

However, in the full operation mode, the loss distribution in SMs is relatively uniform, the temperature of each switching device is similar, so the difference of on-resistances is small, which can be considered as same as the on-resistance of S_4 in the traditional operation mode. Therefore, the sum of the on-resistances is smaller than that in the traditional operation mode, and the change of the number of inserted SMs does not cause a significant effect on the sum of the on-resistances.

To observe the influence of the loss distribution in SMs on the unbalanced degree of capacitor voltages, a single-phase full-bridge MMC simulation model was built in the PLECS software. The variance of capacitor voltages is used as an indicator to judge the unbalanced degree of capacitor voltages. The larger the variance, the higher the unbalanced degree.

The simulation parameters are shown in the Table 1:

Table 1. Simulation parameters.

DC-link voltage U_{dc}	Output AC voltage (AMP)	Initial capacitor voltage $U_{C0\ i}$	Number of SMs on upper bridge arm N
600V	220V	200V	3

The simulation results are shown in Fig. 8 below.

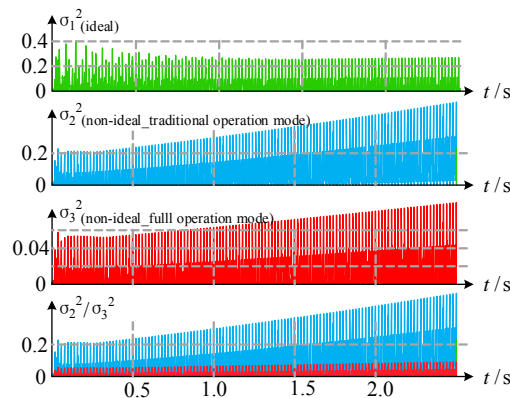


Figure 8. Capacitor voltage unbalanced degree in different situations.

It can be seen from Fig. 8 that, in the ideal condition, the variance of capacitor voltages fluctuates around 0, which means the capacitor voltages remain dynamically balanced. In the non-ideal case, due to the existence of on-resistances of switching devices, the variance of capacitor voltages shows an upward trend, and the dynamic balance of the capacitor voltages is broken. By comparing the waveforms in Fig. 8, the unbalanced degree of capacitor voltages in the traditional operation mode is greater than that in the full operation mode. In other words, the uneven loss distribution in SMs leads to an increasement of the unbalanced degree of capacitor voltages, which verified the correctness of theoretical analysis.

6. Conclusion

Starting from the traditional operation mode of full bridge MMC, this paper analyzes the difference of the capacitor voltages under the ideal condition and the non-ideal condition, respectively, and explains the influence of the on-resistances of switches on the unbalanced degree of capacitor voltages. Basing on these analyses, simulation models are built in PLECS to observe the temperature of switches in a FBSM and the variances of capacitor voltages in different conditions. And the simulation results show that optimizing the loss distribution in SMs can reduce the unbalanced degree of capacitor voltages, which further verify the correctness of the theoretical analysis.

Acknowledgments

This work was financially supported by Research on the balance control of capacitor voltage for MMC system based on multi-structures and variable operation conditions of submodules fund (61673210).

References

- [1] Weimin Ma, Fangjie Wu, Yiming Yang, et al. Flexible HVDC Transmission Technology's Today and Tomorrow [J]. High Voltage Engineering, 2014, 40 (8): 2429-2439.
- [2] Yongjie Luo, Yaohua Li, Zixin Li, et al. DC Short-circuit Fault Ride-through Control Strategy of Full-bridge MMC-HVDC Systems [J]. Proceedings of the CSEE, 2016, 36 (7): 1933-1943.
- [3] Qingrui Tu, Zheng Xu. Dissipation analysis of MMC-HVDC based on junction temperature feedback method [J]. High Voltage Engineering, 2012, 38 (6): 1506-1512.
- [4] Yufei Dong, Heya Yang, Wuhua Li, et al. An Optimal Strategy for Loss Distribution of Full-bridge Submodules in Modular Multilevel Converters [J]. Proceedings of the CSEE, 2016, 36 (7): 1900-1907.
- [5] Kai Li, Zhengming Zhao, Liqiang Yuan, et al. An Improved Phase-shifted Carrier-based Modulation and Loss Distribution Analysis for MMC Using Full Bridge Sub-modules [C]. 2016 IEEE 8th International Power Electronics and Motion Control Conference, 2016: 1252-1258.
- [6] Qiang Song, Wenhua Liu, Xiaoqian Li, et al. A Steady-State Analysis Method for a Modular

- Multilevel Converter [J]. IEEE Transactions on Power Electronics, 2013, 28(8): 3702-3713.
- [7] Chuyang Wang, Lan Xiao, Chujiao Wang, et al. Analysis of the Unbalance Phenomenon Caused by the PWM Delay and Modulation Frequency Ratio Related to the CPS-PWM Strategy in an MMC System [J]. IEEE Transactions on Power Electronics, 2018: 1-13
- [8] Binbin Li, Rongfeng Yang, Dandan Xu. Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters [J]. IEEE Transactions on Power Electronics, 2015, 30 (1): 297-310.
- [9] Steffen Rohner, Steffen Bernet, Marc Hiller, et al. Modulation, Losses, and Semiconductor Requirements of Modular Multilevel Converters [J]. IEEE Transactions on Industrial Electronics, 2010, 57 (8): 2633-2642.
- [10] A. D. Rajapakse, A. M. Gole, P. L. Wilson. Electromagnetic Transients Simulation Models for Accurate Representation of Switching Losses and Thermal Performance in Power Electronic Systems [J]. IEEE Transactions on Power Delivery, 2005, 20 (1): 319-327.