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MIMO Transceiver based on Software Defined Radio

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Abstract. Amplitude-phase consistency of multiple input multiple output (MIMO) transceivers has a significant impact on the performance of digital beamforming algorithms and MIMO communication algorithms. Based on the concept of software defined radio (SDR), architecture of a MIMO transceiver with a amplitude-phase consistency calibration scheme was designed. By looping the output signals into input channels, amplitude-phase consistency of the output or input channels can be measured, thus the channel calibration was performed in the digital signal processing. Based on the designed architecture, a MIMO transceiver prototype was implemented by adopting SDR radio frequency (RF) agile transceivers and a digital signal processing system on chip (SOC), with software running on it also implemented. Experiments show that the MIMO transceiver achieves high amplitude-phase consistency performance after calibration, and has the characteristics of high integration, miniaturization and high flexibility.

1. Introduction

Amplitude-phase consistency of multiple input multiple output (MIMO) transceivers makes significant impact on the directivity, beamwidth and sidelobe levels of digital beam forming (DBF) algorithms [1]. Thus performance in space resolution, anti-interference, and bit error rate (BER) in MIMO radar or communication systems decreases for poor multi-channel amplitude-phase consistency [2-3]. Therefore, it is necessary to try eliminating the multi-channel amplitude-phase errors in MIMO transceiver design in which extra calibration circuits are required along with the basic MIMO circuits improved [4].

Research progress in software defined radio (SDR) technique makes signal processing systems tend to employ both software defined hardware and more integrated hardware. SDR based signal processing platforms are with lower hardware complexity and smaller size, which enables miniaturization of wireless systems and helps building the amplitude-phase consistency calibration circuits in MIMO transceivers.

RF front-end which is composed of discrete components including multiple analog-to-digital converters (ADCs) and multiple digital-to-analog converter (DACs) is complex in design and it cannot meet the requirements of integration, universality, and flexibility of MIMO transceivers with SDR technique adopted. Thus some of the recent developed devices attempt to make up the gap. AD9361 is an RF 2×2 agile transceiver with integrated 12-bit DACs and ADCs. It covers 70 MHz to 6 GHz, which adopts advanced SDR technique and supports MIMO technique [5-6]. Signal processing platforms based on AD9361 have the characteristics of high integration, low power consumption, and easy programmable.

Meanwhile, implementation of SDR technique requires the signal processing platforms with high real-time performance and massive computation capability. One of the choices is the ZYNQ series system on chip (SOC) provided by Xilinx, which integrates processing system (PS) and programmable



logic (PL) [7]. Signal processing platform based on this series SOC features both high real-time programmable logic in PL with parallel computation capability and complex software in PS with high flexibility.

Combining SDR technique with MIMO technique, architecture of a MIMO transceiver with an amplitude-phase consistency calibration scheme is designed in this paper. And a MIMO transceiver prototype with a small size supporting up to 32 RF channels is implemented.

This paper is organized as follows. Section 2 designs the architecture, main circuit and synchronization scheme of the proposed MIMO transceiver. Section 3 describes the hardware and software prototype implementation. Section 4 verifies the MIMO transceiver prototype both in basic functions and in the multi-channel amplitude-phase consistency performance with the test data presented. Finally a summary of the work is presented in section 5.

2. Architecture Of An Sdr Based Mimo Transceiver

2.1 Architecture

The proposed MIMO transceiver is mainly composed of an signal processing (SP) element, an radio frequency (RF) unit, a power supplier, and a clock processing unit. It functions baseband signal processing, amplitude-phase consistency calibration, and controlling based on SDR technique. Architecture of the proposed MIMO transceiver is depicted in Fig. 1.

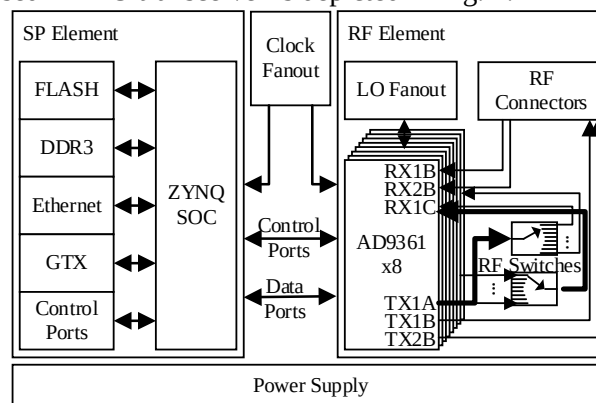


Figure 1: Architecture of the MIMO transceiver.

2.2 Circuits Design

The SP element adopts the ZYNQ-7000 series SOC as the signal processor. ZYNQ-7000 series SOC connects the RF unit, receives/transmits/processes digital signals, and provides high speed GTX (gigabit transceiver: high speed serial transceivers provided by Xilinx FPGAs) transceivers and controlling interfaces. The RF unit employs multiple AD9361 with extra circuits for amplitude-phase consistency calibration designed.

2.2.1 The SP Element. A ZYNQ-7000 series SOC is employed as the signal processor. PS of the SOC is software programmable and deals with low real-time tasks, while PL of the SOC is hardware programmable and deals with high real-time parallel computation and logic tasks. PS and PL are connected via Advanced eXtensible Interface (AXI) with high transmission throughput. Fig. 2 presents the architecture of the SP element.

As depicted in Fig. 2, external interfaces of the SP element include the control and data ports connected to AD9361, GTX transceivers for external data transmission, and the extra low-voltage differential signaling (LVDS) ports. The SP elements also include the peripherals necessary for signal processing, such as a FLASH controller, a DDR3 memory controller, a 10/100/1000 BASE-T Ethernet, and the debug ports.

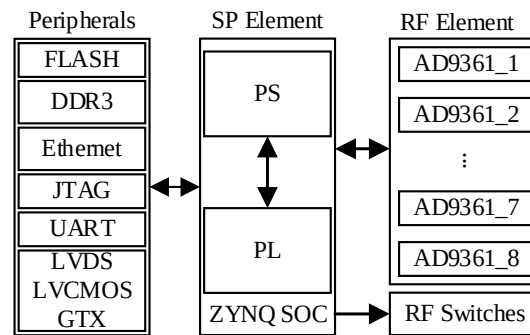


Figure 2: Architecture of the SP element

2.2.2 The RF Element and the Multi-channel Synchronization Circuits. AD9361 implements an RF 2x2 transceiver with integrated 12-bit ADCs and DACs. Each of the dual receivers supports 2 differential output ports [6]. And each of the dual transmitters supports 3 differential input ports. Thus one AD9361 is adopted as two independent transmitters and two independent receivers, each with another multiplexed input port and output port connected to an RF switch for amplitude-phase consistency calibration purpose.

Multiple AD9361s are assembled to work as one MIMO transceiver, with multiple channels synchronized. For the purpose of multi-chip synchronization and multi-channel amplitude-phase consistency, it is required that the routed input and output, and the clocks are synchronized. The synchronized input clocks are obviously required. An input clock is provided from an oscillator or external circuit. It is then fanned out by a low latency clock buffer and finally input to the multiple AD9361s. The clocks should be well routed with equal length.

Similarly, the synchronized local oscillators (LO) are also required. The LOs are used in mixers of the transceivers. An external LO is input to a low latency clock buffer. It is then fanned out and at the end input to the LO input ports of the multiple AD9361s. The LOs should also be well routed with equal length.

Besides, the synchronized baseband data interfaces are required. The interfaces use LVDS signals to transfer baseband data between PL and AD9361 with the data clock up to 250 MHz. AD9361s provide a specific SYNC signal to synchronize the multichip baseband. Data, framing signals, the data clocks, and the SYNC signals should be well routed with equal length.

2.2.3 The Amplitude-phase Consistency Detection Circuit. There are residual amplitude-phase errors in the MIMO signals processed by the synchronization circuits presented in section 2.2.2. In order to further improve the amplitude-phase consistency, an error detection and compensation scheme is designed. The scheme is based on internal loop back circuits. With the redundant input and output ports connected to RF switches, the SP element can acquire the loop back signals and then detect the amplitude-phase consistency of the multiple receivers and transmitters. Because two channels in one AD9361 features high amplitude-phase consistency, only one channel for one chip is needed to be detected. Architecture of the loop back circuits is presented in Fig. 3.

As depicted in Fig. 3, the thick arrows represent the reference transmitted signal and the reference received signal. The thin lines represent signals need to be selected for testing. The RF switches will select one of thin lines to connect to the reference line in amplitude-phase consistency detection process.

When detecting consistency of the multiple receiver (RX) channels, PL use direct digital synthesizer (DDS) to transmit single-tones via the reference transmit channel. The RF switch connects the reference signal to every RX1C port of the eight channels need to be tested in turn. PL receives the signal acquired by the corresponding channel. The received loop back signal is then send to PS for amplitude-phase error calculation. Similarly, when detecting consistency of the multiple transmitter (TX) channels, the eight channels transmit single-tones. The RF switch in turn connects these signals to RX1C port of the reference receiver channel. The loop back signal corresponding to the TX channel

is acquired by the reference receiver and then send to the PS via PL. PS finally calculate the amplitude-phase error.

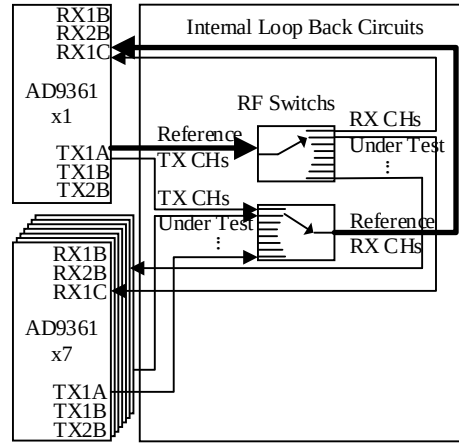


Figure 3: Architecture of the loop back circuits

When switching the multiple channels, single-tones should maintain continuous phase process. For convenience, the channel switch interval T , frequency of the signal tones f_{dds} , and the sampling frequency f_s should be integral multiple.

$$T = N_1 / f_{dds} \quad (1)$$

$$f_s = f_{dds} / N_2 \quad (2)$$

where N_1, N_2 are positive integers.

2.3 Amplitude-Phase Error Compensation Scheme

Based on the circuits presented above, an amplitude-phase errors compensation scheme should be developed to achieve better performance. Amplitude error can be simply compensated by a multiplier. While phase error compensation scheme can be developed as followed.

The acquired baseband IQ signals can be formulated as

$$x_I(t) = r(t) \cos \phi_X(t) \quad (3)$$

$$x_Q(t) = r(t) \sin \phi_X(t) \quad (4)$$

where $r(t)$ represents the signal envelope varying with time, $\phi_X(t)$ represents the signal phase varying with time.

The TX LO with the initial phase φ_{tx} can be written as

$$x_{TXLO}(t) = e^{j(2\pi f_0 t + \varphi_{tx})} \quad (5)$$

where f_0 is the LO frequency.

Then the zero IF baseband signal transmitted is

$$\begin{aligned} x(t) &= \text{Re}\{[x_I(t) + jx_Q(t)]e^{j(2\pi f_0 t + \varphi_{tx})}\} \\ &= x_I(t) \cos(2\pi f_0 t + \varphi_{tx}) \\ &\quad - x_Q(t) \sin(2\pi f_0 t + \varphi_{tx}) \end{aligned} \quad (6)$$

In the amplitude-phase detection circuits, the transmitted baseband signal is directly looped back to an RX channel. LO of the receiver is with an initial phase φ_{rx} and can be written as

$$x_{RXLO}(t) = e^{-j(2\pi f_0 t + \varphi_{rx})} \quad (7)$$

Assembling Eq. 6 and Eq. 7, with a low pass filter applied, we have the baseband received signal $y(t)$ to be

$$\begin{aligned}
y(t) &= 2x(t)e^{-j(2\pi f_0 t + \varphi_{rx})} \\
&= x_I(t) \cos(\varphi_{tx} - \varphi_{rx}) \\
&\quad + jx_I(t) \sin(\varphi_{tx} - \varphi_{rx}) \\
&\quad - x_Q(t) \sin(\varphi_{rx} - \varphi_{tx}) \\
&\quad + jx_Q(t) \cos(\varphi_{tx} - \varphi_{rx}) \\
&= [x_I(t) + jx_Q(t)]e^{j(\varphi_{tx} - \varphi_{rx})}
\end{aligned} \tag{8}$$

It is found in Eq. 8 that the loop back signal acquired by the receive channel is added with both the initial phase of TX LO and that of RX LO. By analyzing spectrum of the received loop back signal, this phase can be calculated for each of the channels, and then the phase difference or phase error among all the channels can be calculated: 1) Using one dedicated reference receive channel with a fixed φ_{rx} and switching the transmit channels, the TX phase error φ_{x1} of the different channels can be calculated; 2) Using one dedicated reference transmit channel with a fixed φ_{tx} and switching the receive channels, the RX phase error φ_{x2} of the different channels can be calculated.

The phase error φ_{x1} and φ_{x2} can be compensated by

$$x_I(t) = \text{Re}\{[x_I(t) + jx_Q(t)]e^{j\varphi_x}\} \tag{9}$$

$$x_Q(t) = \text{Im}\{[x_I(t) + jx_Q(t)]e^{j\varphi_x}\} \tag{10}$$

Eq. 9 and Eq. 10 can be used both in the transmitter and the receiver.

3. Implementation

3.1 The Fabricated MIMO Transceiver Prototype

Base on the architecture proposed in section 2, a MIMO transceiver prototype is fabricated, which adopted one Xilinx XC7Z100 SOC and eight AD9361s. Fig. 4 depicts such a 32 channels MIMO transceiver prototype.

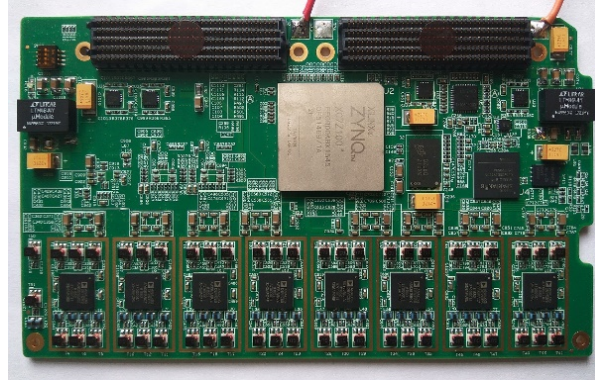


Figure 4: MIMO transceiver prototype

MIMO transceiver depicted in Fig. 4 implements both 16 TX channels and 16 RX channel in a relatively small size. It achieves high amplitude-phase consistency performance on account of the improved hardware and carefully designed calibration scheme. A wide band of 70 MHz~6 GHz is covered with the channel bandwidth up to 56 MHz [6]. The main SP processor XC7Z100 is composed of a dual core Cortex-A9 ARM processor and programmable logic. Performance of the programmable logic is close to corresponding ones of the Kintex-7 series FPGAs. XC7Z100 can provide both high real-time and low real-time signal processing resources. There are two FMC connectors on the prototype for external data transmission via both 10/100/1000 BASE-T Ethernet and GTX transceivers. The prototype also provides the necessary interface as TX LO, RX LO, and synchronized clock input ports. Besides, the proposed amplitude-phase consistency detection circuit depicted in section 2.2.3 is implemented on the prototype, which ensures the implementation of the calibration scheme.

3.2 Software Architecture

There are two kind of software run on the proposed MIMO transceiver prototype. One is for PL and the other is for PS.

PL is hardware programmable and the ‘software’ run on it are hardware described logic cells. A high real-time calculation module, high speed transmission ports, and external interfaces are provided by the PL logic. In detail, it consists of IP cores for AD9361 interfacing, baseband signal transmission and control, direct memory access (DMA) controller, channel amplitude-phase compensation, RF switches controlling, high speed data transmission, and etc. Besides, there is a chip selection module in PL for SPI enabling using a 3-8 decoder to extend the chip selection (CS) signals provided by PS. Architecture of the logic in PL is presented in Fig. 5.

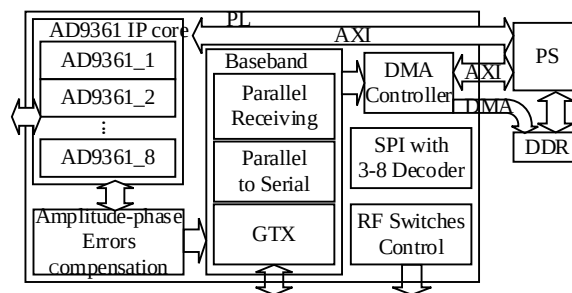


Figure 5: Architecture of the logic in PL

PS implements the system initiation, channel calibration, and other software which is application related. Algorithms are run on the built-in real-time operation system (OS). Procedures of the software in PS is presented in Fig. 6.

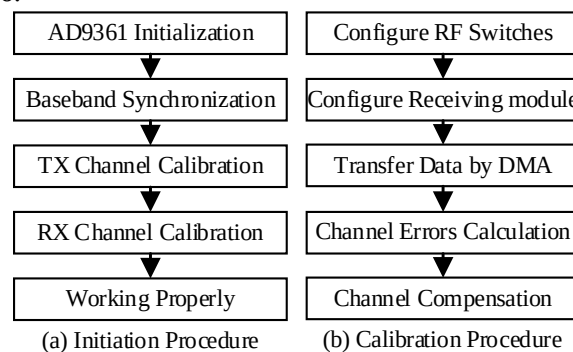


Figure 6: Procedures of the software in PS

3.2.1 Initiation Procedure. When powered on, AD9361s are initialized at first. Then PS configures hardware to support the baseband synchronization. After that both the TX channel calibration and RX channel calibration are conducted in turn. Finally the MIMO transceiver can work properly.

3.2.2 Calibration Procedure. The calibration procedure is conducted by cooperation of PS and PL. PL appropriately selects both the RX channel and the TX channel among all the channels, acquires the corresponding loop back single-tones via the parallel receiving module and the parallel to serial module, and then transfer these data to the DDR memory attached to the PS by a DMA controller. The acquired data are buffered in first input first output (FIFO) before being transferred by the DMA controller. PS accomplishes the amplitude-phase errors calculation on the data acquired.

The channel compensation module is integrated in the AD9361 interfaces, which can be configured by PS via the AXI on chip bus. PS writes the calculated amplitude-phase errors to registers in the channel compensation module and the errors are compensated according to Eq. 9 and Eq. 10.

4. Experiments

In order to verify the basic functions and the amplitude-phase error calibration scheme, the proposed MIMO transceiver was tested in laboratory. Multi-channel amplitude consistency with residual errors was firstly tested. Then the multi-channel phase calibration procedure was verified with the multi-channel phase errors before and after calibration presented.

4.1 Multi-channel Amplitude Consistency with Residual Errors

Agilent's signal generator E4438C was used to generate a 2 GHz single tone. The 2 GHz single tone was split to eight ones and supplied to the LO input ports of the eight AD9361s (with the real LO frequency to be 1 GHz, as the datasheet described). DDS in PL was configured to transmit a 5 MHz sine wave. Thus the frequency of the transmitted sine wave was 1005 MHz. Agilent's spectrum analyzer N9020A was used to test the transmitted signal power. Absolut signal power of all the eight channels is depicted in Fig. 7.

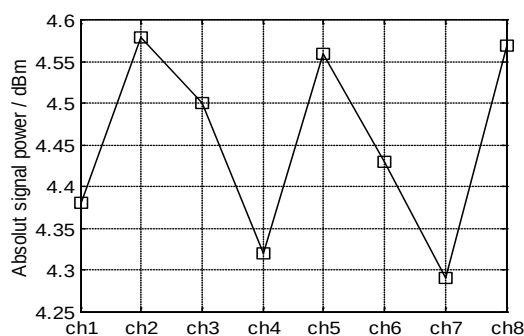


Figure 7: TX channel amplitude consistency

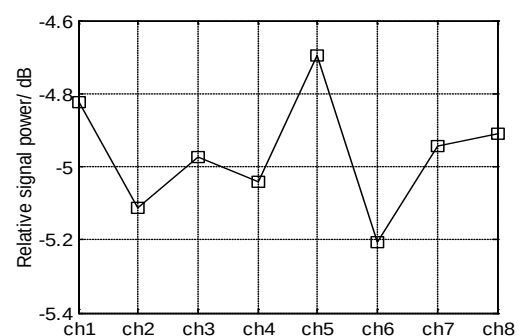


Figure 8: RX channel amplitude consistency

As depicted in Fig. 7, ch1~ch8 correspond to the TX channels of the eight AD9361s. Because we didn't issue the amplitude calibration procedure, the test results indicate that TX channel amplitude consistency without calibration among the 8 AD9361s is 0.3 dB, in the case of the 1 GHz LO frequency.

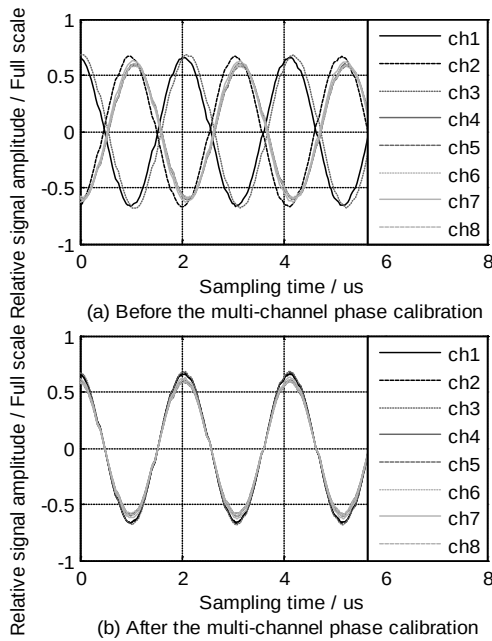
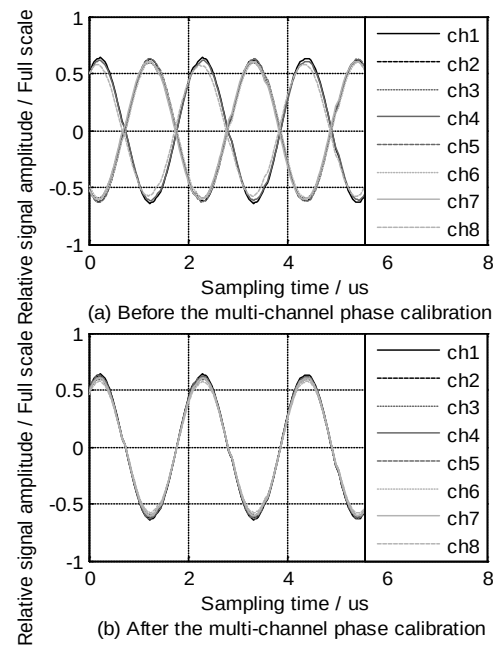
RX channel amplitude consistency was also conducted. LO frequency was configured as the experiment presented above, while another signal generator E4438C was used to provide a 1005 MHz sine wave. The generated wave was split to 8 ones and supplied to the input ports of RX channels of the eight AD9361s. PL and PS acquired the input signal. Spectrum of the acquired data was analyzed using FFT, and we have the relative signal power consistency, as depicted in Fig. 8.

As depicted in Fig. 8, ch1~ch8 correspond to the RX channels of the eight AD9361s. Because we didn't issue the amplitude calibration procedure, the test results indicate that RX channel amplitude consistency without calibration among the 8 AD9361s is 0.5 dB, in the case of the 1 GHz LO frequency.

A 0.3 dB and 0.5 dB amplitude consistency is sufficient for many scenarios. And further compensation only needs multipliers. So the detailed amplitude calibration experiment is not presented, while we focus more on the phase calibration procedure.

4.2 Multi-channel Phase Consistency Verification

LO frequency was also configured to be 1 GHz, and the DDS in PL was configure to output a 480 kHz. The TX channels under test were switched in an interval of 0.1 ms. The single tones corresponding to eight TX channels were in turn received via the reference RX channel. The loop back single tones were acquired before and after the multi-channel phase calibration, respectively. The acquired waves are presented in Fig. 9.

**Figure 9:** TX channel delay/phase consistency**Figure 10:** RX channel delay/phase consistency

In Fig. 9 (a), some of waves are phase reversed. LO feature of AD9361 results in this phenomenon. AD9361 needs an LO input with twice frequency of the real LO used, so there is a frequency divider in the chip with a 180 degree phase ambiguity. After the FFT calculated on the received waves, the 180 degree phase ambiguity was firstly corrected and then the multi-channel phase errors ϕ_x were derived. The delay error can be derived from the phase error as $t_x = \phi_x / (2\pi f_0)$, where f_0 is the carrier frequency. We acquired the waves multiple times, and the derived channel delay errors are presented in Tab. 1.

Table 1: Channel delay errors of multiple times

Channel	T0/ps	T1/ps	T2/ps	T3/ps
ch1	0	0	0	0
ch2	18	18	17	14
ch3	-19	-17	-17	-18
ch4	9	10	10	13
ch5	6	8	8	0
ch6	1	1	1	-3
ch7	-7	-7	-6	-9
ch8	13	15	16	20

Tab. 1 indicates that multi-channel delay consistency is less than 40 ps, which coincide with the 25 ps skew of the clock buffers used for LO fanout [8].

The multi-channel phase errors were compensated according to Eq. 9 and Eq. 10. The transmitted waves acquired are presented in Fig. 9(b), with the multi-channel delay errors less than 10 ps.

Multi-channel phase consistency calibration procedure of RX channels is similar to that of TX channels. Experiments show that the multi-channel delay consistency is less than 35 ps before calibration, while it is promoted to less than 10 ps after calibration. The waves acquired are shown in Fig. 10.

It can be summarized from Fig. 9 and Fig. 10 that the proposed MIMO transceiver prototype implemented the multi-channel phase error detection and compensation scheme with multi-channel delay consistency less than 10 ps after calibration.

5. Conclusions

Architecture of an SDR-based MIMO transceiver with multi-channel amplitude-phase consistency calibration scheme was proposed. A small-sized 32 channels MIMO transceiver prototype was then fabricated. Experiments show that the multi-channel amplitude consistency is up to better than 0.5 dB while the multi-channel delay consistency is better than 10 ps, in the case of the 1 GHz LO frequency. The proposed MIMO transceiver has the characteristics of high integration, miniaturization, high flexibility, simplicity in calibration, and high performance in multi-channel amplitude-phase consistency.

6. Acknowledgments

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7. References

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