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Increasing the quality and power capacity of HERIC PV-Inverter through multilevel topology implementation

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Abstract. In photovoltaic generation applications, high efficiency and good output power quality inverter are very important. The most common way to improve the quality of the inverter output voltage is to increase the switching frequency. However, at the same time, this method will increase power losses. This paper introduces a new topology inverter: HERIC multilevel, as an inverter that has good voltage quality (low THD) with a low switching frequency. This topology was tested and analyzed by performing simulations to compare it with the conventional HERIC and cascaded H-Bridge inverters. The results prove that the multilevel HERIC inverter has a lower THD compared to the two inverters. At the switching frequency of 2500Hz; Multilevel HERIC inverters have THD, 1.23%, cascaded H-bridge has 1.34% THD, and conventional HERIC THD 11.4%.

Keywords: inverter HERIC multilevel, *Cascaded H-Bridge*, *switching*, THD.

1. Introduction

In a renewable energy based power plant, besides used as a converter of DC to AC voltage, inverters are a role as an interface to transfer the electrical energy into the electrical system. In this function, the qualification that must be fulfilled by an inverter is the great efficiency and high quality of the generating power, i.e., voltage and current. Similarly, those qualifications are needed by inverter used in photovoltaic generation (PV-inverter). Various researches have been carried out to achieve increased efficiency and quality of output power. Some PV-inverter topologies have been developed for this aim, both through the development of an inverter base topology and by optimizing their operations scheme [1] – [5]

Regarding the efficiency, in 2006, Schmidt et al., created an inverter topology called HERIC (Highly Efficient and Reliable Inverter Concept) which is a modification of full-bridge inverter topology. This topology has been produced and has entered the PV-inverter market [6]. As the name implies, the HERIC topology has a very high-efficiency advantage in converting electrical energy. Kurmaiah and Anil [7], comparing the performance of the HERIC inverter to some other inverter topologies where it was found that HERIC showed its superior efficiency. HERIC topology is suitable for transformerless PV applications because of the small leakage current, and EMI (Electromagnetic Interference) produced [5]. It is also able to overcome reactive power coming from the grid.

Another required aspect of a PV-inverter as generation converter is the power quality, especially the form of output voltage it produces. Ideally, the inverter output voltage is stable and sinusoidal-wave. However, the voltage is often not pure sine, indicating the existence of harmonics [8]. Large



harmonics will cause the performance of the supplied electrical load as well as electrical power distribution components not optimal. The longer it happens will cause damage to the components. Therefore, actions are needed to reduce harmonics at the inverter output. Various efforts have been made to improve the quality of power and reduce the harmonics produced by the operation of PV-Inverters [9], [10].

The output waveform of a PWM inverter can be improved through the switching frequency settings of the semiconductor components that compose it. The higher the switching frequency, the resulting waveform is getting closer to sinusoidal. But along with the increasing switching frequency, the power losses on the switch will also be greater which will reduce the efficiency of the inverter itself. Also, increasing the quality of PV inverter voltage can also be obtained by using a topology that is naturally designed to produce voltage output with small harmonics, this topology as well as the multilevel inverter topology. Besides being able to accommodate high power operations, multilevel inverter technology will produce better voltage quality, lower harmonics with a less switching frequency.

In this paper, a new topology of PV-inverter is presented through modification of the HERIC inverter by applying a multilevel topology to its power circuit topology. Software simulation is presented to show the achievements that can be obtained from this.

2. HERIC PV-Inverter and multi-level inverter topologies

In a photovoltaic system, the inverter functions as a power converter to connect the PV module to the grid. PV-inverter is an important element with the main function is to convert the DC voltage that has been generated into AC voltage in sync with the grid. To support its operations, PV-inverters have complex devices and mechanisms, including DC-DC converters on the input side, MPPT, anti-islanding, output filter, and others. The simple block diagram of a PV-inverter system is shown in Figure 1.

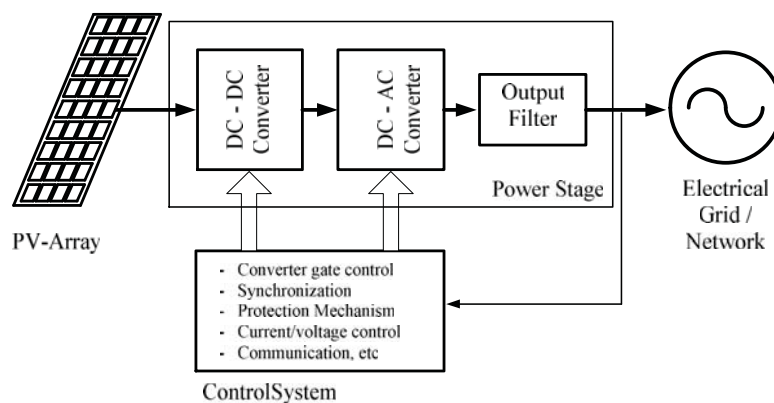


Figure 1. A simple block diagram of a Grid-connected PV-inverter

2.1. PV Inverter HERIC

Development of PV-inverter technology continues to be carried out to improve efficiency and quality. Some PV inverter topologies have been introduced: H5 topologies, H6-type MOSFETs, HRE (High Reliable and Efficient) inverters, and other topologies. In 2006, Sunways introduced the HERIC (Highly Efficient and Reliable Inverter Concept) inverter topology as a modification of the full-bridge topology inverter (Full Bridge). A bypass switch is added on the AC side of the bridge in the form of two back-to-back IGBT components, which are operated on the grid frequency. The HERIC topology circuit and its operation are shown in Figure 2, where C_{in} is a coupling capacitor that is connected

parallel to DC input (dc-link), L_1 and L_2 are inductor filters on the grid side of the inverter. The back-to-back bypass (S^+ , D^+ , and S^- , D^-) has two vital functions: preventing the exchange of reactive power between L and C_{in} during zero voltage conditions, this increases efficiency and isolates the PV module from the grid during zero voltage conditions, this is to eliminate high-frequency content in V_{PE} .

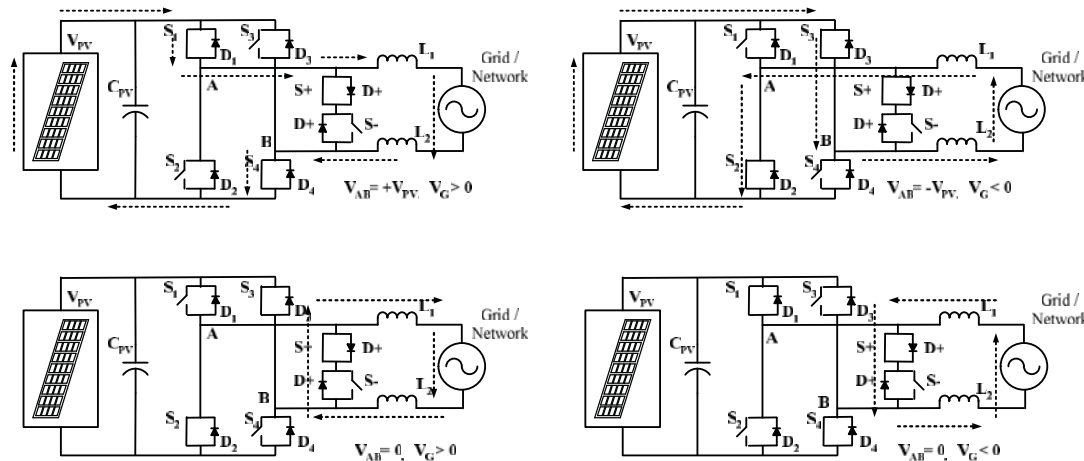


Figure 2. The HERIC PV-Inverter topology and its operation [5]

To produce a positive voltage, S_1 and S_4 are connected (on), they are operating at the switching frequency. When S_1 and S_4 are off, then S^+ will remain connected, so the output from the inverter will be zero voltage. This condition is called a freewheeling situation. Next, to produce a negative voltage, S^+ will be off, S_2 and S_3 are on at the switching frequency. When S_2 and S_3 are off, the current will flow through S^- and D^+ so that the voltage created at the load is zero. The switching pattern on the HERIC inverter is shown in table 1.

Table 1. Switching state of the HERIC PV-inverter

Switches				Diodes				Vout
S1	S2	S3	S4	S+	S-	D+	D-	
on	off	off	on	on	off	off	off	Vin
off	off	off	off	on	off	off	on	0
off	on	on	off	off	on	off	off	-Vin
off	off	off	off	off	on	on	off	0

2.2. Prospective Multilevel topology for combined with HERIC PV-Inverter

Switch components in traditional HERIC PV-inverter work in unipolar PWM mode (0, $+V_{PV}$, 0, $-V_{PV}$, 0), which still gives the possibility of distortion to appear during the modulation process. Also, the use of a single phase full-bridge topology still faces constraints of limited power capabilities. These two weaknesses can be avoided by applying a multilevel topology to conventional HERIC inverter topologies.

Multilevel inverters are DC-AC converters where the output produced has more than two voltage or current levels [11]. This inverter is a conventional inverter like a square-wave or SPWM inverter but is arranged in a cascade. The waveform produced by a multilevel inverter is a stair-wave with a different voltage level, the more voltage levels, the better the output waveform and the THD (Total

Harmonic Distortion) is getting closer to zero. In these inverters, there is no need for a high switching frequency to produce sinusoidal waves, the lower dv/dt stress in the switch components will reduce electromagnetic compatibility (EMC). It can also be operated both at fundamental and high switching frequencies. Low switching frequency operation means that the switching losses are low and the efficiency is high.

Among many proposed multilevel inverter topologies, there are three topologies which are majority applied, they are the cascaded H-bridges with separate DC sources, diode clamped (neutral-clamped), and flying capacitor (capacitor clamped), Figure 3 illustrated the topologies. In the single-phase cascaded one-phase type inverter (Figure 3 left), each separate dc source (Separate DC Source) is connected to a single-phase H-bridge inverter. Each inverter level generates three different output voltages $+V_{dc}$, 0, and $-V_{dc}$, by connecting the DC source through a combination of four switches; S_1 , S_2 , S_3 and S_4 . To obtain $+V_{dc}$, S_1 and S_4 in conditions connected (on), while $-V_{dc}$ is obtained by connecting the S_2 and S_3 . During S_1 and S_2 or S_3 and S_4 are on, the output voltage will be zero. The output of each H-Bridge then is connected in series to obtain total voltage output from each inverter.

The neutral point-clamped converter (Figure 3 center), was a three-level diode-clamped inverter. The advantages of this topology are that all phases use the same source so as to minimize the capacitance needs of converters, capacitors can be pre-charged in groups, have high efficiency for fundamental switching frequencies, while their disadvantages are that the real power flow is difficult for a single inverter and tends to overcharge or discharge without proper monitoring and control, the number of diodes needed is proportional to square with the number of levels so that it will cause difficulty at a high level.

Flying-capacitor-based inverter (Figure 3, right) is an inverter that is similar to diode-clamped inverters except that the diodes clamped are replaced with capacitors. This topology has a ladder structure on the DC side of the capacitor, where the voltage on each capacitor is different from the capacitor next to it. A voltage increase between two adjacent capacitors determines the voltage step in the output waveform. The advantage of this inverter is that it has to tap on the inner voltage level; in other words, two or more switch combinations can unify an output voltage. Phase redundancies are available to balance the voltage level of the capacitor, real power flow, and reactive power can be controlled. While the weakness is: difficult to track the voltage level for all capacitors, the low efficiency of the real power transfer, the higher price and the larger physical size due to the use of a large number of capacitors, packaging will be more difficult at higher levels.

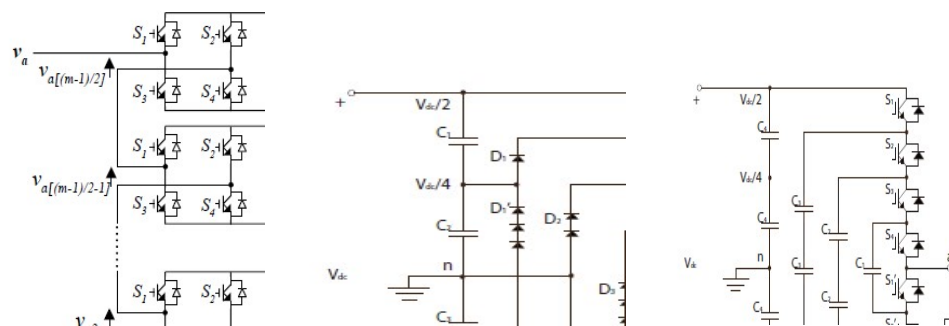


Figure 3. Single-phase multilevel inverter topologies: a. *Cascaded H-Bridge* b. *topology NPC five-level*, c. *topology Flying Capacitor five-level* [12]

3. Proposed PV-Inverter with HERIC Multilevel topology

3.1. Power Circuit Diagram

Based on the advantage and disadvantage of various multilevel inverter topologies described in the previous section, the multilevel HERIC inverter that will be proposed is the single-phase cascade H-bridge inverter of five voltage levels. This inverter circuit is obtained by arranging two full-bridge inverters with separate DC sources. At the load of the circuit, two back-to-back IGBT diodes were added, as was the concept of a conventional HERIC inverter. Eight other switches are used for the two H-bridge. Also, on the load side, the inductor and capacitor components are connected which serve as filters to minimize the harmonic in the inverter output waveform. Figure 4 shows the proposed 5-level HERIC inverter.

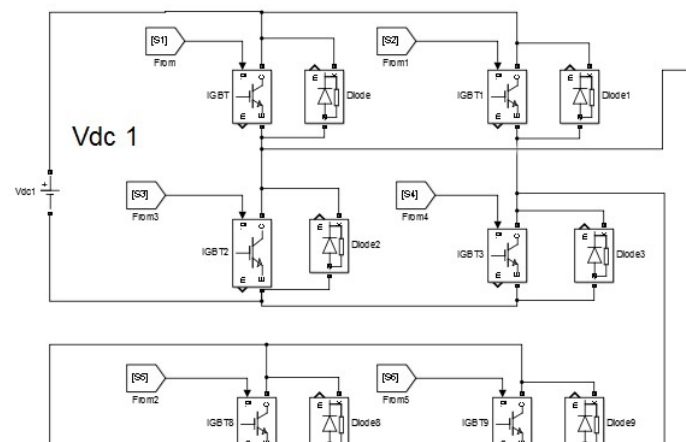


Figure 4. Proposed single phase HERIC cascade H-bridge 5-level inverter

3.2. Gating Signal Generation

Gating signal generation technique for the proposed multi-level on the HERIC inverter is the phase disposition SPWM (PD-SPWM). Compared with other modulation techniques for multilevel-inverter such as the phase opposite disposition (POD) and alternative phase opposition disposition (APOD) – SPWM, the PD-SPWM technique produces smaller harmonics. In this technique, for multilevel inverters with N-voltage levels, N-1 triangular waves are needed. So, for a five-level voltage, four triangular waves as carrier waves (V_c) are modulated with a sinusoidal wave signal (V_m), SPWM technique, Figure 4. The resulting gating signal is used to control eight switch components in the main inverter circuit. For switch components in the back-to-back leg, the gating signal generation is carried out with different techniques; the two switches are operated with the reference signal frequency according to the power frequency, 50 or 60 Hz. One switch is activated when the reference signal is positive ($V_m > 0$), and one other switch is activated when the reference signal is negative ($V_m < 0$). Using Simulink/Matlab, this modulation is described as in Figure 5.

The switching pattern of inverter switch components is designed according to the desired voltage level. For a 5-level inverter with two DC sources, the voltage levels that will be generated are 0, V_{dc} , $2V_{dc}$, $-V_{dc}$, and $-2V_{dc}$. The output voltages are obtained by switching patterns as in Table 1. Switching conditions are also based on the relationship between modulating sine-waves and each triangle wave as a carrier wave, this relationship is seen in Table 2 and 3.

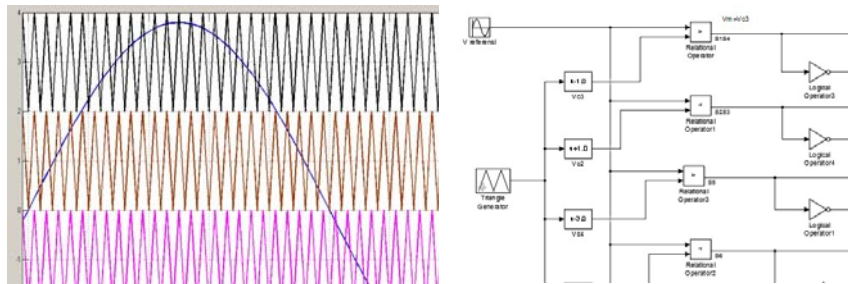


Figure 5. PD-SPWM modulation on HERIC 5-level inverter and Simulink/Matlab gating generation model

Table 2. List of active switches for each voltage level

No	Vout	Active Switches
1	0 V	S1 S2 S5 S6
2	Vdc	S1 S4 S5 S6
3	2Vdc	S1 S4 S5 S8
4	-Vdc	S2 S3 S5 S6
5	-2Vdc	S2 S3 S6 S7

Table 3. Relation between modulation voltage (V_m) and carrier voltage (V_c)

No	Switch (on)	Voltage	V_m and V_c relation
1	S1	0, Vdc, 2Vdc	$V_m > V_{c3}$
2	S2	0, -Vdc, -2Vdc	$V_m < V_{c2}$
3	S3	-Vdc, -2Vdc	$V_m < V_{c3}$
4	S4	Vdc, 2Vdc	$V_m > V_{c2}$
5	S5	0, Vdc, -Vdc, 2Vdc	$V_m > V_{c4}$
6	S6	0, Vdc, -Vdc, -2Vdc	$V_m < V_{c1}$
7	S7	-2Vdc	$V_m < V_{c4}$
8	S8	2Vdc	$V_m > V_{c1}$

4. Performance Comparison of the HERIC Multilevel inverter with Conventional HERIC

To evaluate the improved performance and to compare the quality parameters of the proposed and the conventional HERIC topology, Simulink / MATLAB software simulation is performed by building a simulation model of each topology. Each model is tested with the same value for the modulation index (m_a), input voltage, filter size, load magnitude, and switching frequency level. Furthermore, the power quality parameters that are harmonics produced by both inverters are measured and compared. Another parameter that is compared is the power losses that occur during the operation of both topologies. Power losses include conduction losses and switching losses [14].

Conduction losses are power losses that arise as a result of the condition of the switch during conducting (on). To analyze these losses, the current and voltage equation on the inverter component where the dominant power loss occurred, i.e. on the switch components, is first modeled. A switch component can be modeled as a linear transistor in series with a voltage source, so:

$$V_{ce} = V_q + i_q \cdot R_q \dots\dots\dots (1)$$

and for the diode:

$$V_{ak} = V_d + i_d \cdot R_d \dots\dots\dots (2)$$

Here, the V_{ce} is the voltage drop on the switch, V_{ak} voltage drop on the diode, i_q is current on the switch, i_d is current in the diode. The parameters V_q , R_q , V_d , and R_d can be found on the component datasheet. From this equation, the power loss in a component is calculated by multiplying the effective voltage drop and current. Square of effective current multiplication to the component's resistance results in resistor power loss in both components. For this approach, the current on the switch, diode, and the load are assumed to be sinusoidal, so that the effective current is calculated by the equation:

$$I_q(\text{avg}) = I_0(pk) \left[\frac{1}{2\pi} + \frac{ma \cdot \cos \phi}{8} \right] \dots\dots\dots (3)$$

$$I_q(\text{rms}) = I_0(pk) \left[\sqrt{\frac{1}{8} + \frac{ma \cdot \cos \phi}{8}} \right] \dots\dots\dots (4)$$

$$I_d(\text{avg}) = I_0(pk) \left[\frac{1}{2\pi} + \frac{ma \cdot \cos \phi}{8} \right] \dots\dots\dots (5)$$

$$I_d(\text{rms}) = I_0(pk) \left[\sqrt{\frac{1}{8} - \frac{ma \cdot \cos \phi}{3\pi}} \right] \dots\dots\dots (6)$$

$I_0(pk)$ is the loads peak current, ϕ is power angle, m_a is the modulation index. Simply, the conduction losses on switches ($P_{(q\text{-con})}$), and in diodes $P_{(d\text{-con})}$ can be expressed as:

$$P_{q\text{-con}} = V_q \cdot I_q(\text{avg}) + R_q \cdot I_q(\text{rms})^2 \dots\dots\dots (7)$$

$$P_{d\text{-con}} = V_d \cdot I_d(\text{avg}) + R_d \cdot I_d(\text{rms})^2 \dots\dots\dots (8)$$

It must be noted; the above equations are to calculate the losses contained in a switch and a diode. To calculate total losses on all switches and diodes, it is calculated using the equation:

$$P_{\text{tot-con}} = n(P_{q\text{-con}} + P_{d\text{-con}}) \dots\dots\dots (9)$$

Here, $P_{\text{tot-con}}$ is the total conduction losses and n is the number of switches and diodes in the inverter.

Switching losses are the power losses resulting from the process during transition conditions. It occurs during the turn-on, turn-off condition and reverse discovery processes on diodes. This loss can be obtained from the switching energy value as in the components data sheet as well as from the conventional test of voltage and current (V_{test} and I_{test}). Generally, there is a value of turn-on and turn-off energy of the switch (E_{on} and E_{off}). Thus, the total energy used during the switching process follows the equation:

$$E_{\text{tot}} = Kg \cdot (E_{\text{on}} + E_{\text{off}}) \cdot \frac{V_s}{V_{\text{test}}} \cdot \frac{I_0(pk)}{I_{\text{test}}} \dots\dots\dots (10)$$

E_{tot} is the total energy during switching condition and the K_g is a correcton factor. Total losses during the switching process can be calculated using the following equation:

$$P_{tot-sw} = n f_s \left(\frac{E_{tot}}{\pi} \right) \dots\dots\dots (11)$$

Where $P_{(tot-sw)}$ is total losses during the switching process and f_s is the PWM switching frequency. Finally, the total losses in the switch can be calculated by adding up the conduction losses and switching losses:

$$P_{tot(inv)} = P_{tot-sw} + P_{tot-sw} \dots\dots\dots (12)$$

The comparison of the power losses of the two inverters is done by comparing the power losses when the THD output of each inverter is the same value. At the same THD value for the two inverters, the switching frequency of each inverter is recorded and used to calculate the power losses on the switch as the equation (1 - 12)

4.1. Simulation of HERIC Inverter 5-level

The HERIC inverter testing is performed using the power circuit and control model as in Figure 4 and 5, the values of the component described in Table 4.

Table 4. Parameter of HERIC inverter 5-level

No	Components	Value	Amount
1	V_{dc}	100 Volt	2 pcs
2	switching Frequency	2500 Hz	-
3	Modulation index	0.95	-
4	Filter L	30 mH	2 pcs
5	Filter C	1,6 μ F	1 pcs
6	Resistor (linier load)	100 Ohm	1 pcs

By using these values, a voltage and current waveform at the 5-level HERIC inverter output is obtained as shown below:

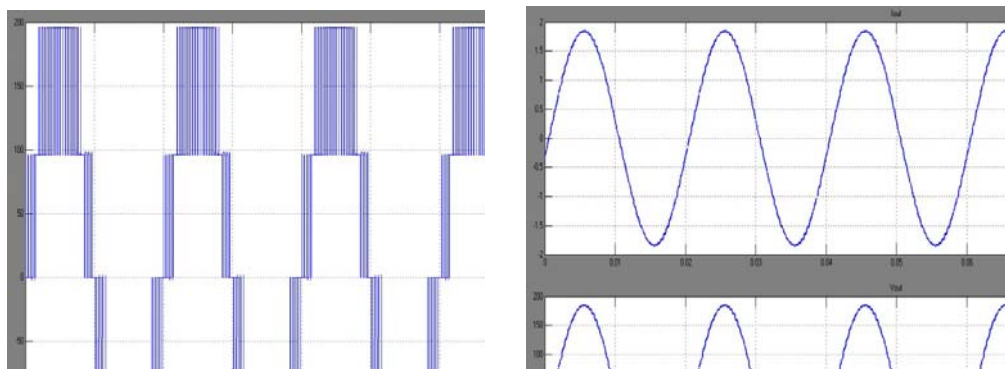


Figure 6. The output voltage of the HERIC inverter 5-level without (left) and with (right) output filter

Waveform the form of the inverter output voltage and current with the addition of a filter makes the output waveform more sinusoidal. The THD inverter will be evaluated at the inverter output with an additional filter. In Figure 7, it can be seen that the THD of the 5-level HERIC inverter output is 1.23%.

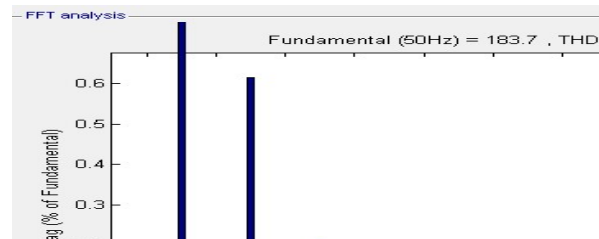


Figure 7. Total harmonics distortion on the voltage output of HERIC inverter 5-level
The following is the distortion value of HERIC inverter 5-level for various switching frequency values, modulation index, and load.

4.2. Simulation of Conventional HERIC Inverter topology

Conventional HERIC inverter testing is done as a comparison against 5-level HERIC inverters. The simulation test is carried out with the same variable values of the 5-level HERIC inverter as in Table 4. The only difference is in the number of DC sources used. In conventional HERIC inverters only use one DC source, as shown in Figure 8.

Table 5. THD as the function of switching frequency, modulation index and a load of HERIC Inverter 5-level

No	Switching Frequency	Distortion	Modulation index	Distortion	Load	Distortion
	Fs (Hz)	THD %	m	THD %	R (Ohm)	THD %
1	1000	5,93	0,6	1,52	10	0,78
2	2500	1,23	0,7	1,55	100	1,23
3	5000	0,7	0,8	1,5	1000	1,37
4	7500	0,66	0,9	1,31	5000	1,46
5	10000	0,65	1	1,12	10000	1,88

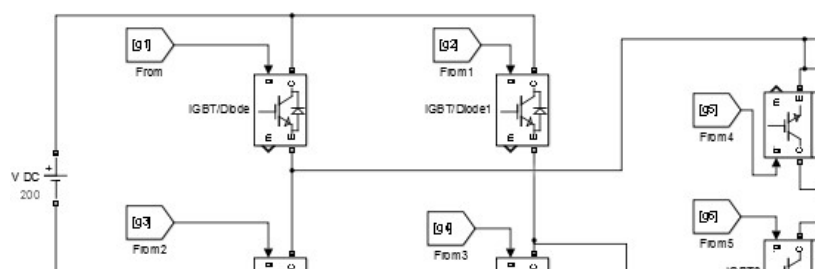


Figure 8. Simulation circuit of the conventional HERIC inverter

In this simulation, the same variable as was varied in the previous 5-level HERIC inverter simulation is also done. Following are the results of conventional HERIC inverters with variations of the variables:

Table 6. THD as a function of switching frequency, modulation index and a load of Conventional HERIC

No	Switching Frequency Fs (Hz)	Distortion THD %	Modulation index m	Distortion THD %	Load R (Ohm)	Distortion THD %
1	1000	16,45	0,6	16,07	10	4.36
2	2500	11,4	0,7	14,74	100	11.89
3	5000	11,65	0,8	13,33	1000	22.80
4	7500	11,62	0,9	12,32	5000	28.27
5	10000	11,65	1	11,45	10000	28.67

4.3. Comparison of Multilevel HERIC Inverters with Conventional HERIC Inverters

This section shows the comparison between the two types of inverters that have been simulated above. The comparison will be shown in the form of graphs obtained from the test results data on the simulation of each inverter.

In the THD comparison, the two inverters have the same variable values according to the values listed in Table 4. Figure 9 shows clearly that THD of a 5-level HERIC inverter is much smaller than a conventional HERIC inverter.

Power losses for each inverter are calculated using eq.12. Power losses are compared with the assumption that both types of inverters use the same switch. Therefore the power loss calculation only considers the number of switches and switching frequencies used. The comparison was done in conditions when the two inverters produce the same THD level of 11.54%. In this condition, the 5-level HERIC inverter has a switching frequency ($f_s = 588\text{Hz}$), while conventional HERIC inverters have a switching frequency ($f_s = 5000\text{Hz}$). Also, both multilevel HERIC and conventional HERIC inverters have two switches operated on fundamental frequencies ($f_{\text{fund}} = 50\text{Hz}$). Therefore, the switching losses equation becomes:

$$P_{\text{tot-sw}} = n f_s \cdot \frac{E_{\text{tot}}}{\pi} \cdot 2 \cdot f_{\text{fund}} \cdot \frac{E_{\text{tot}}}{\pi} \dots \dots \dots (13)$$

or

$$P_{\text{tot-sw}} = (n f_s + 2 \cdot f_{\text{fund}}) \frac{E_{\text{tot}}}{\pi} \dots \dots \dots (14)$$

Where n is the number of switches operating at switching frequency, f_s is switching frequency, and f_{fund} is fundamental frequency. The total power losses for each inverter are as follows:

Power losses on inverter HERIC multilevel, P_{tot} (IHM):

$$P_{\text{tot}}(\text{IHM}) = P_{\text{tot-con}} + P_{\text{tot-sw}} = 10 \left(P_{\text{q-con}} + P_{\text{d-con}} \right) + \left((8 \times 588\text{Hz}) + (2 \times 50\text{Hz}) \cdot \frac{E_{\text{tot}}}{\pi} \right) P_{\text{tot}}(\text{IHM}) = 10 \text{ a} + 4804 \text{ b} \dots \dots \dots (15)$$

Power losses on the conventional HERIC inverter, P_{tot} (IHC):

$$P_{\text{tot}}(\text{IHC}) = P_{\text{tot-con}} + P_{\text{tot-sw}} = 6 \left(P_{\text{q-con}} + P_{\text{d-con}} \right) + \left((4 \times 5000\text{Hz}) + (2 \times 50\text{Hz}) \cdot \frac{E_{\text{tot}}}{\pi} \right) P_{\text{tot}}(\text{IHC}) = 6 \text{ a} + 20100 \text{ b} \dots \dots \dots (16)$$

Where:

$$P_{\text{q-con}} + P_{\text{d-con}} = \text{a} \quad (\text{conduction losses})$$

$$\frac{E_{\text{tot}}}{\pi} = \text{b} \quad (\text{switching losses})$$

From the calculations obtained, it can be seen that the 5-level HERIC inverter power loss has higher conduction losses than conventional HERIC, with a ratio of $10/6 = 1.66$. This happened because of the number of switches larger than the 5-level HERIC. However, the 5-level HERIC inverter switching losses are much lower with the ratio of $4.804 / 20100 = 0.24$ than in conventional HERIC. This means that conventional HERIC inverters have switching losses of almost four times higher than 5-level HERIC inverters. Conventional HERIC inverters require a high switching frequency to produce good waves which result in large power losses when compared to 5-level HERIC inverter.

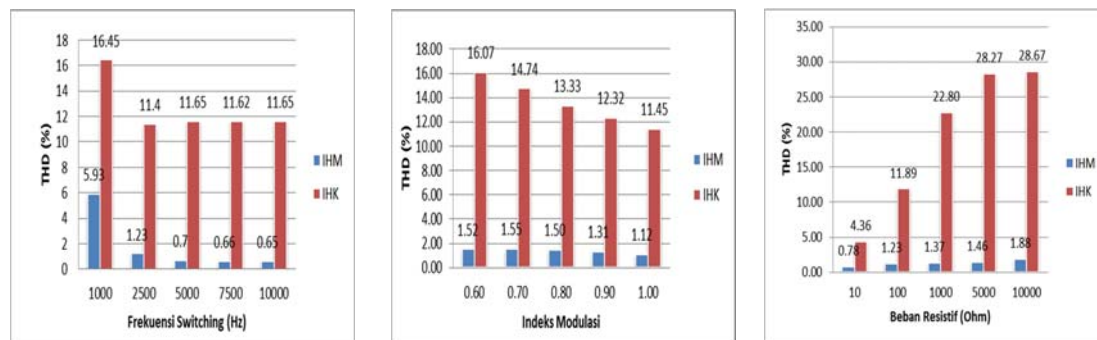


Figure 9. Distortion comparison due to the variation of Switching frequency, modulation and load level of Multilevel HERIC Inverters (IHM) and Conventional HERIC Inverters (IHK)

4.4 HERIC Multilevel Inverter and Cascaded H-Bridge Multilevel Inverter comparison

In this section, a comparison between a 5-level HERIC inverter and a 5-level cascaded H-Bridge inverter is made. A HERIC multilevel inverter is a cascaded H-Bridge inverter with additional back-to-back switches on the output side. Therefore, a comparison is made to see the effect of adding back-to-back switches to THD and the resulting power losses.

Comparison of the distortion effect is done by the same technique as the comparison with the previous conventional HERIC inverter, that is, by varying the switching frequency, modulation index, and load. The figure shows that the THD of both inverters are lower if the switching frequency is increased, but THD of the HERIC multilevel inverter is lower along the frequency range. By varying the modulation index, multilevel inverter shows distortion level higher than the HERIC along the variation range. In loading variation, averagely multilevel HERIC inverter shows distortion level higher than the cascaded H-Bridge inverter.

Losses comparison between a multilevel HERIC inverter and a conventional multilevel inverter (both inverter using 5 level voltage) was performed during both inverter shows distortion as high 1.23% THD. In this condition, the switching frequency for multilevel HERIC is 2500Hz and multilevel inverter is 2639,3Hz. The following is the loss calculation for both inverter: For inverter HERIC 5-level, it has eight switches that are operated with a switching frequency and 2 switches operated at the fundamental frequency (50Hz), so the power loss equation becomes:

$$\begin{aligned}
 P_{\text{tot}} &= P_{\text{tot-con}} + P_{\text{tot-s}} \\
 &= 10(P_{\text{q-con}} + P_{\text{d-con}}) + \left((8 \times 2500\text{Hz}) + (2 \times 50\text{Hz}) \cdot \frac{E_{\text{tot}}}{\pi} \right) \\
 &= 10(P_{\text{q-con}} + P_{\text{d-co}}) + \left(20100 \cdot \frac{E_{\text{tot}}}{\pi} \right) \\
 P_{\text{tot}} &= 10 a + 20100 b \dots\dots\dots
 \end{aligned} \tag{17}$$

For inverter *cascaded H-Bridge*, only eight switches are operated at switching frequencies without additional switches such as multilevel HERIC inverters. So that the power loss equation becomes:

$$\begin{aligned}
 P_{\text{tot}} &= P_{\text{tot-con}} + P_{\text{tot-s}} \\
 &= 8(P_{\text{q-con}} + P_{\text{d-con}}) + \left((8 \times 2639,3\text{Hz}) \cdot \frac{E_{\text{tot}}}{\pi} \right) \\
 &= 8(P_{\text{q-con}} + P_{\text{d-con}}) + \left(21114,4 \cdot \frac{E_{\text{tot}}}{\pi} \right) \\
 P_{\text{tot}} &= 6a + 21114,4b \dots\dots\dots
 \end{aligned} \tag{18}$$

From the calculations obtained, it can be seen that the HERIC 5-level inverter has a higher conduction loss than conventional multilevel inverter with, which a ratio of 10: 8. In other words, a multilevel HERIC power loss of 1.25 times greater than a multilevel inverter. This happens because the number of switches is more than the 5-level HERIC due to the addition of the back-to-back switches.

In switching losses comparisons, the 5-level HERIC inverter and Cascaded H-Bridge have losses ratio as much as 20,100: 21,114.4 (multilevel HERIC inverters are 1.05 times larger). In general, the comparison shows that multilevel HERIC inverters have a slightly greater power loss than cascaded H-Bridge inverters.

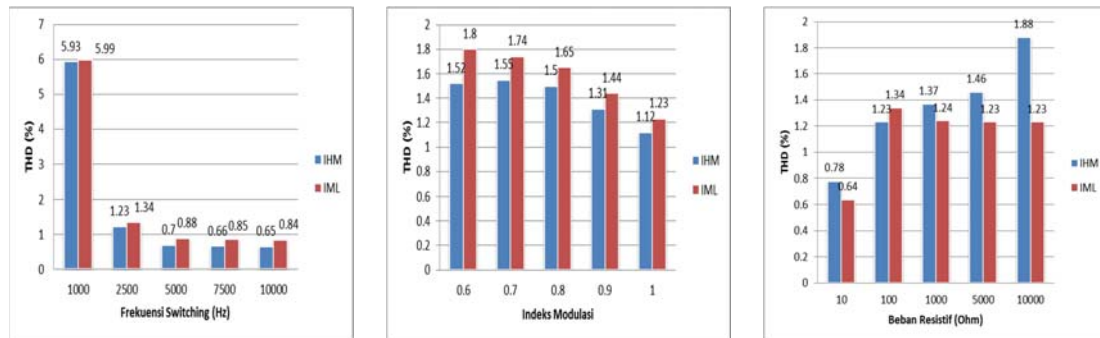


Figure 10. Distortion comparison due to the variation of Switching frequency, modulation and load level of Multilevel HERIC Inverters (IHM) and multilevel Inverters (IHK)

4.5 The Role of bidirectional switches in multilevel HERIC Topology Inverters

This section will explain the effect of bidirectional (back-to-back) switches owned by multilevel HERIC inverters. By its main function, this switch serves to prevent the exchange of reactive power when the inverter feeds an inductive load. In the simulation, the inverter is loaded by resistors and inductors. Then, the current on the source capacitor (C_{in}) and the back-to-back switch was monitored. The following figures show the difference between both currents.

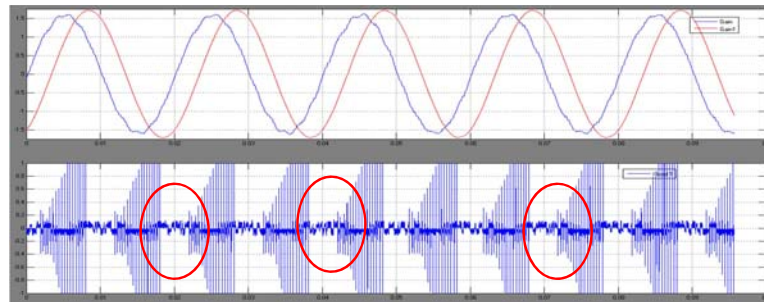


Figure 11. The current shape on source side capacitor during inverter operated with a back-to-back switch

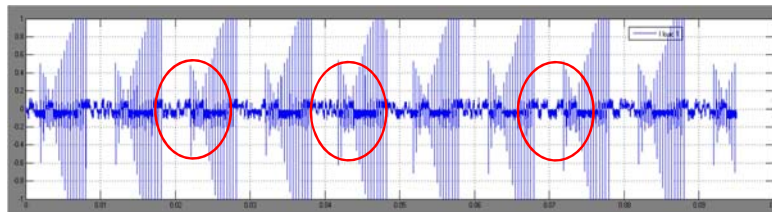


Figure 12. The current shape on source side capacitor during inverter operated without back-to-back switch

In the two figures, there is a slight difference in the current flowing in C_{in} . In inverter without back-to-back switches and loaded by a reactive load, the current in C_{in} is greater than the one with back-to-back switches. This happens because of the influence of bidirectional switches owned by HERIC inverters. At the HERIC inverter, the current will flow on the back-to-back switch as shown in figure 13. It is confirmed why the current to capacitor was reduced.

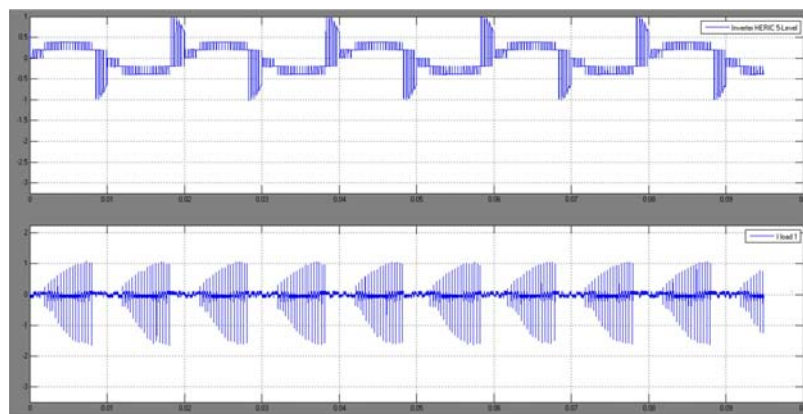


Figure 13. Current condition in bidirectional switches (upper) and source side capacitor C_{in} (lower) during inverter loaded by the reactive load

5. Conclusion

It has been described as a proposed schema to improve the performance of HERIC PV-inverter. The scheme is applying a multilevel to the original HERIC PV-Inverter topologies. Performance from the

aspects of power quality and losses that occur during the operation of the proposed inverter was compared to original multilevel and HERIC PV-Inverter.

From the experiments based on software simulation and also from calculations performed in this research, it is known that multilevel HERIC inverters had a lower distortion (THD) when compared to conventional HERIC inverters and cascaded H-Bridge inverters at the same switching frequency. In the same output quality conditions (THD), 5-level HERIC inverters have lower switching power losses than conventional HERIC inverters but have higher conduction losses. The higher the switching frequency, the lower the inverter output THD will be. The control signal circuit for multilevel inverters will be more complex at more voltage levels. Based on the result, it is seen that there is a trade-off between switching frequency and losses during operation the proposed topology, further research is needed to get the optimal condition.

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