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ESD protection circuit for V-band RF applications in a 65nm CMOS technology

Allenn C. Lowaton¹, Lemuel Fil L. Bañez²

Microelectronics Laboratory, Electrical Engineering and Technology Department,
Mindanao State University – Iligan Institute of Technology, Iligan City, Philippines

¹allenn.lowaton@g.msuiit.edu.ph; ²lemuelfilbanez@g.msuiit.edu.ph

Abstract. To apply radio frequency circuits, nanoscale CMOS technologies are greatly used but this consequence to a thinner gate oxide and silicided drain/source. With this, the electrostatic discharge (ESD) robustness of RF circuits will be much more degraded. Therefore, there is a need for an ESD protection circuit design in RF circuits against ESD damages. In this paper, the proposed ESD protection circuit is presented with concept based silicon-controlled rectifier (SCR) device, two diodes, PMOS transistor and an inductor to efficiently provide protection for radio-frequency (RF) circuits from ESD damages in nanoscale CMOS process. The concept based SCR device is aided with an inductor to provide efficient ESD path discharge to the SCR device. Moreover, the inductor is used to resonate out the parasitic capacitance generated by the ESD protection circuit at the preferred frequency. In addition, the proposed ESD protection circuit is implemented to a low noise amplifier (LNA) at 60-GHz frequency within an efficient area. Furthermore, the ESD protection circuit is simulated to achieve over 2-kV human body model ESD robustness with good RF performances on LNA in 65-nm CMOS technology.

1. Introduction

The increasing trend of wireless communication has been promising since the emergence of fast and compact smart phones in the global market. However, the use of these devices expressed some issues on effects of electrostatic discharge (ESD) on the devices performance and reliability. As the current technology advances, more concerns are raised on the association between ESD and decreasing size of devices [1]. In modern integrated circuits(IC), the problem of ESD has become the principal reliability issue as ICs are manufactured from fabrication to the use of consumers. ESD zapping can happen at any moment at different places and the trouble of ESD damages increases as thinner gate oxides and smaller diffusion junction arises [1].According to ESD Association, 25% of all electronics damaged with causes that were not known are designated to be an ESD related problem and around \$5 billion (USD) per



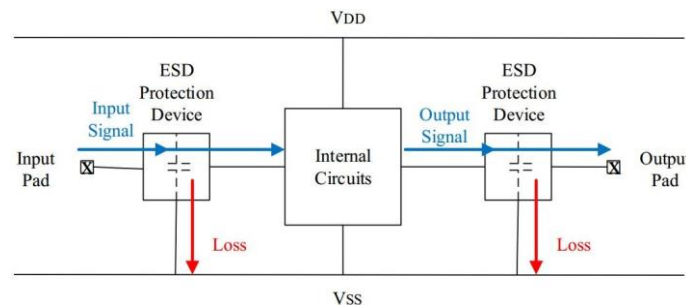


Figure 1. Signal Loss at I/O Pads of IC with ESD Protection Devices

year is the cost of ESD damage to the Electronics Industry [2]. The failures of CMOS are attributed to ESD damage which cost the IC industry billions of dollars [3], therefore the existence of ESD problems can no longer be neglected. To avoid electrostatic discharge, precautions were made and ICs should be capable to withstand ESD events for it to become reliable. Identifying the ESD susceptible devices and protect them with an ESD protection circuit should be included in the design process. Furthermore, designers should test the circuits with ESD protection to ensure its reliability under ESD stresses [1]. As stated in the International Technology Roadmap for Semiconductors (ITRS), the design of on-chip ESD protection circuit to radio frequency (RF) circuits rises as a primary challenge in its reliability and performance. Since RF ICs operate at high frequencies, these circuits are highly sensitive to any parasitic effects created by ESD protection structures which always affect the RF ICs performance [4]. One of the most important design considerations for RF circuits is the parasitic capacitance which comes from the addition of ESD protection devices. Using large device dimensions in conventional ESD protection circuit will have parasitic capacitance that is too large to be tolerated for RF circuit applications [5]. Figure 1 shows the effect of parasitic capacitance on ESD protection devices. The parasitic capacitance causes signal loss from the input/output pad to ground. Furthermore, it changes the input matching condition of the device which results in the deterioration of RF performance [5]. To lessen the performance degradation caused by the addition of ESD protection circuits, some design techniques have been developed to minimize its parasitic capacitance [5]. The ESD protection circuit with smaller parasitic capacitance can be easily co-designed or combined with RF circuits [6]-[7].

In this study, a new design approach is proposed for ESD protection circuit which will improve the ESD robustness of LNA under ESD events. Furthermore, a two-stage cascode topology is used for the LNA circuit which achieves high gain and good impedance matching. Both the proposed designs utilize the Synopsys IC design tools.

2. System architecture

The design of ESD Protection circuit is composed of two blocks, the SCR-Based ESD protection block and the Power-rail ESD clamp block. Furthermore, to evaluate the performance of the ESD protection circuit, a low noise amplifier block is used as the device under test. As shown in Fig. 2, the SCR-Based ESD protection serves as the main block of ESD protection circuit since it is connected with the input port while the power-rail ESD clamp circuit provides protection of the device under test from ESD events that flows between supply voltage and ground. Lastly, the low noise amplifier is the device under test that is ESD Protection Circuit Device under Test being protected using the proposed ESD protection design. The proposed system architecture is shown in Fig. 2.

2.1. SCR concept based ESD protection

Among the ESD protection devices, such as the diode, MOS, BJT or field-oxide device, silicon controlled rectifier (SCR) device has been revealed to be useful for RF ESD protection design due to its high ESD robustness within a small layout area and low parasitic capacitance [8]. Aside from that, the SCR device usually has a holding voltage of ~ 1.5 V in the bulk CMOS processes [9]. Furthermore, as the supply voltage (VDD) decreases in a 65-nm CMOS process, the SCR can be safely used without latchup danger [8]. Silicon Controlled Rectifier has a pnpn structure with two parasitic

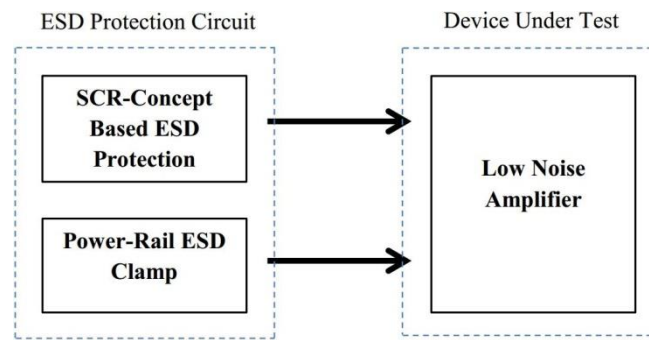
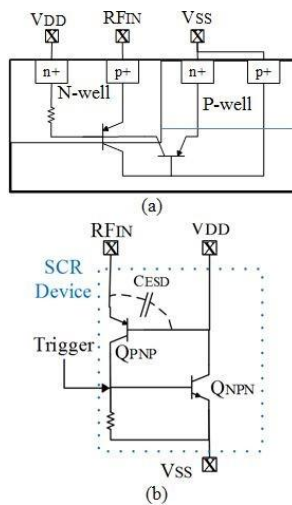
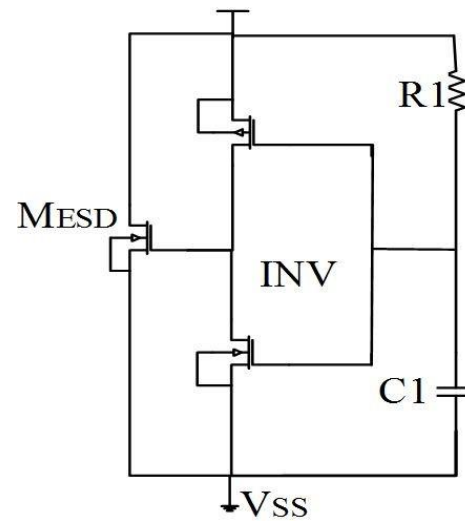
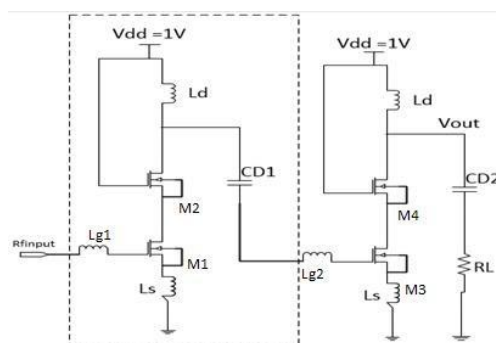
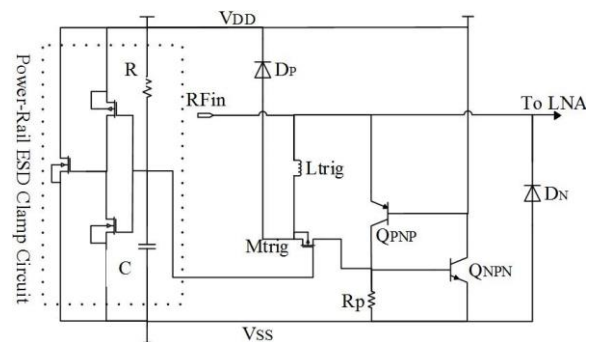
transistors. Fig. 3 shows the cross sectional view as well as the equivalent circuit of SCR device. The equivalent circuit of the SCR consists of a PNP BJT (Qnpn) and an NPN BJT (Qnpn), as shown in Fig. 3(b). The (Qnpn) is formed by the N-well, P-well, and N+ [11], and the (Qnpn) is formed by the P+, N-well, and P-well. By turning on the parasitic npn bipolar transistor due to avalanche breakdown generated current, the SCR is triggered. Furthermore, SCR has the capability to switch from high impedance state to low impedance state since the feedback mechanism keeps both the bipolar transistors on and therefore [1]. The SCR path between RFin and Vss consists of P+, N-well, P-well, and N+. Moreover, the parasitic diode path between RFIN and VDD consists of P+ and N-well/N+. When ESD zapping occurs from RFin to Vss, the positive-feedback regenerative mechanism of Qnpn and Qnpn of the SCR will be highly conductive making SCR very robust against ESD stresses [9]. Due to almost ideal conductivity modulation of SCR, it can conduct very high current with very low on resistance. SCR can efficiently discharge ESD current in both directions since it provides full voltage swing. Also, SCR has low parasitic capacitance, higher secondary breakdown current, I_{t2} , and smaller area which offer a favorable choice for ESD protection designs. However, the drawback of using SCR must be solved like higher first breakdown voltage and lower holding voltage (causes latch up) [8]. There have been various modified SCR designs that were developed to solve the disadvantages of SCR, making SCR the most preferred ESD protection device [1]. The trigger signal can be sent to enhance the turn-on speed to reduce the trigger voltage of an SCR device. Some design techniques have been reported to enhance the turn-on efficiency of SCR devices [9]. However, adding a trigger circuit to SCR device also increases the parasitic capacitance seen at the RFIN pad, which is difficult to handle for RF and MMW circuit applications [11].

2.2. Power-Rail ESD clamp circuit

Figure 4 shows the power-rail ESD clamp circuit which is the discharge path of current under ESD events. The circuit is composed of the RC-inverter-triggered NMOS, which is used to provide ESD current paths between VDD and VSS under ESD stress conditions. The R1 (~10k) and C1 (~10 pF) having a time constant of 0.1 s to 1 s can determine the ESD transients from the normal circuit operating conditions. The NMOS (MESD) with ~3000- μ m width is used as the main ESD clamp device. The large-sized NMOS (MESD) is turned on to provide ESD current path from VDD to VSS when positive ESD stress occurs from VDD to VSS. Likewise, when negative ESD stress from VDD to VSS, the parasitic diode in large-sized NMOS (MESD) also provides the ESD current path from VSS to VDD. The power-rail circuit does not contribute parasitic effects to RF input port since the power-rail ESD clamp circuit is placed between VDD and VSS [10].

2.3. Two-Stage low noise amplifier

Figure 5 shows the cascode configuration of LNA. This configuration provides a good input-output isolation and the transistor M2 isolates the Miller capacitance. Furthermore, the input impedance is obtained using the source degeneration inductor L_s , while the gate inductor L_g sets the resonant frequency [12]. To achieve simultaneous noise and power matching, the inductive source degeneration is used. The values of this inductor is designed for both gain and stability considerations. The main design parameters of the input stage are the sizes of M1 and M3, the source inductor, L_s and the gate inductor L_g of Figure 5. The sizes are then determined based on optimization to enhance impedance matching as well as achieve enough power gain [12].

**Figure 2.** System Architecture**Figure 3.** (a) Device Cross-sectional View (b) Equivalent Circuit of SCR**Figure 4.** Power-Rail ESD Clamp Circuit**Figure 5.** Power-Rail ESD Clamp Circuit**Figure 6.** Proposed ESD Protection Circuit

2.4. Proposed ESD protection scheme

Figure 6 shows the proposed ESD protection circuit. The circuit uses an inductor-triggered SCR which consists of SCR architecture, an inductor, a MOS transistor and the RC-based ESD detection circuit coming from the power rail circuit block. The PMOS transistor exhibits the initial-on function for ESD protection, wherein, it can quickly pass the trigger signal to the SCR device. Under normal power-on conditions, the PMOS transistor is turned off to block the steady leakage current path from RFin to the trigger port of the SCR device. Meanwhile, during ESD stress conditions, the PMOS transistor is turned on so that the SCR device is quickly turned on to discharge the ESD current. The RC-based detection circuit coming from the power rail circuit is used to distinguish ESD stress conditions from normal circuit operating conditions with a time constant of 0.1 μ s to 1 μ s. The inductor is used to

provide trigger path between RFin and trigger port of the SCR under ESD stress conditions. Moreover, it is used to compensate the parasitic capacitance of the SCR device (CESD). In addition, diodes Dp and Dn complete the proposed ESD protection circuit [10].

The dimensions of the inductor, PMOS transistor, SCR device and diodes Dn and Dp can be designed to minimize the RF performance degradation. Since the capacitor used in power-rail ESD clamp circuit is large enough ($\sim 10\text{pF}$) to keep the node between R and C at ac ground, the impedance of trigger path seen at RFin to ground is calculated as;

$$Z_{\text{trig}} \approx j\omega L_{\text{trig}} + 1/j\omega(C_{\text{trig}} + C_{\text{dp}}) \quad (1)$$

$$Z_{\text{trig}} = j\omega(L_{\text{trig}} - 1/(\omega^2(C_{\text{trig}} + C_{\text{dp}}))) \quad (2)$$

where the ω is the angular frequency and the C_{trig} can be expressed as

$$C_{\text{trig}} \approx C_{\text{gs}} + C_{\text{gb}} + C_{\text{db}} \quad (3)$$

, C_{gs} denotes gate-to-source capacitance, C_{gb} denotes gate-to-body capacitance and C_{db} denotes drain-to-body capacitance of the PMOS transistor. The resonance angular frequency (ω_0), which is designed to be the operating frequency of RF signal, can be obtained by

$$\omega_0 = 1/((L_{\text{trig}} - 1/(\omega^2(C_{\text{trig}} + C_{\text{dp}})))(C_{\text{esd}})) \quad (4)$$

, where C_{esd} is the parasitic capacitance contributed by SCR and diode (Dn). Furthermore, solving for the value of L_{trig} , the equation becomes

$$L_{\text{trig}} = 1/(\omega^2 C_{\text{esd}}) + 1/(\omega^2(C_{\text{trig}} + C_{\text{dp}})) \quad (5)$$

The proposed circuit utilizes the impedance isolation technique where it uses the inductor L_{trig} to resonate out the parasitic capacitance generated by the ESD protection circuit. This technique is highly suitable for higher frequencies greater than 5-GHz and parasitic capacitance can be designed to be zero (ideally) at the desired frequency. The conventional ESD protection circuit consists of low capacitance diodes. The conventional diodes show that it is suitable only for lower frequencies (less than 5-GHz) but it is worst at high frequency applications. In contrast, the use of conventional diodes has smaller layout area compared to impedance isolation technique in the proposed circuit.

The proposed circuit is similar to the inductor-triggered SCR configuration but the only difference is the addition of diode Dp from the terminal of inductor from RFin pad to power supply VDD. The idea of adding a diode Dp comes from the circuit configuration where an ESD protection can be placed between one terminal of inductor to power supply VDD. From equation 5, the parasitic capacitance generated by diode Dp is inversely proportional to the size of the inductor L_{trig} . Knowing that the inductor contributes the largest area in layout design, it is important that the size of the inductor is small to save layout area as well as cost of fabrication. Thus, with the addition of diode (Dp), it will decrease the size of the inductor resulting to smaller layout area. Furthermore, diode Dp will provide another discharging path of ESD current/voltage when ESD zapping (PD-Mode) occurs from RFin pad to power supply VDD.

Figure 7 shows the ESD current paths under positive-to-Vss (PS), positive-to-VDD (PD), negative-to-Vss (NS), and negative-to-VDD (ND) ESD stress conditions. During positive-to-Vss (PS) ESD stress, ESD current will first pass through the inductor and PMOS to trigger the SCR device. The major ESD current will be discharged by the SCR device from the RFin pad to Vss. Under positive-to-VDD ESD stress, the ESD current will be discharged by the parasitic diode path embedded in the SCR device from the RFin pad to VDD. During negative-to-Vss (PS) ESD stress, the ESD current will be discharged by the forward-biased Dn from the Vss to RFin pad. Under negative-to-VDD (ND) ESD stress, the ESD current will be discharged by the power-rail ESD clamp circuit and the Dn from VDD to RFin pad. The proposed ESD protection scheme can provide the corresponding current discharging paths with good ESD robustness.

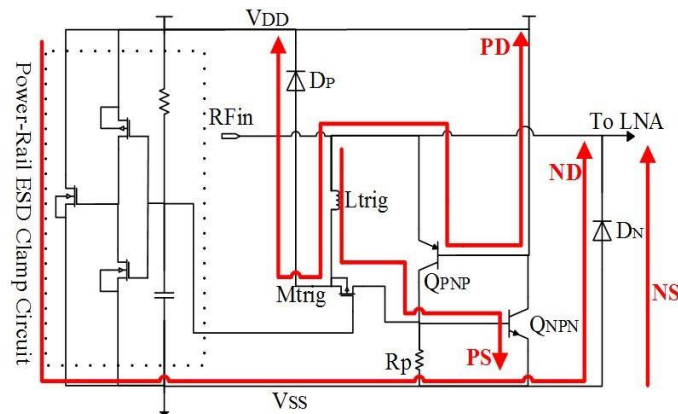


Figure 7. Proposed ESD Protection Circuit with ESD Zapping Modes

3. ESD simulations

3.1. S-Parameter simulation

The proposed ESD protection circuit will be simulated using the circuit in figure 8. The S-parameters S21 and S11 will determine the performance of the proposed ESD circuit design. The ideal value of S21 should be close to unity which indicates that no signal loss occurs during the simulation. Moreover, the desired value of S11 should be as small as possible to have good impedance matching.

3.2. ESD robustness simulation

Figure 9 is used to simulate the HBM model. The Ch capacitor is estimated to be the capacitance that comes from the human body, while the resistor Rh is estimated to be the resistance of the hands of the body as the person touches the device. Each component will be thoroughly investigated if the threshold voltage generated by each device/component exceeds the breakdown voltages. The device under test is composed of the low noise amplifier with the proposed ESD protection circuit. For LNA, the transistor M1, M2, M3 and M4 will be examined as shown in fig. 5. Whereas, diodes Dp and Dn, Ptrig, PNP and NPN bipolar transistors, as well as the NMOS and PMOS transistor in inverter and MESD transistor of the power rail circuit in fig. 4. The device under test is simulated with different values of voltage source of 2-kV, 4- kV, 6-kV and 8-kV to test the robustness of the device.

4. Simulation results of proposed ESD circuit

One of the most challenging parts in this study is the designing of the ESD protection circuit. The researcher has tried implementing different techniques and schemes to cancel out the parasitic capacitance which degrades the whole performance of the device under test. In the end, the researcher used an inductor to resonate out the parasitic capacitance at a high frequency. The proposed circuit has been designed in 65-nm CMOS process.

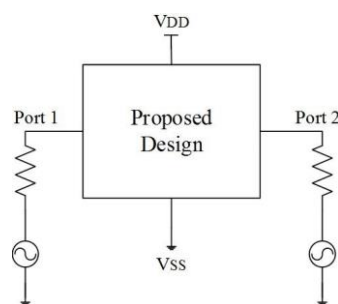


Figure 8. Schematic diagram for s-parameter simulation

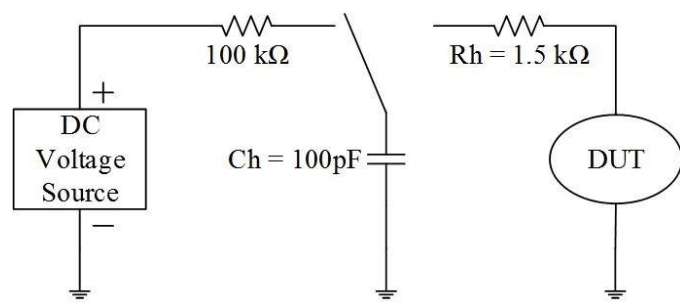


Figure 9. Schematic diagram for human body model simulation

4.1. Pre-Simulation

4.1.1 Circuit performance

Figure 10 shows the plot of the ESD protection circuits S parameters, obtained when the LNA circuit is not connected in the circuit. In the design, the ESD protection circuit achieved an S21 parameter of -0.473mdB and S11 parameter of -24.6dB. Due to the contribution of built-in parasitic capacitances of the circuit, the S21 parameter is not ideally equal to zero but it majorly cancels the parasitic capacitances. Furthermore, the ESD circuit is designed to operate at 60-GHz frequency. All the values of S11 parameter of the different process corners are less than -10 dB which indicates good impedance matching. Moreover, the S21 parameters have values that are close enough to each other which indicate a reliable performance under different process conditions.

4.1.2 ESD robustness

ESD induced failure is the effect when an ESD-sensitive device becomes part of the discharge path or when under the influence of high electrostatic field. One of the ESD induced failures is the dielectric breakdown. The researcher simulated the breakdown voltages of each component. According to Baker, the maximum electric field across a device gate is limited to 10MV/cm. This translates into 1V/10A of gate

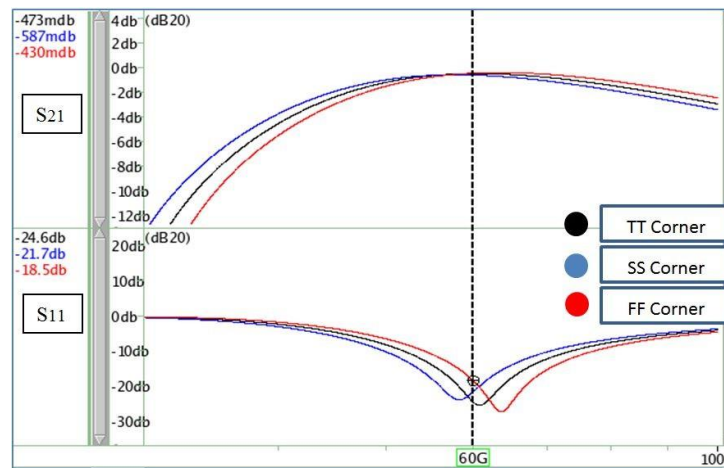


Figure 10. Graph of S-parameters (S21, S11)

oxide. Given in the BSIM 4 (v4.5) model of Synopsys Library, the CMOS transistor has tox or electrical gate equivalent oxide thickness of 30Å [13]. Thus, under supply voltage of 1V, the maximum allowed DC voltage that can be applied across the gate oxide is 3V based on the calculation below.

$$(1V/10A) * 30A = 3V \quad (6)$$

Table 1. Gate oxide breakdown voltage of MOS transistors

	Low Noise Amplifier				ESD Protection Circuit			
Dielectric	M1	M2	M3	M4	MEsd	Nch	Pch	Ptrig
BV	/3V/	/3V/	/3V/	/3V/	/3V/	/3V/	/3V/	/3V/

Table 2. Reverse breakdown voltages of diodes

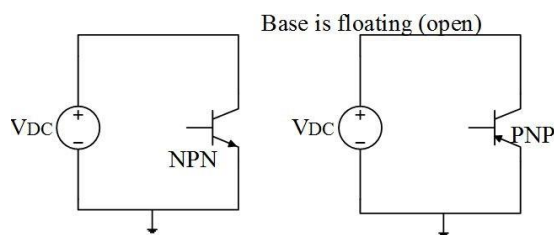
Reverse Breakdown Voltage of Diodes	
Dp	Dn
/10V/	/10V/

Table 3. Breakdown voltage of bipolar transistors

Breakdown Voltage of Bipolar Transistors	
NPN	PNP
6.8kV	2.87kV

Table 1 shows the gate oxide breakdown voltage of MOS transistors based on the calculation of equation 6. The threshold voltage V_{gs} of each transistor must not exceed the gate oxide breakdown voltage so that the transistor will not be damaged.

Table 2 shows the tabulated results of the reverse breakdown voltage of diodes Dp and Dn found in the proposed circuit. The reverse breakdown voltages of diodes are also shown in BSIM 4 (v4.5) Library used in simulating diodes. It is found out that, the reverse breakdown voltage is also -10V.

**Figure 11.** Circuit used in simulating the I-V characteristics curve of BJT**Table 4.** Pre-simulation HBM ESD results

Process Corner Variations			
	TT	SS	FF
PS HBM ESD Level (kV)	2	2	2
PD HBM ESD Level (kV)	6	4	8
NS HBM ESD Level (kV)	6	6	8
ND HBM ESD Level (kV)	4	4	4

The circuit used in simulating the I-V characteristic curve of BJTs is shown in figure 11. Based on simulations, the breakdown voltage BV_{CEO} , between collector and emitter when base is open is tabulated in table 3.

Table 4 shows the pre-simulation results of the ESD robustness level of the device under different process corners. The results passed the 2-kV level military standard of robustness. These results come from the simulated circuit of figure 9.

A PS HBM ESD level of 2-kV means that the components of the proposed circuit withstand a 2-kV voltage supply without exceeding the breakdown voltages on each component. The breakdown voltages are determined for MOS transistor, diodes and BJTs of the proposed circuit with the LNA configuration. The same applies for PD Mode, NS Mode and ND Mode. Notice that all ESD zapping modes passed the 2kV military standard.

4.2. Post-simulation

4.2.1 Circuit Performance

Figure 12 shows the results of post-simulations of the proposed ESD circuit. Notice that, the TT, SS and FF process corners have values of S21 and S11 that are close to each other. Among the S21 parameters, the FF corner has the least value which is close to the desired value of unity. All of the S11 values are less than -10 dB which indicates that the circuit has good impedance matching.

4.2.2 ESD robustness

Table 5 shows the post-simulation results of Human Body Model. Notice that the results showed that at each process variation, it passed the military standard that HBM ESD level must be greater than or equal 2-kV. These results are simulated using figure 9. Like the pre-simulated values, the post-simulated values depend on the ability of each component/device (from the proposed ESD circuit with LNA) to withstand a large amount of voltage (2-kV, 4-kV, 6-kV and 8-kV). The component can withstand the voltage if the threshold voltage generated will not exceed to the breakdown voltages. For MOS transistors in LNA, the breakdown voltage is 3V, whereas for diodes in ESD protection

circuit, the breakdown voltage is $|10V|$. For BJTs, the breakdown voltage is $|6.8kV|$ and $|2.87kV|$ for NPN and PNP respectively.

Voltage generated will not exceed to the breakdown voltages. For MOS transistors in LNA, the breakdown voltage is $3V$, for diodes in ESD protection circuit, the breakdown voltage is $|10V|$. For BJTs, the breakdown voltage is $|6.8kV|$ and $|2.87kV|$ for NPN and PNP respectively.

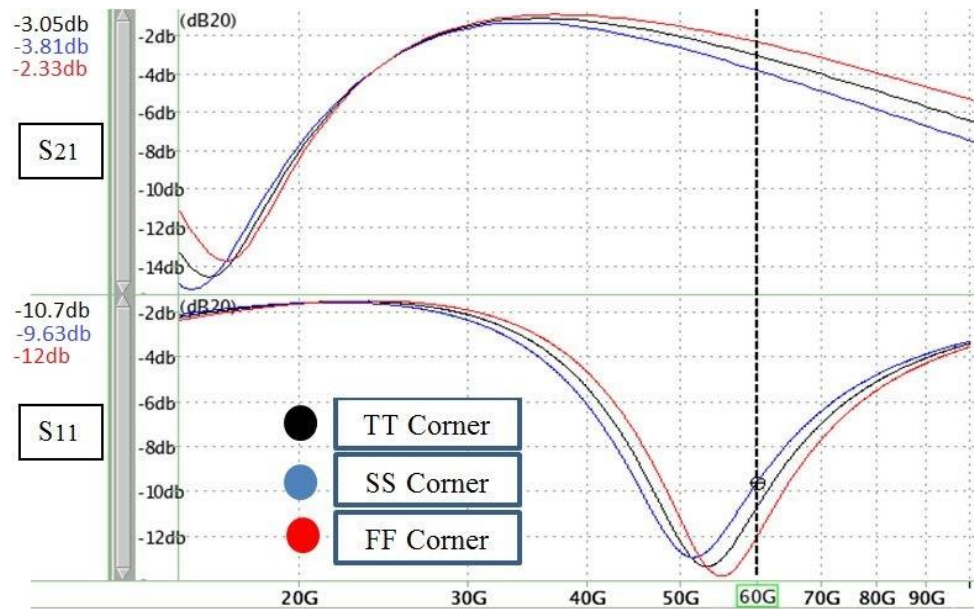


Figure 12. S-Parameters of Post-simulations of Proposed ESD Circuit

Table 5. Post-sim HBM ESD results

Process Corner Variations			
	TT	SS	FF
PS HBM ESD Level (kV)	2	2	4
PD HBM ESD Level (kV)	2	4	4
NS HBM ESD Level (kV)	2	8	8
ND HBM ESD Level (kV)	2	6	8

Table 6. Presim versus Post-sim HBM ESD results

Process Corner Variations						
	Pre-simulation			Post-simulation		
	TT	SS	FF	TT	SS	FF
PS HBM ESD Level (kV)	2	2	2	2	2	4
PD HBM ESD Level (kV)	6	4	8	2	4	4
NS HBM ESD Level (kV)	6	6	8	2	8	8
ND HBM ESD Level (kV)	4	4	4	2	6	8

4.3. Pre-simulation versus Post-simulation

Figure 13 shows the pre-simulation and post-simulation of the S-Parameters of the ESD protection circuit. For S21 parameter, the pre-simulated value is -472mdB which is close to the ideal value of unity or 0-dB . A 0-dB value of S21 parameter means that there is no loss in applying the ESD Protection circuit. The post-simulation value is -3.1dB which is mainly due to the parasitic capacitance and parasitic inductance generated by the layout design of the circuit. Furthermore, the S11 parameter must be as small as possible to have good impedance matching. Since both the pre-simulation and post-simulation values of S11 are less than -10dB , then, both results indicate good impedance matching.

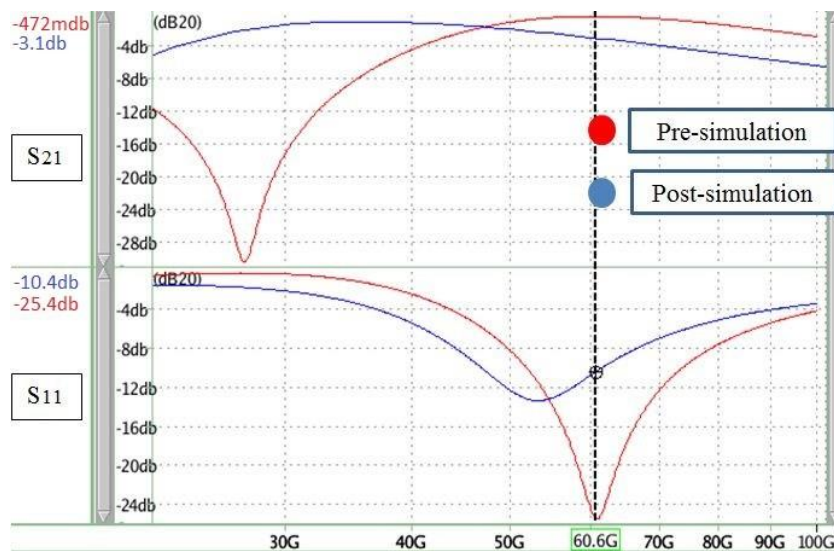


Figure 13. Pre-simulation and Post-simulation Results of ESD Protection Circuit

Table 6 shows the pre-simulation and post-simulation values of HBM level. From the results, all corners pass the 2-kV requirement of the military standard. It can be inferred that the proposed ESD protection circuit can withstand 2-kV of power supply if fabricated. Figure 14 shows the pre-simulation and post-simulation of the LNA performance with ESD circuit. The pre-simulated value of S21 parameter is 13.4dB. However, the post-simulated value becomes 12.4dB. The results showed that there is a loss in gain or S21

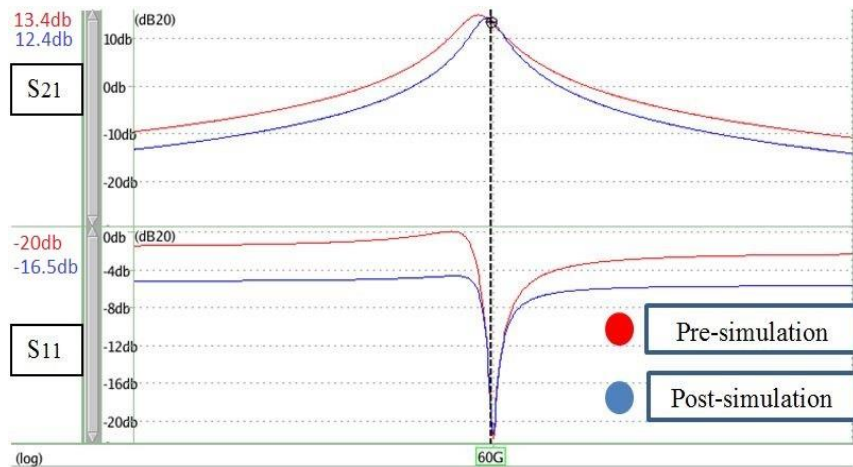


Figure 14. Pre-simulation and Post-simulation Results of LNA with ESD Circuit

parameter by 1dB. This is mainly due to the parasitic capacitances introduced by the ESD protection circuit. Moreover, the post-simulation value of S11 parameter of the LNA with ESD circuit becomes higher from -20dB to -16.5dB. Same reason applies as the S21 parameter which is caused mainly by the parasitic capacitance introduced by the ESD protection circuit. Parasitic capacitances from the ESD protection circuit will cause signal loss of the RF input signal.

4.4. Assessment between L_{trig} , D_p and D_n

To show the relationship of the components of the proposed circuit and its impact to its performance, an assessment is needed to verify the concepts presented in related literature and methodology. Table 7 shows three cases where the values of L_{trig} , D_p and D_n are changed to its optimum ESD performance level which is designed at 60-GHz frequency. Notice that as the value of L_{trig} increases,

the value of D_p and D_n decreases as shown in the decrease in value of multiplier. Thus, a larger value of L_{trig} is needed to cancel out the parasitics generated by smaller D_p and D_n . However, as the device/component becomes larger in size, it increases the parasitic capacitance but it becomes more robust to ESD stress/events [10]. Figure 15 shows the simulated S_{21} and S_{11} parameters of the three different cases presented. As observed in figure 15, all cases are designed to efficiently function at 60-GHz frequency. Table 8 summarizes the results shown in figure 15. Table 8 shows the tabulated results of figure 15. The ideal value of S_{21} is unity or 0dB, whereas S_{11} should be small enough to have good impedance matching. Among all cases, case 3 offers the best performance having the closest S_{21} parameter of the ESD protection circuit to 0dB. Also, case 3 has the smallest S_{11} parameter. However, the drawback of case 3 is the increasing size of the inductor which poses the highest layout area of approximately 150um x 180um. In contrast, the ESD circuit used in this paper is case 1 which has the least S_{21} parameter but comparable to the other cases. Also, all three cases pass the requirement of S_{11} parameter that is -10 dB, to have a good impedance matching according to [10]. Thus, from the results, the performance of the ESD protection circuit is inversely proportional to the layout area knowing the inductor has the largest exposure of area. As the value of inductor increases, the performance of ESD circuit is better but the layout area increases.

Table 7. Different values of L_{trig} , D_p and D_n

	L_{trig} (nH)	D_p	D_n
Case 1	0.11	$W/L = 0.9\mu/20\mu$, $M = 9$	$W/L = 0.9\mu/20\mu$, $M = 3$
Case 2	0.2	$W/L = 0.9\mu/20\mu$, $M = 4$	$W/L = 0.9\mu/20\mu$, $M = 2$
Case 3	0.2	$W/L = 0.9\mu/20\mu$, $M = 1$	$W/L = 0.9\mu/20\mu$, $M = 1$

Table 8. Simulation Results on S_{21} , S_{11} and area

	S_{21}	S_{11}	Layout Area of ESD
Case 1	-473 mdB	-24.6 dB	95um x 120um
Case 2	-339 mdB	-27.9 dB	125um x 150um
Case 3	-257 mdB	-30.7 dB	150um x 180um

4.5. Layout Design

Figure 16 shows the layout design of the ESD protection circuit without the power rail circuit. The layout area of the proposed design is 95um x 120um. Figure 17 shows the whole layout of ESD protection circuit. It can be observed from the figure that the area mainly depends on the size of the inductor and the capacitor.

4.6. Comparison among ESD protection circuits

Table 9 shows the comparison results of the designed ESD protection circuit compared with other references. Among all ESD protection circuits presented, Ref. [10] has the best S_{21} parameter while Ref. [8] has the best S_{11} parameter. However, the layout of the proposed circuit has 12% reduction in area of Ref. [8] and Ref. [10] papers. Among the ESD protection circuits, this study has the lowest area but also has the least S_{21} parameter of -3.1 dB. Furthermore, among all ESD circuit, this work has the highest value of S_{11} parameter with the value of -10.4 dB. Nevertheless, it still has good impedance matching. The performance of the proposed ESD protection circuit is dependent on the parasitic capacitance and parasitic inductance of the different elements in the circuit itself. Moreover, the proposed ESD protection circuit passed the military standard requirement of ESD robustness which is 2-kV based on simulations.

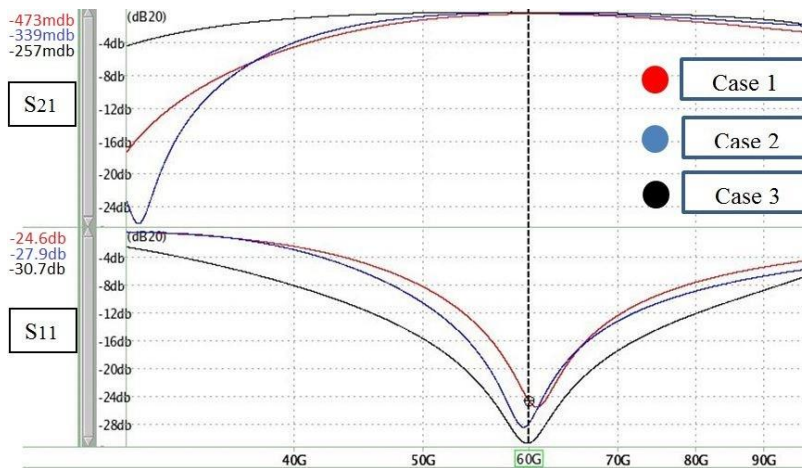


Figure 15. Simulated S21 and S11 Parameters of Three Cases

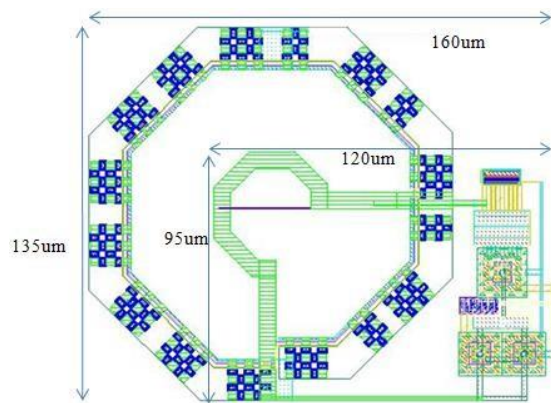


Figure 16. Layout Design of ESD Protection Circuit without Power Rail Circuit

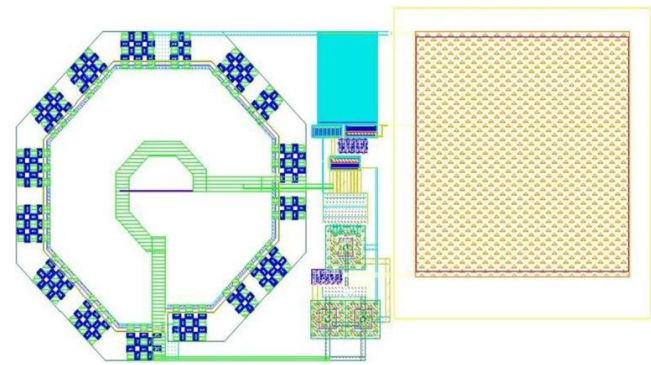


Figure 17. Layout Design of ESD Protection Circuit with Power Rail Circuit

5. Conclusion

This study completes the design of a compact ESD protection circuit for V-band RF applications in a 65-nm CMOS process. The ESD protection circuit is developed to help RF circuit designers for them to easily apply ESD protection circuit in 60-GHz RF circuits. The proposed ESD protection circuit uses an inductor triggered SCR concept based circuit as well as ESD protection diodes which are provided in the commercial CMOS process. The ESD protection circuit is then applied to the low noise amplifier circuit to determine its performance. However, for an integrated circuit to be reliable; the IC should be capable to manage the ESD events that occur from manufacturing process to end user. Testing and characterizing the circuits to guarantee the reliability of ESD circuits is one concern for designers. In the study, the robustness of ESD protection circuit was simulated and can achieve the 2-kV HBM ESD level. Based on the simulated result, the ESD protection circuit can achieve the required 2-kV ESD robustness condition in military standard if fabricated. In addition, the proposed ESD protection circuit is compact and area efficient, which is a useful solution for on chip ESD protection design in 60-GHz RF applications to save fabrication cost. The layout chip area of the ESD protection circuit is 95 μm x 120 μm which has 12% reduction of area compared to related references. Despite of having an efficient area, the ESD protection circuit attained a low S11 parameter of less than -10 dB which indicates good impedance matching but due to parasitic capacitance and parasitic inductance in the layout process, the simulated S21 parameter is -3 dB which presents a drawback in the study. Nevertheless, this result is comparable due to the LNA with ESD performance which has

small degradation in performance. Therefore, the proposed ESD protection scheme can be widely used to achieve high ESD robustness within small layout simultaneously.

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References

- [1] D. Raju, *Study of ESD Effects on RF Power Amplifiers*, May 2011.
- [2] R. Strube, *Challenges of Electro-Static Discharge (ESD) in the Electronics Industry*, Retrieved from <http://www.uic.com/challenges-of-electro-static-discharge-esd-in-the-electronics-industry/> 2015.
- [3] A. Wang, *On-Chip ESD Protection for Integrated Circuits, an IC Design Perspective*, Norwell, MA: Kluwer Academic Publishers, 2002.
- [4] A. Wang, *ESD + RFIC Co-Design for Whole-Chip Design Optimization*, Retrieved from <http://www.asqed.com/English/Archives/2010/Tutorials/> 2010.
- [5] M. Ker, C. Lin, Y. Hsiao, *Overview on ESD protection designs of low parasitic capacitance for RF ICs in CMOS technologies*, IEEE Trans. Device Mater. Reliab., vol. 11, no. 2, pp. 207218, 2011.
- [6] W. Soldner, M. Streibl, U. Hodel, M. Tiebout, H. Gossner, D. SchmittLandsiedel, J. Chun, C. Ito, R. Dutton, *RF ESD protection strategies Codesign vs. low-C protection*, Microelectron. Reliab., vol. 47, no. 7, pp. 10081015, 2007.
- [7] V. Vassilev, S. Thijs, P. Segura, P. Leroux, P. Wambacq, G. Groeseneken, M. Natarajan, M. Steyaert, H. Maes, *Co-design methodology to provide high ESD protection levels in the advanced RF circuits*, in Proc. E OS/ESD Symp., pp. 19, 2003.
- [8] C. Lin, L. Chu, M. Ker, *ESD protection design for 60-GHz LNA with inductor-triggered SCR in 65-nm CMOS process*, IEEE Trans. Microw. Theory Tech., vol. 60, no. 3, pp. 714723, 2012.
- [9] M. Ker, K. Hsu, *Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits*, IEEE Trans. Device Mater. Rel., vol. 5, no. 2, pp. 235249, 2005.
- [10] C. Lin, L. Chu, S. Tsai, M. Ker, *Design of Compact ESD Protection Circuit for V-Band RF Applications in a 65-nm CMOS Technology*, 2012.
- [11] L. Chu, C. Lin, M. Ker, *Design of Dual-Band ESD Protection for 24-/60-GHz Millimeter-Wave Circuits*, 2013.
- [12] A. Karanicolas, *A 2.7-V 900-MHz CMOS LNA and Mixer*, IEEE J. Solid-State Circuits, vol. 31, pp 1939 1944, 1996.
- [13] R. Baker, *CMOS: Circuit Design, Layout, and Simulation*, Third Edition, 2010.
- [14] C. Lin, L. Chu, M. Ker, *Design and implementation of configurable ESD protection cell for 60-GHz RF circuits in a 65-nm CMOS process*, Microelectron. Reliab., vol. 51, no. 8, pp. 13151324, Aug. 2011.