Design of Ultrasonic Guided Waves Signal Generator Based on FPGA

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Design of Ultrasonic Guided Waves Signal Generator Based on FPGA

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Abstract. Ultrasonic guided waves have been widely concerned in recent years due to their long transmission distance, wide coverage, and no influence on production. In the future, they have great potential to become a new descaling method widely used in industry. Piezoelectric ultrasonic transducer is an actuator based on ultrasonic guided waves descaling system, which requires high-precision signal source to drive. This paper designs a high-precision signal generator based on FPGA. The DDS signal generator based on FPGA and the ultrasonic guided waves descaling system based on FPGA are introduced. Through theoretical analysis and experimental verification, the test results show that the FPGA-based signal generator can generate the required excitation signal, and the FPGA-based ultrasonic guided waves descaling system proposes a new descaling method for the industry.

1. Introduction

Ultrasonic guided waves (UGW) have been used for testing due to the longer coverage distance. In 2004, Alleyne[1] had proven that UGW can be used for long-distance detection of sludge and blockages in chemical plant pipeline. The potential of the UGW on a long-distance cleaning have been mentioned by some researcher. In 2006, Nakagawa[2] had used ultrasound vibration for descaling a 192 mm long unfilled tube. This paper presents an FPGA-based ultrasonic guided waves pipeline descaling system. To some extent, the most important of the system is driver and the driver requires a high-precision signal generator. Generally, the signal generator is usually composed by using a discrete component or a monolithic dedicated integrated chip. However, this design method has the disadvantages of low frequency, poor stability and complicated circuitry[3]. With the continuous development of Field Programmable Gate Array (FPGA), the application of Direct Digital Frequency Synthesizer (DDS) technology is becoming more mature, and the DDS principle can be used to develop high performance waveform signal generator on the FPGA platform. Compared with the traditional signal generator, this design has the advantages of low cost, simple operation, and online update[4]. This paper proposes a signal generator system that meets the high performance requirements based on FPGA development platform, and proposes a new idea for of ultrasonic guided waves descaling method.

2. FPGA-based ultrasonic guided waves descaling system

In order to meet the requirements of ultrasonic guided wave descaling system signal source, this paper uses Verilog HDL code to implement DDS function on FPGA and generate excitation signal source, and then convert digital signal into analog signal through digital to analog converter (DAC). Finally, it is sent to the power amplifier to generate the target excitation voltage signal to drive the piezoelectric sensor (PZT) to realize the function of ultrasonic guided wave descaling. The composition of ultrasonic guided wave descaling system based on FPGA is shown in figure 1.

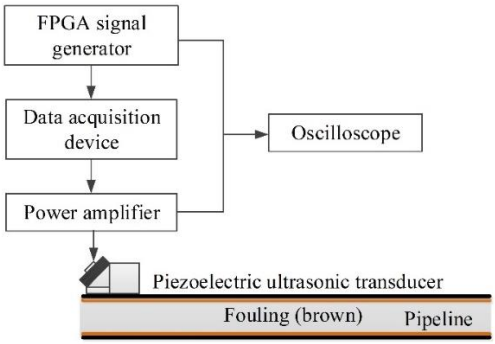


Figure 1. FPGA-based ultrasonic guided wave descaling system.

3. FPGA-based DDS signal generator

3.1. Overall program

The signal source of the descaling system in this paper is based on FPGA development platform and DDS technology to realize the signal generator, that is, the FPGA-based DDS signal generator design to meet the multi-waveform output of the predetermined parameter. The overall structure of the FPGA-based signal source generator is shown in figure 2. The FPGA-based signal source generator is mainly realized by FPGA development platform and code program. It is modeled by QUARTUS development tool and Verilog HDL program and verified by ModelSim simulation software. It is mainly composed of a key input module, a DDS control module, an IP core storage module and a display module.

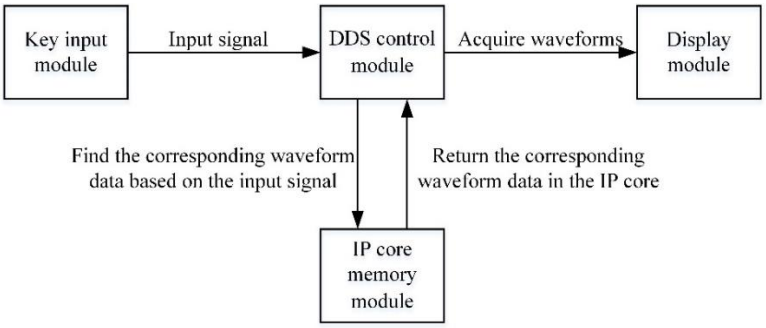


Figure 2. Signal source generator structure.

ALTERA Cyclone IV E series development platform was used in this article, and FPGA chip model is EP4CE6F17C8, with rich resources to meet the needs of this paper.

3.2. Theory

Suppose the expression of the sinusoidal signal is as follows：

$$y = A\sin(\varphi + \varphi_0) \quad (1)$$

Equation 1 can be transformed into:

$$y = A\sin(2\pi ft + \varphi_0) = A\sin 2\pi(ft + \varphi_0 / 2\pi) \quad (2)$$

Where: φ is the phase of the sine function, and φ_0 is the initial phase of sine function.

If the sine signal is digitally synthesized, the phase must be sampled. If the binary sample bit number of a periodic phase is N, then the sampling resolution is 2^N, and the sampling time interval is expressed as:

$$\Delta t = T / 2^N = 1/(f_0 2^N) \quad (3)$$

$$t = n \cdot \Delta t \quad (4)$$

Where: n is the independent variable of the digital domain of the sine signal, and its changing frequency is f_0.

The frequency of the output signal can also be modified according to the follow formula.

$$f_{out} = M / 2^N \cdot f_c \quad (5)$$

Where: f_{out} is the destination output waveform frequency; M is the frequency control word; N is the phase accumulator bit number; f_c is the system clock frequency.

DDS technology mainly includes three parts: frequency control register, phase accumulator and high speed calculator[5]. Under the action of the system clock f_c, the N-bit phase accumulator performs a linear accumulation of the frequency control word M. At this time, the output data of the phase accumulator is the phase of the synthesized signal, and the frequency of the phase accumulator is the output signal frequency of the DDS. At the same time, the output data of the phase accumulator is used as the phase sampling address value of the ROM waveform table, so the binary encoding of the waveform can be obtained to complete the phase-amplitude conversion[6]. The DA converter receives the output digital signal from the ROM waveform table and converts the digital signal into an analog signal to obtain a desired excitation signal. The DA then acquires the signal and transmits it to the power amplifier, which amplifies the signal to drive the piezoelectric sensor to work[7]. The working principle diagram of DDS is shown in figure 3.

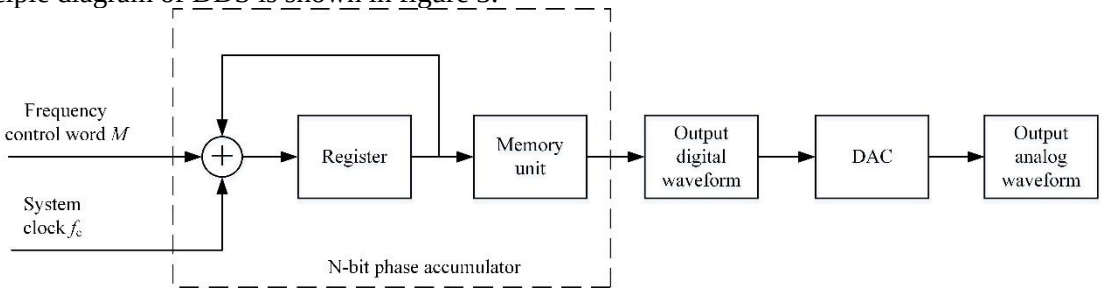


Figure 3. DDS working principle diagram.

The system clock used in this article is 50 MHz and the phase accumulator number N is 32. The output signal frequency of DDS is determined by Equation 5. Therefore, the frequency accuracy is 0.001 Hz, which meets the design requirements. In the program, the frequency within the range of 10 KHz to 80 KHz and the accuracy of 0.001 Hz can be generated.

3.3. Signal generator

The signal generator mainly includes a key input module, a DDS control module, an IP core storage module and a display module, and its RTL level view is shown in figure 4.

The key input module is input through three keys, the DDS control module recognizes the input signal from the key input module, and then calls the corresponding IP core storage module through the address signal. The waveform data initialized in the end is finally transmitted to the digital tube of the display module and the VGA interface through the address signal and the output waveform signal for display, thereby implementing the lookup table function of the DDS control module, that is, the design of the FPGA-based signal generator is realized. The subsequent signal source needs to be collected and transmitted to the power amplification module through the DA module, and the amplified voltage signal is used to drive the descaling module. At this time, the wedge-shaped piezoelectric sensor is

excited to work, and the descaling work is completed. At the same time, the oscilloscope can display waveform information.

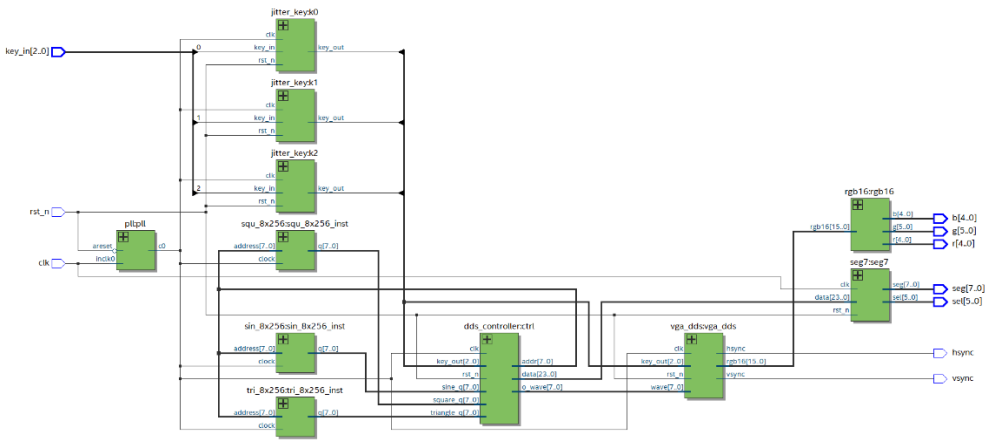
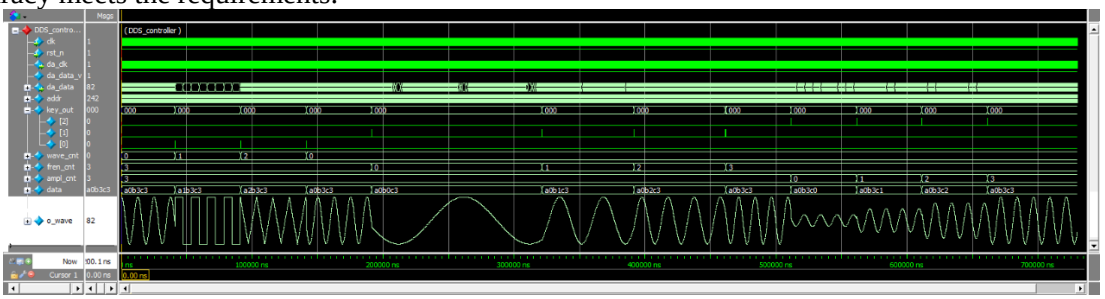


Figure 4. RTL-level view of the signal source generator.

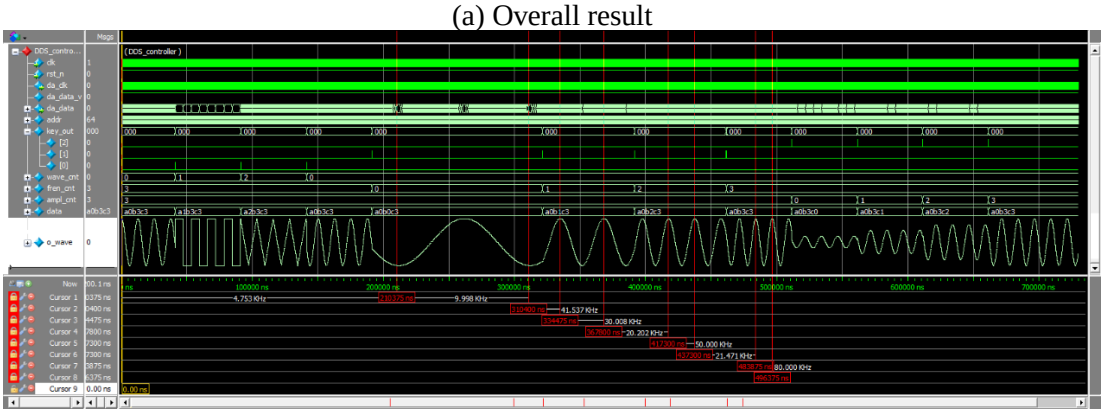
4. Performance Testing

4.1. Software testing

Each sub-module is instantiated into the top-level file by Verilog HDL code through QUARTUS software. Then the test file is written through the ModelSim simulation software for functional simulation verification. As shown in figure 5, the defined waveform, frequency and amplitude counters correspond to the input keys, and the final output waveform achieves the expected function. Figure 5(a) is divided into three parts: waveform adjustment, frequency adjustment and amplitude adjustment. The sine wave frequency accuracy is analyzed in figure 5(b). It can be seen that the simulation results are 9.998 KHz, 30.008 KHz, 50.000 KHz and 80.000 KHz, respectively, and the accuracy meets the requirements.



(a) Overall result



(b) The Frequency switching result of sine wave

Figure 5. ModelSim software simulation results.

4.2. Hardware testing

Although the software simulation results achieve the expected purpose, hardware testing is also required. Firstly, the pin is allocated for full compilation, and the data stream file is generated. Secondly, the JATG port is used to download the file for hardware testing. Finally, the DA module needs to collect data to the oscilloscope to observe the waveform in real time, or through the digital tube and display of the development board. Taking a sine wave as an example, after the power is initialized, the actual situation is shown in figure 6.

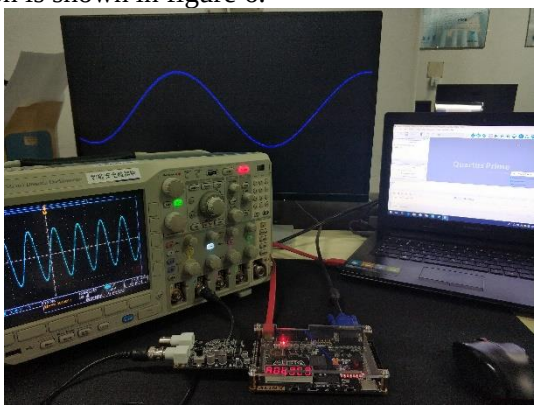
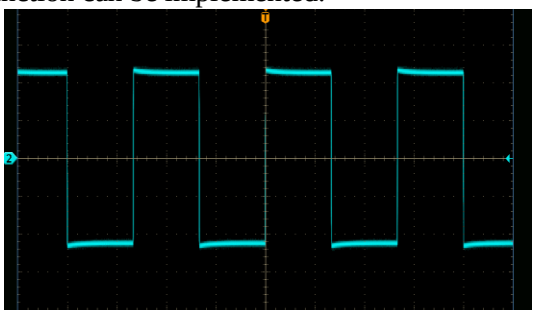


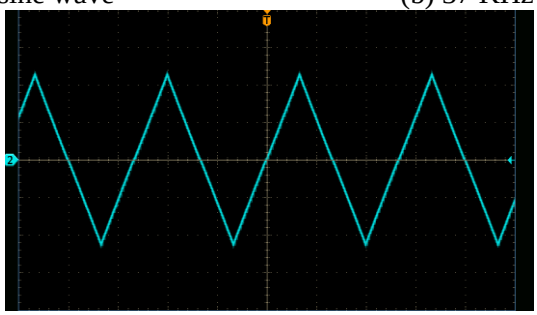
Figure 6. The hardware test results.

Taking the test waveform switching function as an example, press the Key 1 one by one, and the waveform diagrams are respectively shown in figure 7. It can output a sine wave, a square wave and a triangle wave. In the case, the waveform switching function can be implemented.

(a) 37 KHz sine wave



(b) 37 KHz square wave



(c) 37 KHz triangle wave

Figure 7. Waveform switching results.

In order to accurately analyze the system performance, the sine wave is taken as an example to quantitatively test the waveform output frequency. The data of multiple sets of specific frequency tests are shown in Table 1.

From the software simulation results and the actual results of the hardware test, the FPGA-based signal source generator realized by Verilog HDL code can generate waveforms of any frequency in the range of 10 KHz to 80 KHz, and there is no waveform distortion, which can be used as the signal generator of descaling experiments.

Table 1. The test output frequency DDS signal generator.

Standard frequency	Actual output frequency (KHz)			Average value (KHz)
	Test result 1	Test result 2	Test result 3	
10KHz	10.0001	9.9999	9.9998	9.9999
30KHz	30.0002	29.9999	30.0001	30.0000
50KHz	50.0001	50.0000	49.9998	50.0000
80KHz	79.9998	79.9999	80.0001	79.9999

5. Conclusion

The innovation of this paper is to combine FPGA development platform, DDS core algorithm and DAC data acquisition to achieve a high-precision signal generator, which greatly improves the stability of the descaling system and also has guiding significance for building highly integrated ultrasonic guided wave descaling system.

Acknowledgments

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