Design of a High Resolution TDC Based on Multi-channel

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Design of a High Resolution TDC Based on Multi-channel

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Abstract. In this paper ,a high precision time digital converter (TDC) system is designed based on Xilinx 7 series FPGA chip, which includes fine time measurement module, logic control module, rough count module and display module. The key point of FPGA TDC design is that there are a large number of delay units in the underlying hardware resources with stable delay. A delay chain consisting of 64 fast carry chains (CARRY4) is constructed by using the CARRY4 module inherent in the chip. In addition, the code density method is used to solve the nonlinear problem of internal special carry chain delay unit, effectively eliminate the error caused by wiring path, and reduce the integral nonlinear and differential nonlinear error. The experimental results show that the code density method can accurately reflect the distribution of delay time.

1. Introduction

Precision time measurement is widely used in communication, laser ranging, scientific metrology, medical imaging and other fields[1]-[3]. Time to digital converter (TDC) is a basic means of Time interval measurement. It converts the analog signal of Time interval turned into digital signal to realize the measurement of Time interval [4].

The traditional time interval measurement technology is based on the system reference clock counter technology, the minimum measurement resolution is determined by the clock cycle. If the resolution of time interval measurement is increased to 50ps, the corresponding clock frequency should reach 20GHz, which brings great challenges to the circuit design. In addition, in high-resolution interval measurement, the non-linearity of TDC is a key factor affecting the further stability of accuracy, which must be considered in the design and use of measurement equipment.

Currently, the implementation of TDC system is mainly divided into two ways: fully customized ASIC-TDC design based on CMOS and FPGA-TDC design based on field programmable gate array. Compared with ASIC-TDC, FPGA-TDC has the advantages of short design cycle, low development cost and flexibility to adapt to different measurement fields. Therefore, the tapped delay line structure is selected in this paper,and the mainstream Xilinx tool(Vivado) is used to realize the TDC system in the 7-series FPGA chip.

Carry chain design has great advantages, there are also some key technical problems to be solved. Firstly, it is difficult to implement a fixed and continuous carry chain in the FPGA due to the optimization problem of the compilation tool itself [5]. Most importantly, the time of the minimum delay unit in the FPGA is uncontrollable and varies with the change of temperature, power supply voltage and other factors[6], so the possible deviation of the TDC system needs to be calibrated.

2. Measurement Principle

In order to ensure the design requirements of the range and resolution, this paper divides the measurement into two parts: rough measurement and fine measurement. Rough measurement can meet the design requirements of the range, and fine measurement is used to improve the resolution requirements. Coarse measurement usually uses pulse counting method, which is the simplest time measurement method. Fine measurement is realized by a carry adder, which measures the distance between the open and close signal edge and the reference clock edge.

The research scheme designed in this paper adopts the time interpolation technology based on FPGA, and USES the MUXCY inside CARRY4 module in the 7-series chip as the most basic delay unit, as shown in figure 1. Each CARRY4 cell has four MUXCY units within it, and up to four tapped delay units can be configured. The signal is input from the CI end of CARRY4 and output from the CO(3) end, and the output is connected to the CI input end of the next CARRY4 unit. In this way, a long enough delay chain is solidified in the FPGA, and the dedicated carry chain is cascaded in the chip to form the delay chain. Four taps are extracted from the CO[3:0] of CARRY4 and input to the D input end of the adjacent D trigger for data locking.

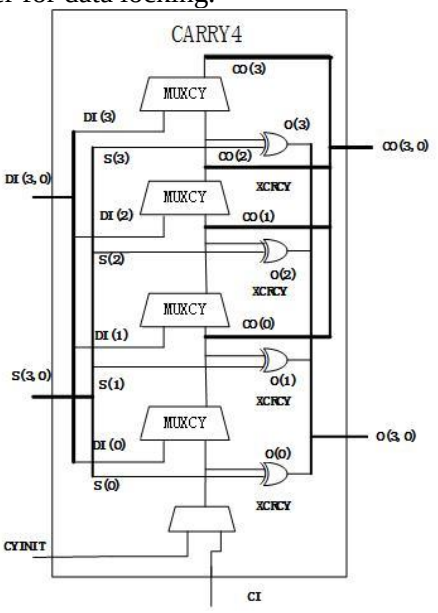

Fig.1 CARRY4 structure

The start signal and stop signal are sent into the delay chain successively. When the rising edge of the open and close signal arrives, the signal can be propagated in the carry chain and the position of the carry signal can be captured by the D trigger. If the output of a level D trigger changes from 1 to 0, it means that the carry signal has been propagated to the level. If the delay of each carry chain is known, the time interval between the rising edge of the signal to be tested and the rising edge of the next clock can be obtained. By this method, the time difference between two signals and the rising edge of the clock can be calculated. The TDC timing diagram is shown in figure 2.

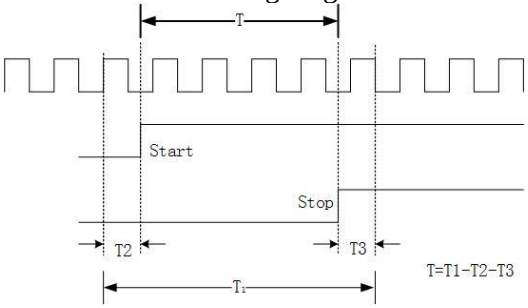

Fig.2 Timing diagram of measurement

3. Structure Design And Implementation

For physical research experiments, the time measurement system has two core indicators: one is the minimum time interval that can be distinguished, which requires the measurement accuracy to be as small as possible. The current measurement accuracy can basically reach the picosecond level. The other is the maximum time interval that can be measured, with a large measurement range. Specifically, the measurement range must meet the standard according to the actual requirements. The range enlargement is mainly realized by expanding the number of Gray code rough count.

In this paper, the range of the fine count time measurement module should reach 5ns (the highest clock frequency we have reached 200MHz), and the time resolution of the whole system should be less than 100ps. Leave 10ps margin for logic control circuit and signal transmission; The jitter space of 10ps is left for the measured signal. The precision of TDC fine time measurement module is expected to be less than 100ps. According to the data analysis and combining with the existing practice, Xilinx tool is adopted to realize the TDC system in the 7-series FPGA chip, so as to meet the requirements of the measurement accuracy.

The TDC system designed in this paper is shown in figure 3, which is mainly composed of delay chain, two-stage D trigger latching array, calibration module and coding module. When the chip reference clock is 200MHz, 255 delay units can be configured to meet the actual needs. The TDC system designed in this paper adopts two-stage D flip-flop latching technology. The latching control signal of the first-stage D flip-flop is a reference clock, which is triggered by the rising edge. The latch control signal of level 2 D trigger is the data output of the upper trigger triggered by the rising edge. This latching technique can not only reduce the metastability of D flip-flop, but also make the holding time of the latched thermometer code be flexibly controlled, which is not limited by the reference clock frequency and reduces the processing speed requirement of the coding circuit.

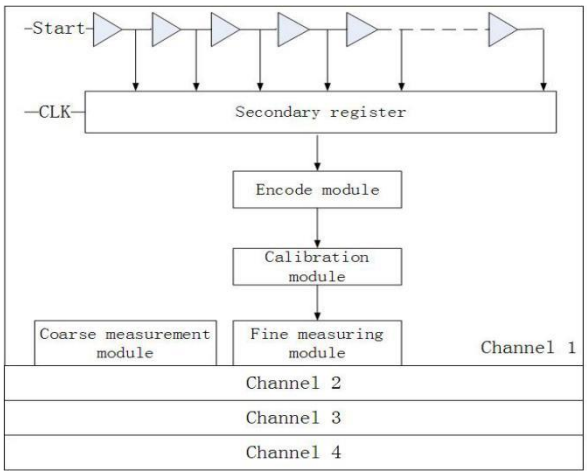

Fig.3 TDC system structure diagram

At the same time, in order to further improve the measurement accuracy of the system, four delay chains are equipped with Start and Stop signals to be measured simultaneously in this paper, and the final measurement results are obtained by averaging.

4. Design Of Calibration Circuit Based On Code Density

Although the compiled software can preliminarily simulate the delay of the carry chain, this is only an ideal value. The actual research shows that the delay of carry chain is not stable, and the delay of carry chain at different levels is not the same. Even if the same carry chain is at different voltages and temperatures, its actual delay will change[7]-[8].

Therefore, the primary problem to realize TDC with this method is to solve the problem of realizing and curing the carry chain inside the device, and to maintain the consistency of each operation of the system. In addition, all kinds of clock frequency drift and internal wiring of the

hardware will bring some systematic errors to the final measurement results, which must be corrected in the system to improve the measurement accuracy of TDC.

Code density is a bit-by-bit calibration method that measures the delay time of each delay unit. Whose basic principle is: the first use of a large number of uniform distribution on [0, T) in random pulse as input signals to be measured in the TDC system. if the input signal is random, then the input signal is hit in one clock cycle at any point in time the probability are equal. And then calculates the delay unit number, and the random events under the premise of enough, delay time will have a direct relationship with the number of events, which can calculate the size of each delay unit delays, computation formula is as follows:

$$T_m = \frac{M}{N} \times T \qquad (1)$$

The code density data sampled by the Tm delay unit is m, N is the number of random signals, and Tm is the delay time of the delay unit.

Through the above analysis, the calibration circuit structure diagram designed in this paper is shown in figure 4. The calibration circuit module is mainly composed of random signal generation circuit, random signal holding circuit and calibration look-up table storage circuit. The random signal generation circuit uses a ring oscillator to generate random calibration signals. Calibration lookup table storage circuit is to establish an accumulative lookup table for TDC calibration results.

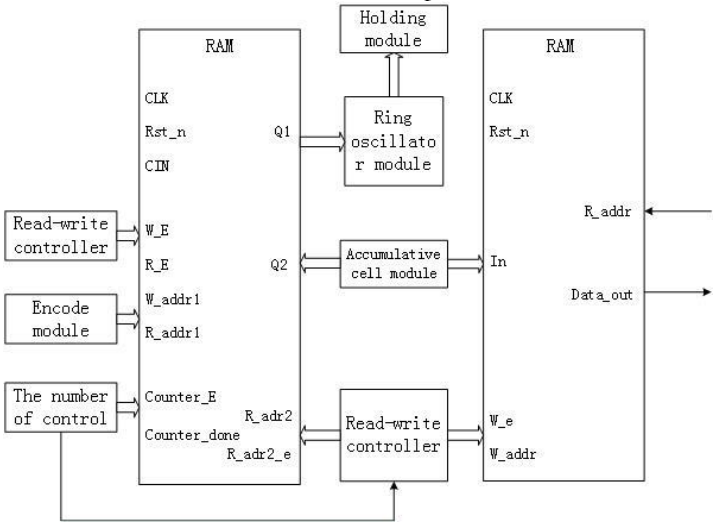

Fig.4 Calibrate circuit diagram

5. Results analysis

Resolution, also known as code width, is the smallest measure of time interval that a system can recognize. It is usually represented by the Least Significant Bit (LSB). The smaller the Least Significant Bit (LSB), the higher the measurement resolution.

The delay time of each delay unit is not uniform, which results in the nonlinearity of the system. Nonlinearity (NL) is usually measured by two parameters: differential nonlinearity (DNL) and integral nonlinearity ((INL).

Differential non-linearity (DNL) refers to the deviation value between the actual output code width and the theoretical LSB, which can be expressed as:

$$DNL = \frac{LSB' - LSB}{LSB} \qquad (2)$$

LSB' is the actual delay time of each delay unit

LSB is the average delay time of each delay unit

Differential nonlinearity is actually a reflection of the inhomogeneity between the time code widths, and severe differential nonlinearity will lead to the loss of the code, that is, some output codes will never appear.

Integral non-linearity ((INL) is equivalent to the accumulation operation of differential non-linearity (DNL), which can be expressed as:

$$INL = \frac{\sum_{i=0}^{n} LSB' - nLSB}{LSB} \quad (3)$$

LSB' is the actual delay time of each delay unit

LSB is the average delay time of each delay unit

According to the result statistics, the simulation results of differential non-linearity and integral non-linearity are shown in figure 5 and figure 6. It can be seen that the delay chain differential non-linearity (DNL) is (-1,2) LSB and the integral non-linearity (INL) is (0.5,5.8) LSB, indicating that this method has good stability and linearity.

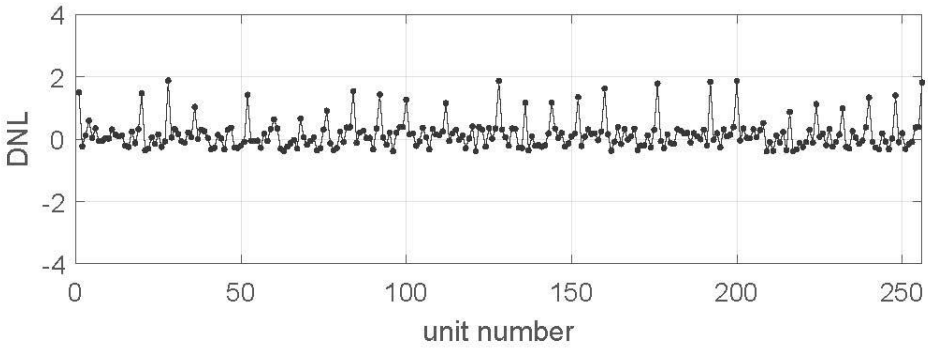

Fig.5 Differential nonlinearity

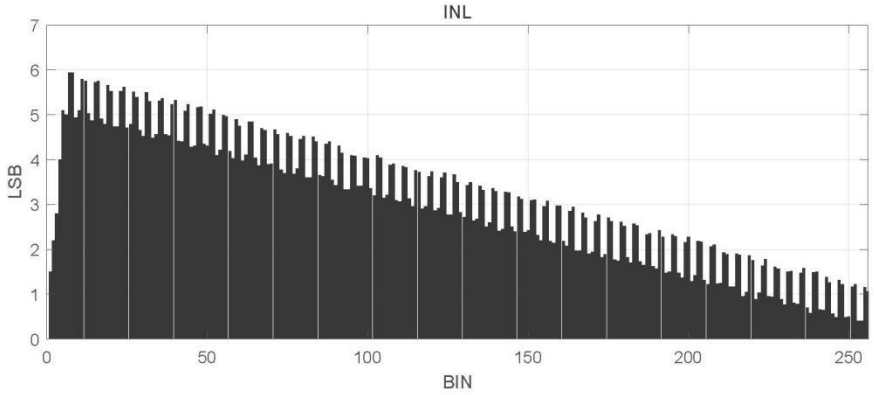

Fig.6 Integral nonlinearity

6. Conclusion

In this paper, Xilinx 7 series FPGA chip, which has been widely used in recent years, is used to design a high-precision time digital converter system with the help of mainstream software. The specific delay time of each delay unit was measured by code density method, and the inconsistency was analyzed. In the data locking process of tapped delay line, a two-stage D flip-flop is adopted to reduce the metastability and keep the system stable. This method can be applied to the mainstream FPGA chip of Xilinx company at present, which fills the technical gap of using carry chain to realize TDC on the mainstream FPGA device of Xilinx company, and is conducive to the promotion and application of this method in various electronic fields.

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