Design of ZVS DC/DC converter based on DSP2812 phase-shifted full bridge

IOP Conf. Series: Materials Science and Engineering **563** (2019) 042079 doi:10.1088/1757-899X/563/4/042079

Design of ZVS DC/DC converter based on DSP2812 phase-shifted full bridge

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Abstract. The phase-shifted full-bridge DC/DC converter is a very important component of power electronics and is suitable for medium and large power output applications based on switching power supplies. Aiming at the implementation of soft-switching and the problem of power loss, this paper firstly describes the structure and working mode of DC/DC converter, then analyzes the calculation and selection process of resonant inductance and capacitance parameters in the converter, and finally adopts the traditional PI control to achieve stable control of the output voltage. The simulation and experimental results fully prove the feasibility and rationality of the design and parameter selection of this scheme.

1. Introduction

In recent years, with the rapid rise of the automobile industry, the automobile has brought great convenience to people, but caused environmental pollution and energy shortage. In this context, new energy is vigorously popularized, and the demand for power supply equipment in various industries is growing day by day. The higher demands are placed on its performance, volume, stability and work efficiency. Due to its small size, high reliability, and high work efficiency, switching power supplies have gradually replaced linear power supplies and become the mainstream [1] [2].

The performance of the switching power supply has been further optimized with the increasing frequency. However, the switching tube in the switching power supply operates in the switching state, and there must be a certain loss. Soft-switching technology has been introduced to reduce power loss. The phase-shifted full bridge (PSFB) is a relatively successful soft-switching by using a resonant circuit to reduce switching losses. And it is widely used in train power supply systems [3], new energy vehicle charging piles [4], micro-grid energy storage units [5] and other fields.

In the implementation of the entire converter system, the parameter selection of resonant inductance and capacitance is critical to the operation of the converter. Therefore, based on the analysis of PSFB DC/DC circuits, the parameters of resonant inductance and capacitance are selected according to the principle of energy exchange conservation. The output voltage adjustment is realized by PI control from the Miller effect. Finally, theoretical simulation and experimental verification are carried out [6].

2. PSFB circuit topology and its working principle

The main circuit topology of the PSFB ZVS DC/DC circuit is shown in figure 1 [7].

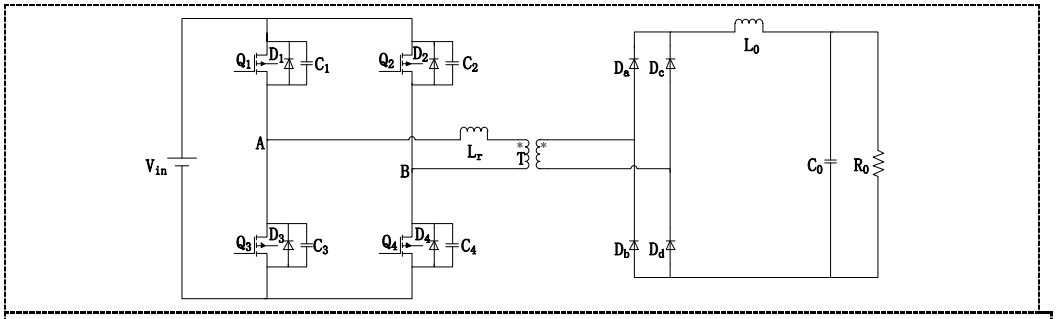


Figure 1. Structure diagram of PSFB ZVS DC/DC converter

As shown in figure 1, in the PSFB ZVS DC/DC circuit, the leading leg (the 'Active to Passive' leg) composed of the complementary-on switching transistors Q1 and Q3 and the lagging leg (the 'Passive to Active' leg) composed of Q2 and Q4 are in the same switching cycle, which can form 12 modes as shown in figure 2.

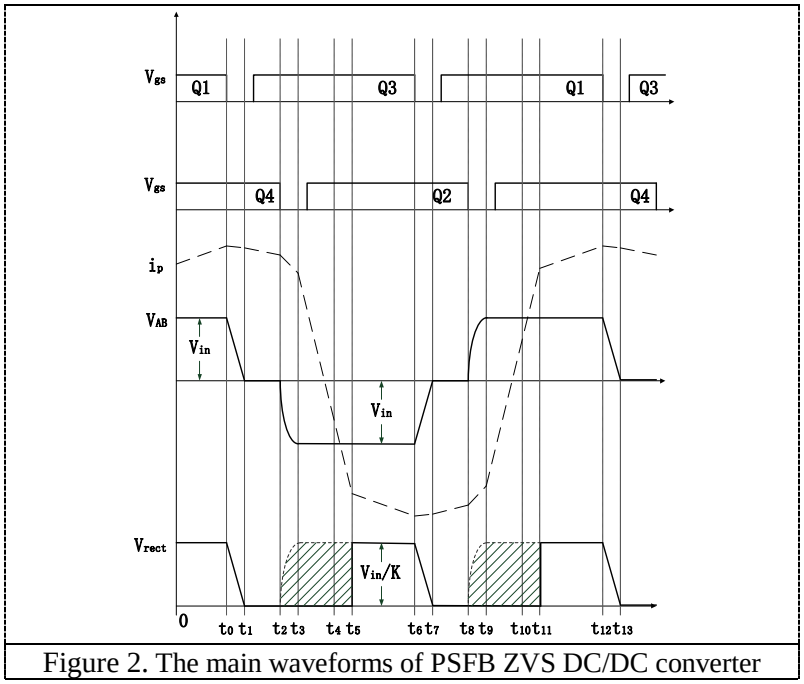


Figure 2. The main waveforms of PSFB ZVS DC/DC converter

From 0 to time t_0, the primary current can fully supply power to the load. During the period from t_0 to t_2, the leading leg's soft-switching is switched. During the process, the primary side resonant inductor is coupled with the secondary side rectifying filter inductor, which can ensure that there is enough energy to release the charge in the resonant capacitor. In the period from t_2 to t_5, it is the process of soft-switching switching with the lagging leg. At this time, the primary side current is only provided by the resonant inductor, and the primary current i_p is rapidly decreasing in the forward direction and rapidly increasing in the reverse direction. The role of resonance in the process is even more critical. Therefore, the calculation of the resonant inductor and capacitor is particularly important [8].

3. Converter parameter design

3.1. Parameter design of PSFB ZVS DC/DC circuit

The main electrical specifications of DC/DC circuit design is that the input voltage is 500VDC, the switching frequency is 80kHz, the load power is 1kw, and the output voltage is 250VDC.

3.1.1. Calculation of transformer parameters. The transformer is the core component of the PSFB DC/DC converter, which acts as a step-down and isolation. Since the switching frequency is set at 80kHz, the transformer core is selected as the ferrite core suitable for high-frequency conditions.

Here, the input voltage V_{in} is required to be 500V, the output voltage V_{out} is 250V, and the secondary maximum duty ratio D_{max} is 0.85. The transformer ratio is：

$$\alpha_1 = \frac{N_p}{N_s} = \frac{(Vin_{min} - 2\times V_{RDSON})\times D_{max}}{V_{out} - 2\times V_F} \quad (1)$$

In the formula (1), the voltage drop of the primary side switch tube $V_{RDSON} = 0.3V$, and the voltage drop of the secondary side diode $V_F = 0.7V$, which can be obtained as $\alpha_1 = N_P/N_S = 12/7$.

3.1.2. Calculation of resonant inductance and capacitance parameters. For a full bridge DC/DC converter, the maximum duty cycle loss on the secondary side of the transformer is 15%:

$$D_{loss} = \frac{2L_r(I_1 - I_2)}{V_{in}T} \leq 15\% \quad (2)$$

In the formula (2), I_1-I_2 is the change of the primary side current when the secondary side diode is freewheeling and is calculated according to $2I_1$. T is the switching period and is calculated as $L_r \leq 35.4uh$, where the resonance inductance L_r takes 33uh.

The value of the resonant capacitance is derived from the following formula (3):

$$C_{lead} = C_{lag} = \frac{4}{3} * C_{oss} * \sqrt{25/Vin} \quad (3)$$

After calculation, $C_{lead} = C_{lag} = 2nf$.

3.1.3. Derivation of the filter inductance and capacitance parameters of the secondary side of the transformer. The filter circuit of the PSFB DC/DC circuit is the same as BUCK circuit. It is necessary to maintain the continuity of the output filter inductor current at 10% of the output current at full load. Therefore, using the formula $I_{outmin} = 0.1 \times \frac{5000}{350} = 1.43A$.

The formula for calculating the filter inductance is:

$$L_0 = \frac{V_{out}}{0.2\times 2f_s \times I_{outmin}}\left(1 - \frac{V_{out}}{\alpha_1 V_{in} - V_{LF} - 2V_F}\right) \quad (4)$$

In the formula (4), f_s is the switching frequency of 80kHz; V_{LF} is the voltage drop across the filter inductor, which takes a value of 1V; V_F is the voltage drop of the rectifier diode of 0.7V. L_0=121uh is calculated.

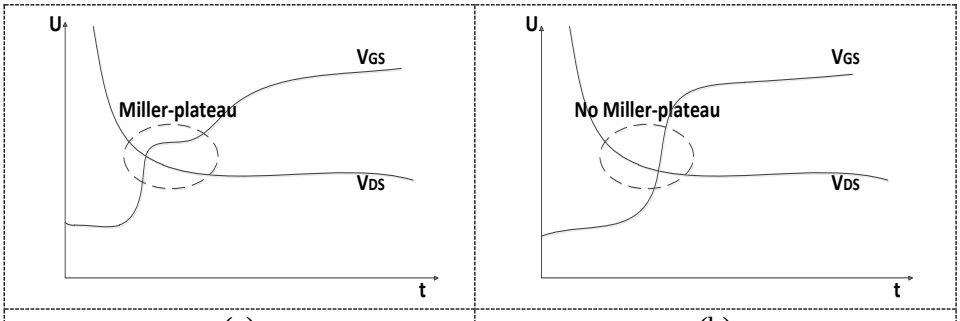
The formula for calculating the filter capacitance is:

$$C_0 = \frac{V_{out}}{8L_0(2f_s)^2\Delta V}\left(1 - \frac{V_{out}}{\alpha_1 V_{in} - V_{LF} - 2V_F}\right) \quad (5)$$

It can be calculated that C_0=850uF.

3.2. Soft-switching experimental verification

When switching the switch tube, its GS and DS waveforms are shown in figure 3:



(a) (b)

Figure 3. The implementation process of ZVS

As shown in figure 3(a), "Miller-plateau" appears when the switch tube is about to be turned off, and the energy stored in the resonant inductor L_r is not enough to be supplied to the circuit to complete the ZVS of the circuit. As shown in figure 3(b), when the "Miller-plateau" disappears on the V_{GS}

voltage, the converter realizes ZVS. In the actual debugging, it is more feasible to verify the correctness and rationality of the circuit parameter value through the "Miller-plateau".

4. Open-loop and closed-loop experiments

The circuit parameters are selected as follows: the switching frequency is 80kHz, the dead time is 1.6us, the transformer turns ratio is 12/7, the secondary side filter inductor is 121uh, the filter capacitor is 850uf, the shunt capacitance is 2nf, and the resonant inductor value is 33uh. The experimental results are as follows:

The GS and DS waveforms of the same mosfet on the lagging leg are shown in figure 4.

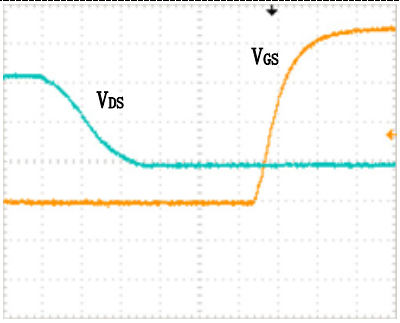


Figure 4. GS and DS diagram of the lagging leg switch tube when the two ends of the switch tube are connected in parallel with 2nf capacitors

In figure 4, the yellow waveform is the GS signal and the blue waveform is the DS signal. At this time, the "Miller-plateau" does not appear on the GS waveform of the switch tube, and the ZVS can be realized by the lagging leg switch tube. Next, measure the primary voltage of the transformer, and the waveform is shown in figure 5.

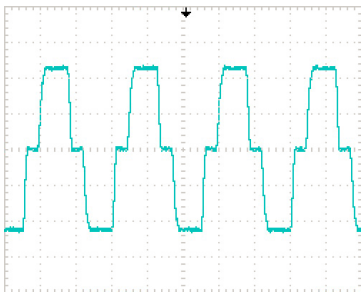


Figure 5. The voltage waveform of the primary side of the transformer when the 2nf capacitor is connected in parallel at both ends of the switch tube

In figure 5, the voltage waveform on the primary side of the transformer does not appear spiked, which is basically consistent with the theoretical waveform, and the circuit can operate stably at this time. Next, the circuit output efficiency is measured under the condition of the load is 70 Ω and the input voltage is 500V. The power test results are shown in table 1.

Table 1. Input and output power at different phase-shifted angles

Phase-shifted Angle(°)	Input voltage(V)	Input current(A)	Input power(W)	Output voltage(V)	Output current(A)	Output power(W)
40	500	2.51	1255	294.8	4.21	1241.5
60	500	2.07	1035	259.8	3.71	964.2
80	500	1.58	790	218.6	3.12	682.7

100	500	1.04	520	176.2	2.52	443.5

By calculating the data in the above table, under the existing parameters, the circuit conversion efficiency can be kept at 85% or more. It can be verified that the open-loop parameters of the system are feasible.

After the system open-loop circuit is built, the PSFB DC/DC circuit is closed-loop controlled. The control block diagram of the closed-loop system is as figure 6.

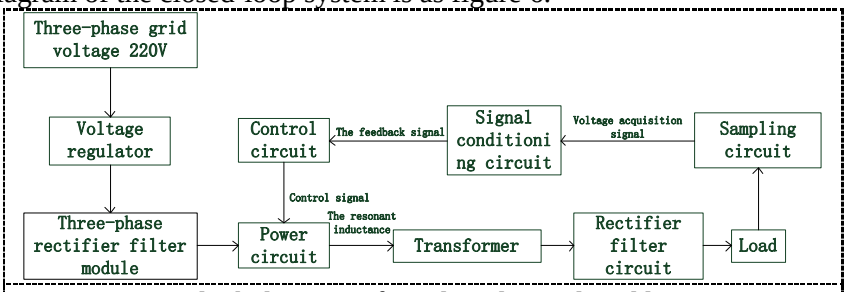


Figure 6. Block diagram of single voltage closed loop circuit

In this paper, the closed-loop control is used for voltage single-closed loop control. As shown in figure 6, the voltage across the load is transmitted to the control circuit through the sampling circuit and the signal conditioning circuit. The PI algorithm is carried out on the feedback signal on the control board and the adjustment value obtained from the calculation is added to the control signal. Closed-loop control of the voltage across the load is achieved. In the process of input slow boost, we use an oscilloscope to observe the voltage across the load as shown in figure 7.

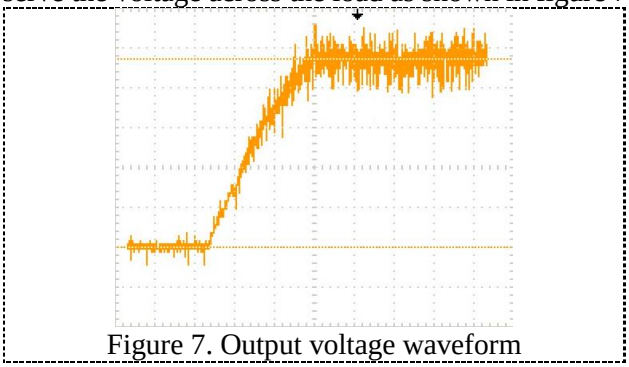


Figure 7. Output voltage waveform

Figure 7 shows the waveform measured by the oscilloscope connected to the sampling module. As can be seen from Figure 7, in the process of slowly boosting to 500V, the voltage across the load can be basically controlled to 250V, and the input current is 2.04A. The input power is 1025W. The current flowing through the load is 3.56A and the output power is 887.9w. It can be calculated that the circuit conversion efficiency is 86.6%.

5. Conclusion

For the zero-voltage turn-on and turn-off of PSFB ZVS DC/DC circuits, this paper chooses to analyze the circuit working principle, component parameter selection, circuit simulation, circuit implementation, and test. The experimental results show that this design in the circuit, the ZVS can be fully realized while reducing the power loss, which fully validates the solution described in the paper. The subsequent closed-loop design of the circuit can now basically control the output voltage to about 250V when the load is 70Ω.

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