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To cite this article: A Islam and K Kalna 2019 *IOP Conf. Ser.: Mater. Sci. Eng.* **504** 012021

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# Analysis of electron transport in the nano-scaled Si, SOI and III-V MOSFETs: Si/SiO<sub>2</sub> interface charges and quantum mechanical effects

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**Abstract.** The ITRS predicts that the scaling of planar CMOS (Complementary Metal Oxide Semiconductor) technology will continue till the 22 nm technology node [1] and a possible extension beyond is appealing [2]. In this work, we investigate the effect of electron confinement [3] in nanoscaled transistor channels of 25 nm surface channel Si and 32 nm SOI (Silicon on Insulator) and 15 nm IF (Implant Free) III-V MOSFETs using a self-consistent solution of 1D Poisson - Schrödinger equation [4,5]. For simulation and development with accuracy of nano-scaled of 25 nm gate length Si MOSFET (Metal Oxide Semiconductor Field Effect Transistor), 32 nm SOI Implant Free (IF) MOSFET, and 15nm Implant Free III-V MOSFET transistors, we investigated the bandstructure and quantum confinement effects occurring near the oxide-semiconductor interface in Metal-Oxide-Semiconductor (MOS) structure of Si MOSFET device. These investigation have been carried out using a self-consistent solution of 1D Poisson-Schrödinger equation across the channel of conventional Si / SOI / III-V MOSFET Transistors. To solve self-consistently 1D Poisson-Schrödinger equations across the channel of a conventional Si, SOI, and an Implant Free III-V MOSFETs to determine the conduction and valence band profiles, electron density, electron sheet density, eigenstate and eigenfunctions in these structures. We present the simulation results of conduction band profile, electron density (classical and quantum mechanical), eigenstate and eigenfunctions for Si, SOI and III-V MOSFET structures at two different bias voltages of 0.5 V and 1.0 V. For comparison, we calculate the electron sheet density (quantum mechanically) as a function of the applied gate voltages.

## 1. Introduction

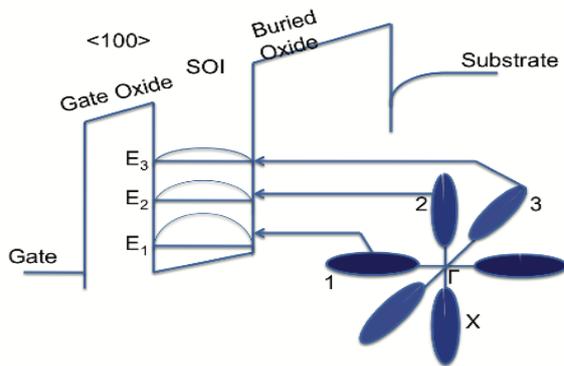
In this section, a connection between the bandstructure and quantum confinement effects with device characteristics in nano-scale devices is established. Three different devices are presented: a 25 nm gate length Si MOSFET, a 32 nm SOI MOSFET and a 15 nm In<sub>0.3</sub>Ga<sub>0.7</sub>As channel MOSFET. We use a 1D Poisson-Schrödinger solver across the middle of the gate along the channel of the devices. The goal is to obtain the calculations of an energy of bound states and associated carrier wavefunctions which are carried out self consistently with electrostatic potential. The obtained wavefunctions are



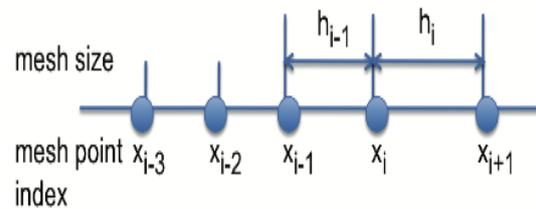
then used to calculate a carrier density which allows to obtain a sheet density across the structure at given bias.

We have chosen the SOI MOSFET for comparison because it is considered for low power applications. The SOI technology is developing now into the commercial area and is included in the ITRS. The SOI based MOSFETs have a silicon channel made of a narrow layer of less than 10 nm grown on a relatively thick SiO<sub>2</sub> layer. The FD (fully depleted) SOI MOSFET has superior electrical characteristics and a threshold control from a bottom gate compared to the bulk CMOS device, which are described as (a) decrease in a power dissipation and faster speed due to reduced junction area, (b) steep sub-threshold slope, (c) negligible floating body effects, (d) increased channel mobility, (e) reduced short-channel effects and an excellent latch-up immunity [4].

We will consider a semiconductor material with a small energy gap sandwiched between energy barriers from a material with a larger energy gap. In this way, a quantum well is formed between the barriers which introduces a potential well with discrete energy levels, where particles are confined in one dimension and move free in other two directions as shown in Figure 1 [3].



**Figure 1.** Schematic of conduction band structure of Silicon <100> oriented narrow channel. The energy levels are also shown in the quantum well.



**Figure 2.** One dimensional discretization scheme using a nonuniform mesh

In classical systems, if a particle is trapped inside a box, then the particle can move at any speed within the box. However, when the well becomes very narrow (nanometres), the system cannot be described classically anymore because the size of the particle becomes comparable to the size of the entrapment box and the classical description has to be replaced by more accurate, quantum-mechanical description. The effect of quantum confinement takes place when the quantum well thickness becomes comparable to de Broglie wavelength [4] of the particles. In quantum mechanics, a wavefunction gives the most fundamental description of the behaviour of a particle; the measurable properties of the particle (such as its position, momentum and energy) may all be derived from wavefunctions [3].

In the calculations, we will determine the conduction band profile, electron density, energy levels (eigenstates), wavefunctions (eigenfunctions) and electron sheet density in the semiconductor device structure under external potential. In this case, both Schrödinger and Poisson equations have to be solved self-consistently. The one-dimensional, time independent Schrödinger's wave equation for a particle in a potential distribution is a second order ordinary differential equation, which is given by [5].

$$-\frac{\hbar^2}{2} \frac{d}{dx} \left( \frac{1}{m(x)} \frac{d}{dx} \right) \psi(x) + V(x)\psi(x) = E\psi(x) \quad (1)$$

After rearranging the above equation, we get

$$\left( -\frac{\hbar^2}{2m(x)} \frac{d^2}{dx^2} + V(x) \right) \psi(x) = E\psi(x), \quad (2)$$

$$\mathbf{H}\psi(x) = E\psi(x),$$

where  $\psi$  is the wave function,  $E$  is the energy eigenvalue,  $V(x)$  is the potential energy assumed to be independent of time,  $\hbar$  is Planck's constant,  $m = m(x)$  is the effective mass of an electron which is a position dependent,  $\mathbf{H}$  represents the Hamiltonian operator associated with the sum of the kinetic and potential energies of the system.

The potential distribution  $\phi(x)$  in the semiconductor can be determined from a solution of the 1 D Poisson equation, which is given by

$$\frac{d}{dx} \left( \epsilon_S(x) \frac{d}{dx} \right) \phi(x) = \frac{-\rho(x)}{\epsilon_0} \quad (3)$$

$$\rho = N_D(x) - N_A(x) + p(x) - n(x) \quad (4)$$

$$\frac{d}{dx} \left( \epsilon_S(x) \frac{d}{dx} \right) \phi(x) = \frac{-q[N_D(x) - N_A(x) + p(x) - n(x)]}{\epsilon_0}, \quad (5)$$

where  $\phi$  is the electrostatic potential,  $\epsilon_S$  is the semiconductor dielectric constant,  $\epsilon_0$  is the permittivity of free space. In the static behaviour,  $N_D$  and  $N_A$  are called the ionized donor and acceptor concentrations and, in the case of dynamic behaviour,  $n$  and  $p$  are known as electron and hole density distributions. When dealing with n -type majority carriers semiconductor devices, we can ignore the holes contribution due to their slow movement compared to the electron dynamics. We will solve the 1D Schrödinger equation on a non-uniform mesh which means that the distance between adjacent mesh points will vary in dependence on their position. To solve Schrödinger equation numerically, we may discretize the differential Equation (2) by using a three-point finite difference scheme as shown in Figure 2

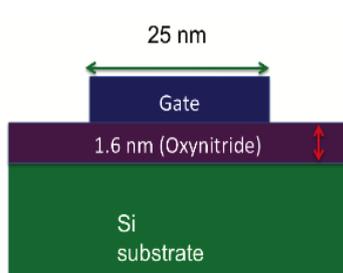
$$-\frac{\hbar^2}{2} \left( \frac{2(\psi_{i+1} - \psi_i)}{m_{i+\frac{1}{2}} h_i (h_i + h_{i-1})} - \frac{2(\psi_i - \psi_{i-1})}{m_{i-\frac{1}{2}} h_{i-1} (h_i + h_{i-1})} \right) = \lambda \psi_i \quad (6)$$

We established 1D Poisson-Schrödinger solver across the middle of the gate along the channel of the MOS structure of the 25 nm gate length Si MOSFET device. In this case, both Schrödinger and Poisson equations have to be solved self-consistently [6].

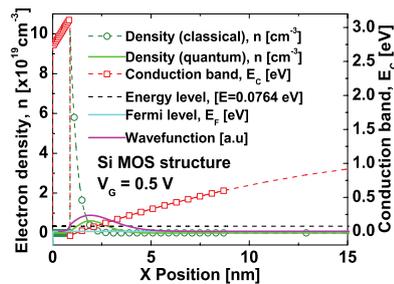
## 2. Solving 1D Poisson -Schrödinger Equations

### 2.1. MOS structure for 25 nm gate length bulk Si MOSFET

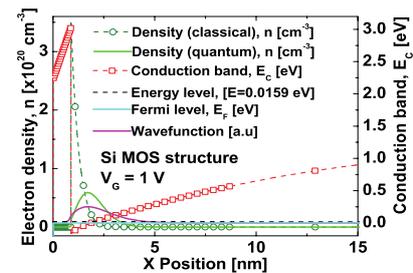
We will investigate a Si MOS structure at a cross-section in the middle of a gate of the 25 nm gate length Si MOSFET. The structure shown in Figure 3, has a p -type silicon substrate, oxynitride (ON) gate oxide with thickness of 1.6 nm, dielectric constant of  $\epsilon_{ON} = 7$  and a metal gate. Figure 4 shows the conduction band and electron density profile, which are classically and quantum mechanically calculated when biased at  $V_G = 0.5$  V at room temperature. The electron triangular-like confinement is moderate at the Si-ON interface at this applied gate voltage. We observed only one energy level and corresponding wavefunction in the triangular-like confinement. The classically calculated electron density exhibits very large peaks at the interface and leads to a large electron density at a given applied gate voltage of  $V_G = 0.5$  V. The quantum-mechanically calculated electron density is lower when compared to the density obtained from classical solution. But most importantly, a maximum density occurs away from the oxide-semiconductor interface due to bound states present in the quantum-mechanical description as compared to the classical calculation [7].



**Figure 3.** Schematic MOS structure for the 25 nm gate length Si MOSFET.



**Figure 4.** Conduction band, electron density, energy levels and wavefunction at  $V_G = 0.5$  V.



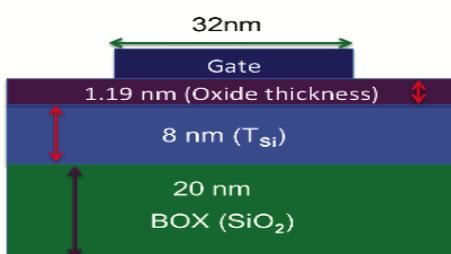
**Figure 5.** Conduction band, electron density, energy Levels and wavefunctions at  $V_G = 1.0$  V.

The conduction band profile in a MOS structure of bulk silicon, biased at  $V_G = 1.0$  V is shown in Figure 5. The surface quantization is often expressed by a triangular well approximation and the potential near the interface has almost a triangular shape because the potential barrier of  $\text{SiO}_2$  is relatively high in silicon MOS structure [8]. Figure 5 shows also the classically calculated electron density which will peak at the interface and predicts a much larger electron density when compared to the previous results obtained at  $V_G = 0.5$  V. The quantum-mechanically calculated electron density is smaller and a displacement of the charge from the interface occurs when compared to the classical calculation [9].

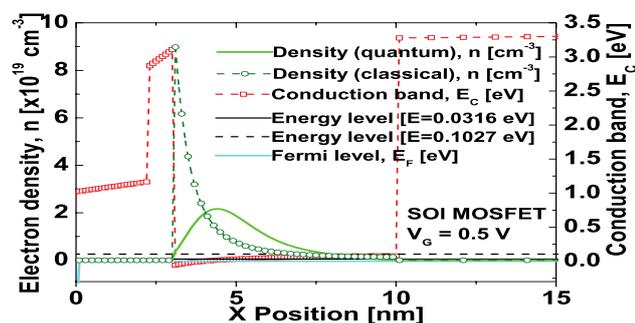
The energy level at the applied voltage of  $V_G = 0.5$  V in Figure 4 appears to be higher when comparing to the voltage of  $V_G = 1.0$  V [Figure 5]. In reality, this is opposite. The bottom of the conduction band at the interface for the voltage of  $V_G = 1.0$  V is much deeper than for the voltage of  $V_G = 0.5$  V. To get comparable positions of the energy levels, we fixed the bottom of the conduction band at the interface on the same scale in the conduction band level for both applied voltages ( $V_G = 0.5$  V,  $V_G = 1.0$  V). Then we observe that the position of the energy level at the voltage of  $V_G = 1.0$  V is higher than the energy level at the voltage of  $V_G = 0.5$  V, which we expected.

### 2.2. MOS structure for 32 nm gate length SOI MOSFET

The SOI structure has a layer of  $\text{SiO}_2$  with a thickness of 20 nm, and is fabricated on Si substrate and the silicon body with a thickness of 8 nm. Hafnium Oxide ( $\text{HfO}_2$ ) layer is deposited above the silicon body as a gate oxide with a thickness of 1.19 nm and a dielectric constant of  $\text{HfO}_2 = 20$  and a top metal contact referred to as a gate as shown in Figure 6. We have investigated the specified 32 nm gate length SOI MOSFET using 1D Schrödinger and Poisson equations. In this structure, the potential energy creates a square quantum well, because the potential difference between the front interface and the back interface is small and the potential barriers are very high. Electrons are therefore confined in the ultra-thin Si body, which is sandwiched between the gate oxide and the BOX.

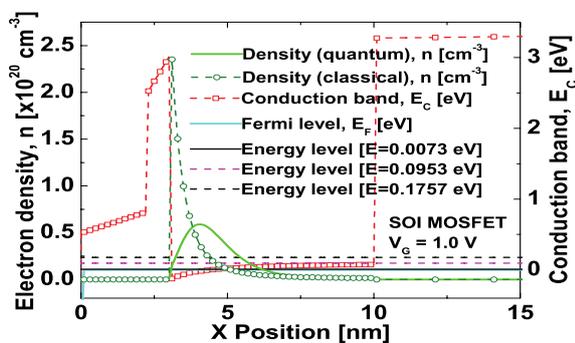


**Figure 6.** A schematic for SOI Structure with 32 nm gate length.

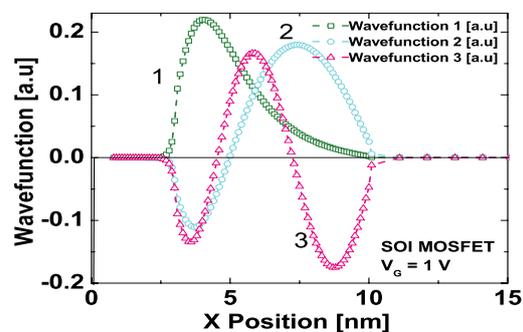


**Figure 7.** Electron density, conduction band and energy levels, bias  $V_G = 0.5$  V.

The classically calculated electron density peak observed at the interface of oxide and semiconductor. The quantum mechanically calculated electron density will peak away from the oxide-semiconductor interface due to displacement of charge from the interface [10]. After applied gate voltage to  $V_G = 0.5$  V, we still observe two discrete energy levels in the quantum well as illustrated in Figure 7. Also, we see the peak of the classically calculated electron density at the interface of oxide-semiconductor is much larger than the quantum-mechanically calculated electron density. At  $V_G = 1.0$  V, we obtain three discrete energy levels in the quantum well with corresponding wavefunction for these energy levels shown in Figures 8, and 9, respectively. We summarise that in future technology the bulk MOSFET will be replaced by an ultra-thin-body (UTB) silicon-on-insulator (SOI) on the basis of better electrostatic integrity, low channel doping to get high mobility, high dielectric material to prevent gate leakage and metal gate [11, 12, 13].



**Figure 8.** Electron density, conduction band and energy levels for the SOI structure, applied bias  $V_G = 1.0$  V.



**Figure 9.** Electron wave functions across the channel of the SOI MOSFET, applied bias  $V_G = 1.0$  V.

### 3. MOS Structure for $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$ Channel Transistor

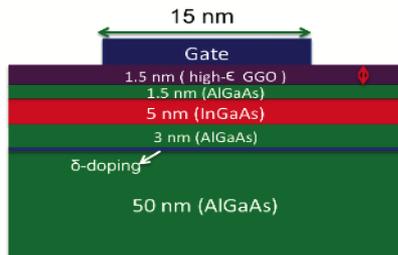
We investigate the effect of confined channel in the InGaAs channel MOSFET with a gate length of 15 nm aimed for the future sub-22 nm Si technology [14]. The IF MOSFET is derived from a HEMT structure which has (a) an oxide layer to prevent gate tunneling, (b) a  $\delta$ -doping layer placed below the channel. This placement allows the metal gate to maintain a good control of carrier transport in the channel, and (c) an ultra-thin body like channel [15].

We have used, Poisson-Schrödinger equation to obtain conduction band profile, energy levels, wavefunctions and electron density in a confined body of this heterostructure MOSFET. The III-V MOSFET consists of InGaAs channel with thickness of 5 nm, high- $\epsilon$  dielectric layer of Gadolinium Gallium Oxide (GdGaO) as a gate dielectric with a thickness of 1.5 nm and whose dielectric constant is  $\epsilon_{\text{GdGaO}} = 20$ . The InGaAs channel is located between AlGaAs layer with a thickness of 1.5 nm and AlGaAs layer of a thickness of 3 nm. The  $\delta$ -doping layer is placed below the channel with a concentration of  $7 \times 10^{12} \text{ cm}^{-2}$ . The AlGaAs (bottom of the structure) is grown as a thick buffer layer of 50 nm as shown in Figure 10. The whole device is grown currently on a GaAs substrate.

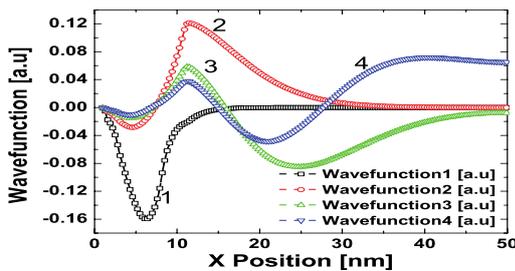
#### 3.1. MOS structure for 15 nm gate length InGaAs MOSFET

Figure 11 and Figure 13 shows the conduction band, discrete energy levels, and electron concentration obtained from 1D self-consistent simulations biased at  $V_G = 0.5$  V, and  $V_G = 1.0$  V. The peak of the classically calculated electron density at the interface of oxide-semiconductor exhibits a high density. The quantum-mechanically calculated electron density has a peak which moves away from the oxide semiconductor interface toward the bottom of the channel. The different behaviour shows that the peak of the density lies at the bottom of the channel in the IF MOSFET, whereas the density peak lies at the top of the channel in the bulk Si and SOI MOSFETs. We observe here four discrete energy

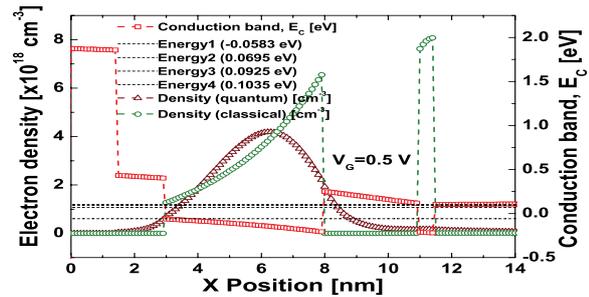
levels, the last two very close with a separation of only 11 meV. The corresponding wave functions in the quantum well are shown in Figure 12.



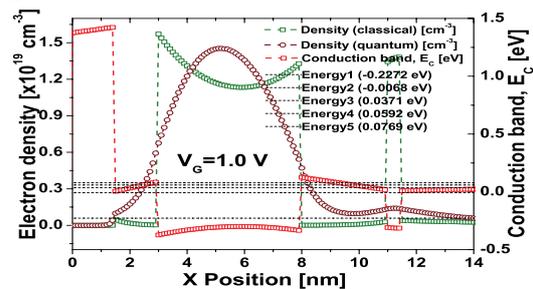
**Figure 10.** Cross-section of the 15 nm gate length InGaAs MOS structure with a high dielectric layer below the metal gate.



**Figure 12.** The wavefunctions across the channel of 15 nm gate length InGaAs MOSFET, applied bias  $V_G = 0.5$  V.



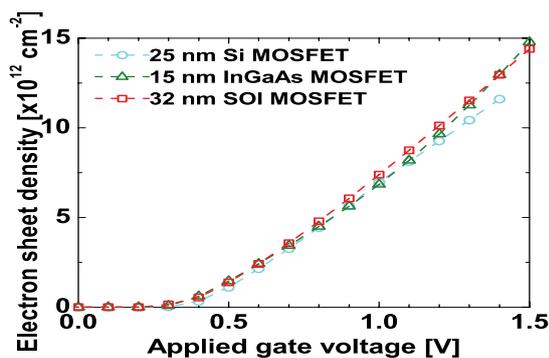
**Figure 11.** Conduction band, electron density and discrete energy levels across the channel of 15 nm gate length InGaAs MOSFET, biased  $V_G = 0.5$  V.



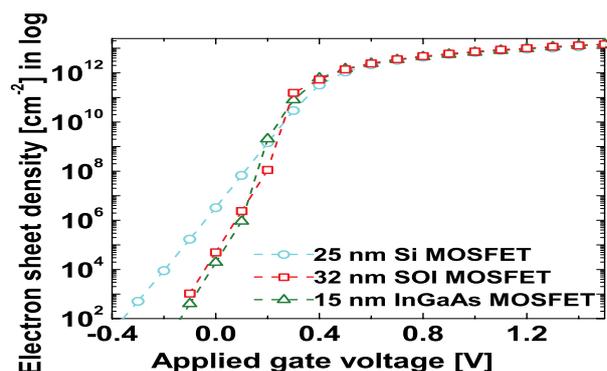
**Figure 13.** Conduction band, electron density, and discrete energy levels under biasing  $V_G = 1.0$  V across the channel of InGaAs MOSFET

#### 4. Comparing results of sheet densities for Si bulk , SOI and IF MOSFET

We have calculated electron sheet densities (quantum mechanically) from 1 D Poisson-Schrödinger solver for the 25 nm gate length Si, the 32 nm gate length UTB SOI and the 15 nm gate length InGaAs MOSFETs as a function of the applied gate voltages, which are shown in the Figure 14 on a linear scale. For all cases, we observe that the electron sheet density increases linearly with increasing of the applied voltage.



**Figure 14.** Electron sheet density versus applied gate bias on a linear scale in a MOS structure of the 25 nm gate length Si, the 32 nm gate length UTB SOI, and the 15 nm gate length In<sub>0.3</sub>Ga<sub>0.7</sub>As MOSFETs. 32 nm gate length.



**Figure 15.** Electron sheet density versus applied gate bias on logarithm scale in a MOS structure of the 25 nm gate length Si, 32 nm gate length UTB SOI, and the 15 nm In<sub>0.3</sub>Ga<sub>0.7</sub>As MOSFETs.

Figure 15 shows the results of electron sheet density on a logarithmic scale. The goal is to determine and compare the subthreshold slope (SS) of three different MOS structures. We have calculated the SS from (open circles) the Si MOS structure, which is almost 88 mV/dec. This value is greater than the theoretical value of  $SS = 60$  mV/dec predicted for an ideal MOS transistor at room temperature [13]. The SS for the SOI MOS structure (open squares) is almost 62 mV/dec. This value is much closer to the value  $SS = 60$  mV/dec of an ideal MOS transistor. Furthermore, we have determined the SS (open triangles) for In<sub>0.3</sub>Ga<sub>0.7</sub>As MOS structure, which is almost 64 mV/dec and is also very close to the ideal value of  $SS = 60$  mV/dec [8, 16].

## 5. Conclusions

These investigations have been carried out using a self-consistent solution of 1D Poisson-Schrödinger equation to determine conduction band profiles, electron density, energy levels (eigenstates) and wavefunctions (eigenfunctions) in the Si, SOI and InGaAs MOS structures under external potential. We have afterwards simulated the electron sheet density as a function of the applied gate bias and made a comparison among the three device structures, the 25 nm gate length bulk Si, 32 nm UTB SOI, and 15 nm gate length InGaAs MOSFETs. We have then calculated sub-threshold slope (SS) from the dependence of sheet densities on applied bias on logarithmic scale. We observe that the SS behaviour in the bulk Si becomes much worse than those in the SOI and in the InGaAs MOSFETs. Clearly, the UTB architectures deliver nearly ideal (theoretical ideal value of  $SS = 60$  mV/dec) value of SS (almost 62 mV/dec) thanks to their superior control of the carrier transport in a channel.

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