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Bit error rate evaluation in high speed communication channels

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Abstract. This work offers calculate technique probability errors in transmitter – receiver path during the design phase with apply theory of probability elements, which is based on results of transient process modeling. As estimation, designed method was verified by comparison his results with computer experiment results. Implementation and using variants of represented algorithm are offered.

1. Introduction

Serial transceivers are essential part of transfer data electronic systems. They provide stability and fast information exchange between devices by external communication lines.

Actual transceivers with data rate 1 Gbps and more should provide number of errors less 10^{-12} . With current data rates (1,25/2,5/3,125 Gbps and more) impact of phase distortion increases on transmitted data integrity.

Bit Error rate (BER) is important and obvious criterion of transceiver path work and is defined as number of errors divided by total number transmitted bits. Currently measuring devices manufacturers offer technique of measurement BER for a couple transmitter – receiver, but actual problem is estimation BER during the design phase.

Eye diagram is image of superposition all bit periods of measured signal. Estimation of correctly data transmit is provided by apply mask to eye diagram. Intersection of mask with eye diagram means error. But this method provides only rough estimate.

There are algorithms estimation BER which is based on some basic principles. Comparison of main methods is represented in Table 1. Methods, which is based on results SPICE modeling, require long time modeling. Example, confirmation of BER level less 10^{-12} require modeling transmit more 10^{12} bit. Statistical methods provide high precision of estimation and high calculate speed. Algorithm types is possible, which can have universality with modeling different transmitter – receiver path types.

Table 1. Comparison common types of evaluation methods BER.

methodology	simplicity	speed	universality
SPICE – modeling	+	-	+
worst-case modeling	+/-	+/-	+
using IBIS models	+	+/-	-
statistical method	+/-	+	+



2. The task of receiving data

The task of any transceiver is to trusty exchange information between two paired devices. It is necessary to control all critical nodes that are subject to changing conditions of the circuit operation and the influence of jitter. One of the main elements of the receiver, requiring attention, is the first trigger of the shift register in the receiver, which latches the input data stream and converts it into an internal data signal Q_CORE (Figure. 1).

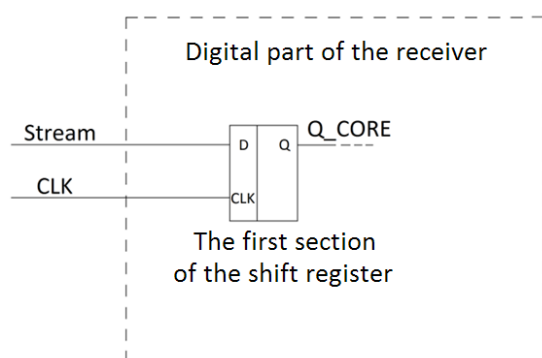


Figure. 1. The first trigger of the shift register of the digital part of the receiver. The Stream and CLK signals are a data signal and a clock signal, respectively. The phase of the CLK signal is restored from the Stream signal using the Clock and Data Recovery (CDR) block. The Stream data signal is received from the interface part of the receiver, the CLK reference signal is produced by a phase and frequency adjustment unit called the CDR. To successfully pass the data signal with the subsequent deserialization of the stream, in general, it is necessary to observe the required phase and amplitude relations between these signals.

From the central limit theorem of probability theory it is known that the sum of a sufficiently large number of weakly dependent on each other random variables having the same scope, subject to the normal distribution. Based on this situation it is assumed that the noise, which is the source of bit errors has a normal distribution in amplitude. Therefore, for the treatment of the consequences of his influence can be to use the tools of probability theory.

The parasitic elements of the topology and the housing deteriorate the parameters of the transmitted signal [4]. Therefore, when the worst bit sequences are transmitted, for example "0101" or "1110", the signal amplitude is distorted and the deterministic jitter increases [5].

Two types of causes of bit errors can be identified. First, at low values of the signal-to-noise ratio, the transmitted signal can cross the receiver switching level (Figure 2), and, consequently, the probability of an error in receiving increases.

Secondly, the necessary condition for obtaining correct data receiver is that the permitted switching timing between the data signal DATA and the clock signal CLK input to flip-flop in the digital portion of the receiver (Figure. 3).

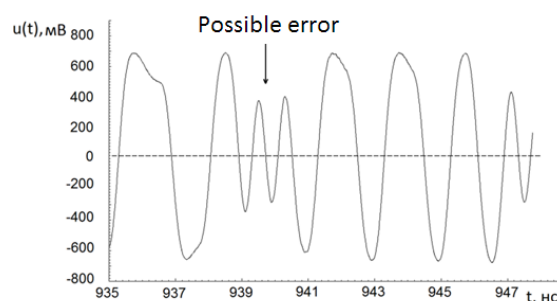


Figure 2. Amplitude distortion effect.

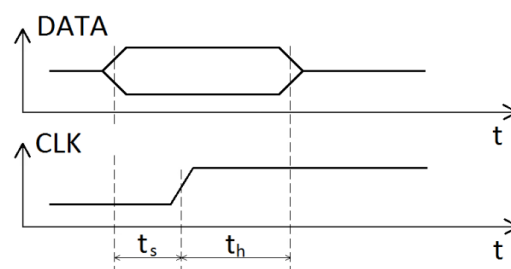


Figure 3. Setup and Hold times.

The data must arrive at the input no later than the minimum setup time (t_{s_min}) to the clock edge. Also, the data must remain at the input after the clock signal drops no less than the minimum hold time

(t_{h_min}). If one of the conditions is not met, the recording of the correct information in the first flip-flop of the shift register becomes impossible.

3. Description of the BER analysis method

During transmission, a bit error can occur regardless of two reasons: amplitude or phase distortion of the input signals. In this case, the error probabilities of these two species will be different. The total BER will be equal to the algebraic sum of the probabilities of bit errors in amplitude and phase as two independent events. The proposed algorithm for estimating BER is a separate analysis of the magnitude of the probability of errors due to phase and amplitude distortions. The analysis of the bit stream of data is carried out in regions A and B, respectively (Figure. 4).

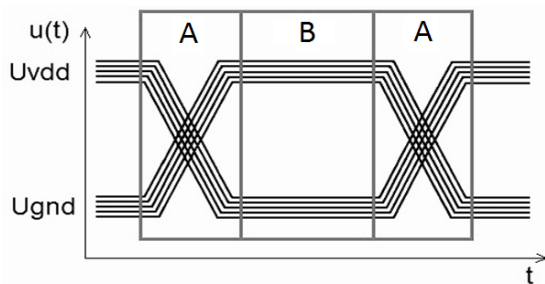


Figure 4. Areas of eye diagram analysis. As was shown above, there are various reasons for the occurrence of bit errors in the transmission of digital data. Therefore, in the process of analysis, it is expedient to divide the eye diagram into regions of influence of the described factors.

On the basis of the obtained values, separately for the zero level and the unit level, the RMS deviation of the random variable σ_A (RMS) is calculated from the signal amplitude:

$$\sigma_A = \sqrt{\frac{1}{n} \sum_{i=1}^n (A_i - m_A)^2}. \quad (1)$$

The mathematical expectation m_A is known: this is either the logical unit level or the logical zero level. The random variable A_i is the instantaneous amplitude of the signal, n is the number of instantaneous amplitude measurements. The number of samples is predetermined. Thus, the probability density function is determined for each of two cases:

$$P_{DATA}^A(A) = \frac{1}{\sigma_A \sqrt{2\pi}} \exp\left(-\frac{(A - m_A)^2}{2\sigma_A^2}\right), \quad (2)$$

where A is the instantaneous amplitude of the signal.

Next, the probability density is integrated over the range corresponding to the case of error generation at the intersection of the receiver response level for each case: (2a) for the “one” level and (2b) for the “zero” level. The probabilities obtained are multiplied by the number of bits in the pattern and added (3).

$$BER_A^0 = \int_{A_{tr}}^{+\infty} P_{DATA}^A(A) dA, \quad (2a)$$

$$BER_A^1 = \int_{-\infty}^{A_{tr}} P_{DATA}^A(A) dA, \quad (2b)$$

$$BER_A = BER^0 + BER^1, \quad (3)$$

Where BER_A^0 – the probability of an error in the transfer of zero bit, BER_A^1 – the probability of an error in the transmission of a one bit, BER_A – the total error probability, A_{tr} – the threshold level of the receiver trigger switching.

BER analysis by phase. In Figure. 5 illustrates the distribution of data phases P_DATA and phases of the clock signal P_CLK at the input of the receiver. In this case it is necessary to satisfy the condition under which the data and clock edges are arranged relative to one another no closer than t_{s_min} - minimum setup time of the data signal. Analysis the relative position of the fronts of these signals to meet the minimum hold time t_{h_min} is similar.

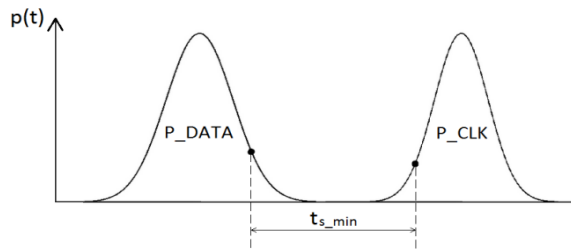


Figure 5. Probability distribution of the phases of the data signal and the clock signal. The probability distribution of signal fronts is described by means of a normal distribution. The occurrence of an error can be considered as the simultaneous occurrence of two random events, for which the condition of time relations between the arrival of the clock signal and the data signal is not satisfied.

The RMS signals DATA and CLK, respectively, have the form:

$$\sigma_{\text{DATA}} = \sqrt{\frac{1}{n} \sum_{i=1}^n (A_i - m_T)^2}, \quad (4)$$

$$\sigma_{\text{CLK}} = \sqrt{\frac{1}{n} \sum_{i=1}^n (A_i - m_T)^2}, \quad (5)$$

где m_T – mathematical expectation, the moment of arrival of the signal front corresponding to an ideal grid of clock signals.

The distribution of the probability density of the arrival times of the DATA and CLK signal fronts, respectively, is:

$$P_{\text{DATA}}^T(t) = \frac{1}{\sigma_{\text{DATA}} \sqrt{2\pi}} \exp\left(-\frac{(t - m_t)^2}{2\sigma_{\text{DATA}}^2}\right), \quad (6)$$

$$P_{\text{CLK}}^T(t) = \frac{1}{\sigma_{\text{CLK}} \sqrt{2\pi}} \exp\left(-\frac{(t - m_t)^2}{2\sigma_{\text{CLK}}^2}\right), \quad (7)$$

where t is the arrival time of the signal front.

RMS deviation of the phase of the data signal and the clock signal are reduced to the total RMS by the formula:

$$\sigma = \sqrt{\sigma_{\text{DATA}}^2 + \sigma_{\text{CLK}}^2}, \quad (8)$$

It is assumed that the phase of the data is unchanged, and the total RMS has a phase of the clock signal. In this case, BER is the probability of the edge crossing of the CLK signal of the minimum thresholds of the setup and hold times t_{s_min} and t_{h_min} . The resulting BER can be calculated from the formula:

$$\text{BER}_T = 1 - \int_{t_{s_min}}^{T - t_{h_min}} P_{\text{CLK}}^T(t) dt, \quad (9)$$

where T is the duration of one bit of data.

In integrated circuits, bitstream transmission produces deterministic jitter, partly due to intersymbol interference. In this case there is the background of the length of several bits results in a variation of the duration of a single bit interval (Figure. 6).

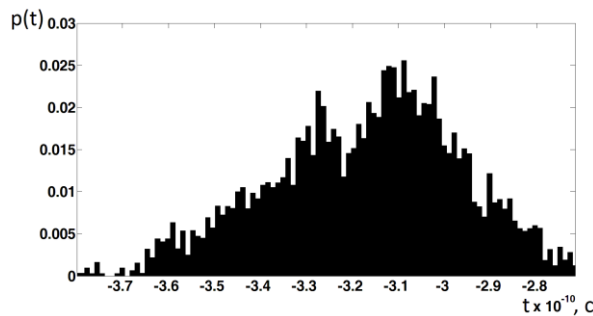


Figure 6. Distribution of the probabilities of the phases of the data signal and the clock signal taking into account the deterministic jitter. As can be seen in the figure, the distribution has two maxima, which should be taken into account during the analysis. This distribution depends on the pattern of the transmitted bit code.

In this case, the sophisticated model takes into account the difference in the lengths of bit intervals, depending on the sequence of transmitted data. The algorithm analyzes the transmitted code, making bit patterns that take into account the history of several data bits. For example, if the length of the pattern is 5, the total number of templates will be 32. In this case, the length of the last bit depends on the sequence of the preceding four bits. Taking the data stream as infinite, the algorithm calculates the probability of the appearance of one or another template, giving them a weighting factor P_j :

$$P_j = \frac{D}{N} * M_j, \quad (10)$$

where D is the length of the pattern in bits, N is the total number of transmitted bits, M_j – The number of repeats of the j th template in the sending of the transmitted bits.

In this case, the probability density function for each of the cases will have the form:

$$P_{DATAj}^T(t) = \frac{1}{\sigma_{DATA}\sqrt{2\pi}} \exp\left(-\frac{(t - m_{tj})^2}{2\sigma_{DATA}^2}\right), \quad (11)$$

where m_{tj} – the mathematical expectation for each of the distribution variants.

Also, as it was described earlier, the RMS phases of the data signal and the clock signal are reduced to the total RMS according to the formula (8).

The presence of two or more distribution peaks since the arrival of data bits means that in the formula (4) will be used to its limits of integration according to each of the data signal distribution maxima. In this case, the RMS for each of the distributions is assumed to be the same. Then integration is performed according to the formula (11) for each of the patterns:

$$BER_{Tj} = 1 - \int_{t_{s_minj}}^{T - t_{h_minj}} P_{CLKj}^T(t) dt, \quad (12)$$

where t_{s_minj} и t_{h_minj} – minimum setup and hold times corrected according to the offset of the data signal distribution center for each of the cases.

Thus, the BER in the signal phase will be the algebraic sum of the BERs for each of the patterns, taking into account their weighting factors:

$$BER_T = \sum_{j=1}^n BER_{Tj}, \quad (13)$$

where n – the number of distribution maxima.

The resulting path BER is a BER amount, calculated by the signal amplitude and phase of the signal:

$$BER = BER_T + BER_A \quad (14)$$

4. Check and use of the methodology.

The technique was tested on the basis of SPICE modeling of the path connecting the transmitter and the receiver operating on the SpaceWire interface at bit frequencies up to 3.125 Gbit / s.

A model of an ideal input trigger of a receiver with a fixed switching level and minimum setup and hold times was created. At its input signal is fed to the data encoded in 8B / 10B and clock signal with a known value of RMS phase and amplitude noise. The length of the bit interval was 320 ps, which corresponds to a bit frequency of 3.125 Gbit / s. After that, the number of erroneously received bits was counted. The obtained data were compared with the results of the prediction of the error rate according to the developed method. A series of computer experiments with a gradual increase in the complexity of the model and the value of jitter. The results are recorded in Table. 2. Thus, A is a model with zero setup and hold times of the receiver's input trigger and with a clock signal drop located in the middle of the bit interval. Model B takes into account the times t_s and t_h , model B - additionally takes into account the different positions of the clock edge within the bit interval.

It was found that if the signal arriving at the receiver satisfies the electrical specifications of the standard in amplitude, then the amplitude noise does not make a significant contribution to the total BER.

Table 2. The results of the verification of the proposed BER evaluation methodology.

m, ps	σ , ps	The calculation formula	Predicted BER*10 ^{^(-3)}	Modeled BER*10 ^{^(-3)}
160	55	$BER_T = 1 - \int_{t_{s,min}}^{T - t_{h,min}} P_{CLK}^T(t) dt$	23,5	24,8
160	55		49,9	55,4
160	65		94	102,6
160	70		160,9	161,5

The sample size was 5000 bits, the setup time was -22 ps and -12 ps, the hold time was -31 ps and -56 ps for writing the unit and zero, respectively.

As can be seen from the table, as part of the verification error by BER estimation method described above is an average of 10%, which is sufficient to assess the order of magnitude of BER at the stage of the transceiver design. Also, with an increase in the sample size, the error decreases.

5. Conclusion.

The described technique is implemented as a program in the MATLAB environment. Before working in the environment files are imported simulation results. This technique can also be used with the VERILOG model, which receives data and clock signals, and generates an analog voltage equal to BER. This method allows us to estimate the BER value with high accuracy, without resorting to long-term SPICE modeling, regardless of the embodiment of the transmitter-receiver path.

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