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Research on FPGA filtering method of Gearbox fault signal

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Abstract. Gearboxes are an important part of marine machinery and equipment such as steam turbines and generators. Under normal circumstances, the performance of the gearbox directly affects whether the relevant mechanical equipment can normally work, so it is very important to detect and eliminate the gearbox failure. The gearbox vibration signal contains a wealth of working status information, and the use of gearbox vibration signal diagnosis is a common method. Since the vibration signal contains strong noise, denoising is the primary task of fault feature extraction. Aiming at this practical problem, in this paper, a denoising filter based on FPGA environment is designed. This filter is used to process the simulated gear fault signal with a signal-to-noise ratio (SNR) of 0.1206. By comparing the time domain diagram and frequency domain diagram before and after processing, the feasibility of using FPGA to realize the mechanical vibration signal processing is verified. This is of great practical significance to the miniaturization and real-time of the mechanical fault diagnosis system.

1. Introduction

The vibration signal is the carrier of the gearbox fault characteristics. Analyzing the vibration signal of the gearbox, extracting the fault characteristics, and then judging the fault of the gearbox according to the fault characteristics. This is the common methods of fault diagnosis of the gearbox. At present, the denoising methods for mechanical fault signals include wavelet transform, empirical mode decomposition (EMD), FIR filter, etc. These methods have been proven to be effective methods. The signal can be filtered by the hardware DSP, but the DSP has poor flexibility and low operation speed, which limits its application.

In the past ten years, the rapid development of various data processing software and hardware has greatly promoted the development of mechanical fault diagnosis technology and made it possible for real-time on-line diagnosis of mechanical equipment. Moreover, the fusion of gearbox fault diagnosis technology and contemporary frontier science is the development direction of gearbox fault diagnosis technology. FPGA that is, field programmable gate array, its internal clock delay is small, all control logic is completed by hardware, fast, high efficiency, high reliability, flexible development mode, easy to modify and so on [3]. At present, the research on FPGA for high-speed data transmission, high-speed data acquisition, and high-speed logic control has aroused great interest [4,5,6]. This paper implements a 50-stage low-pass filter design. The correctness of this method is proved by the experiment of the simulation signal.



2. THE Mathematical model of gear meshing vibration signal

In the normal operation of the gear, the frequency domain characteristic of the vibration signal is mainly the meshing frequency component, and the higher harmonics are sequentially attenuated. At the low frequency, there are gear shaft frequency shift and high harmonic components mf_r ($m = 1, 2, \dots$). Whenever one tooth engagement is completed, the gear meshing stiffness is changed once. According to the mechanical model of gear meshing, the gear vibration signal is expressed as (1):

$$x(t) = r_n(t) \sum_{k=1}^M [\cos 2\pi f_r t + \cos 2\pi \times 2f_r t + [\cos 2\pi k f_z t + \varphi_k(t)]] \quad (1)$$

Assume:

$$e(t) = \sum_{k=1}^M [\cos 2\pi f_r t + \cos 2\pi \times 2f_r t + [\cos 2\pi k f_z t + \varphi_k(t)]] \quad (2)$$

That is:

$$x(t) = r_n(t) \times e(t) \quad (3)$$

In the formula:

$r_n(t)$ -- the fault gear pair meshing stiffness function, the fundamental frequency of which is the frequency of the fault gear shaft;

$\varphi_k(t)$ -- the phase change function caused when the faulty gear pair is engaged;

f_z -- the meshing frequency of the gear;

f_r -- the number of revolutions of the gear shaft (rev/sec);

K -- the highest harmonic order of the meshing frequency;

Z -- the number of teeth of the gear;

Among them: $f_z = f_r \times Z$

When the meshing gear is not faulty, $r_n(t)$ and $\varphi_k(t)$ in equation (1) do not change with time and are a constant. At this time, equation (1) represents the mathematical model of the normal vibration signal when the gear fails. When $r_n(t)$ modulates the amplitude of the normal vibration signal, $\varphi_k(t)$ will modulate the phase of the normal signal, the type of gear failure is different, and the model of the modulation function is different. Gear faults are generally divided into two broad categories, local faults, and distributed faults. Typical local faults include cracks, broken teeth, etc.; distributed faults are somewhat etched, tooth surface wear, pitch error, and installation eccentricity. The local failure will cause a sudden change in the gear meshing point. The abrupt period is the frequency and harmonic of the gear shaft, and the amplitude of the normal vibration signal is mainly modulated. Distributed faults during gear meshing vibration, for example, when there is uniform wear on a plurality of tooth flanks, the fault is gradually extended from one tooth to the other tooth surface, and the fault simultaneously modulates the amplitude and phase of the normal gear meshing vibration signal. Equations (4) and (5) give mathematical models of amplitude modulation and phase modulation signals when the gears have distributed faults.

$$r_n = A + \sum_{n=1}^N a_n \sin(2\pi n f_r t + \alpha_n) \quad (4)$$

$$\varphi_k(t) = \sum_{k=1}^M b_k \sin(2\pi k f_r t + \beta_k) \quad (5)$$

In the formula:

A, a, b are amplitude coefficients;

α, β is the initial phase;

n natural number 1, 2, 3, ..., N , N is the maximum number of harmonics wave;

f_r is the rotation frequency of the gear;

3. Simulation analysis of gear distributed fault vibration signals

For normal gears, the vibration signal frequency includes the meshing frequency and its higher harmonics, the weak shaft frequency and its harmonics wave. When there is a distributed fault in gear, the amplitude modulation and phase modulation functions $r_n(t)$ and $\varphi_k(t)$ of the vibration signal are expressed as shown in equations (4) and (5). Since the phase modulation function is a weak function, the influence of this term on the signal phase is not considered in the simulation signal of this paper.

The simulation parameters of the simulated signal are:

the shaft rotation frequency of the fault gear is $f_z = 5\text{Hz}$;

the number of teeth of the faulty gear is $Z=32$;

meshing frequency $f_z = 32 \times 5\text{Hz}$;

The mathematical expression for simulating the fault-free gear vibration signal is:

$$x(t) = \cos(2\pi f_r t) + 0.2 \cos(4\pi f_r t) + 4\cos(2\pi f_z t) + \cos(4\pi f_z t) + 6 \cos(6\pi f_z t) \quad (6)$$

Figure 1 is a time domain diagram and frequency domain diagram of a simulated fault-free gear vibration signal. It can be seen from the frequency domain diagram that the vibration signal caused by the gear meshing is strong, and the vibration signal caused by the rotating shaft speed is weak.

Formula (2.5) is a mathematical expression when the gear has a pitch error:

$$\begin{aligned} x(t) &= r_k(t)e(t) \\ r_k(t) &= 1.5 + \cos(2\pi f_r t) + 0.2 \cos(4\pi f_r t) + 0.1\cos(6\pi f_r t) \\ e(t) &= \cos(2\pi f_r t) + 0.2 \cos(4\pi f_r t) + 4\cos(2\pi f_z t) + \cos(4\pi f_z t) + \cos(6\pi f_z t) \end{aligned} \quad (7)$$

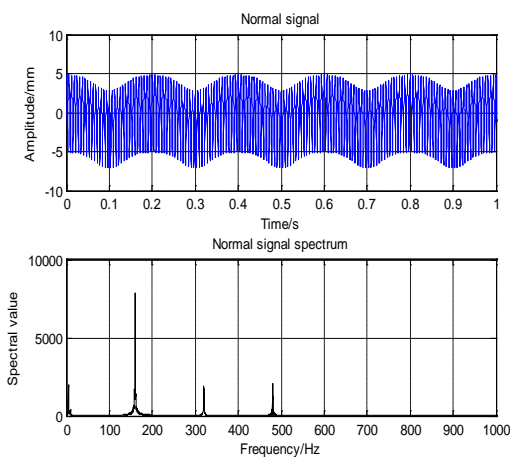


Figure 1 Time and frequency domain of normal signals.

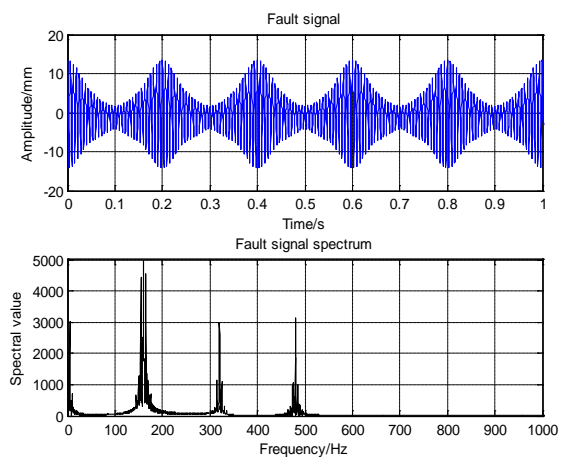


Figure 2 Time domain and frequency domain of fault signal.

Its time-domain diagram and frequency domain diagram are shown in figure 2. Obvious amplitude modulation information appears on the time domain diagram, and the sidebands were appearing at the meshing frequency and its harmonics can be seen on the frequency domain diagram, the frequency interval between the sidebands is exactly the frequency of the faulty gear axis. It can be further seen that the energy of the frequency shift and its harmonics at the low frequency is increased compared with the normal signal. This information is characteristic information of the gear failure.

Figure 3 shows the gear fault vibration signal with a signal-to-noise ratio (SNR) of 0.1206 and a mean square error of 4.2617. The amplitude modulation information is completely submerged in the noise on the time domain diagram, and the fault feature signal disappears.

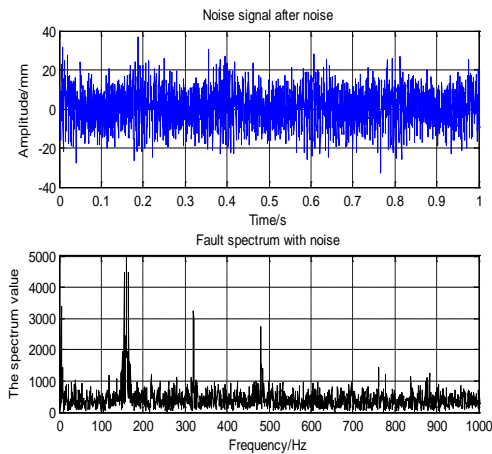


Figure 3 Time and frequency domain of fault signal after noise.

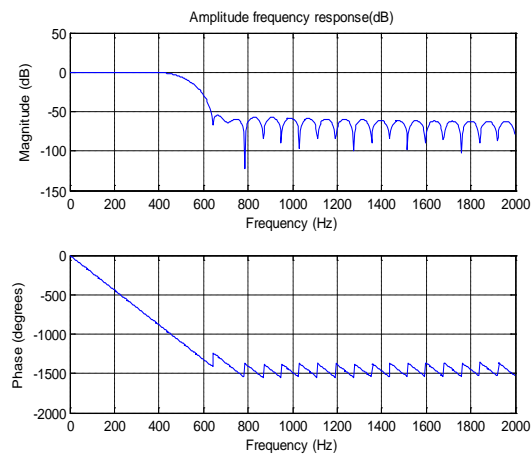


Figure 4 Amplitude frequency response characteristics.

4. FPGA-based filter design

4.1. FIR digital filter principle

The digital filter is a discrete-time linear time-invariant system implemented by a finite precision algorithm to perform signal filtering processing.

The system function of an n -step FIR digital filter is shown in formula (6). In the formula, $h(n)$ is the unit impulse response sequence of FIR, also known as the coefficient of the filter. $X(z)$ and $Y(z)$ are the z transformation of input signal and output signal respectively. The design of FIR filter is to solve the filter coefficient which meets the technical parameters.

$$H(z) = \sum_{n=0}^N h(n)z^{-n} = \frac{Y(z)}{X(z)} \quad (8)$$

From equation (6), the constant coefficient linear difference equation representing the input-output relationship can be obtained as shown in equation (7):

$$y(n) = \sum_{m=0}^N h(m)x(n-m) \quad (9)$$

4.2. FIR coefficient determination

According to the simulated gear fault vibration signal, the technical parameters of the filter are set as follows: the cut-off frequency of passband is 500Hz, the minimum attenuation of stopband is 20dB, and the sampling frequency of the signal is 4KHz. Considering that it takes up as little resources as possible in FPGA and the operation speed problem, the order of the filter should be as little as possible. The selection of window function has great influence on the stopband attenuation of filter. According to the design requirements, hamming window is selected in the design to obtain the amplitude-frequency response curve and phase-frequency response curve of the 50-order filter, as shown in figure 4.

4.3. FPGA implementation of FIR filter

There are four schemes to design direct filter with FPGA: serial structure, parallel structure, distributed structure and the way to refer to IP core. If the FPGA chip provides the IP core, then the IP core scheme is preferred. Since the IP core code is written by professionals and designed with it, the filtering efficiency is higher.

The FPGA implementation of the filter is divided into five steps:

- (1) In the new project, the target device is selected as Cyclone IV series chip EP4CE15F17C8, and the top file is Verilog HDL type.
- (2) Start the "MegaWizard Plug-In Manager" tool in the QuartusII 13.0 software and select "DSP--Filters--- Compiler v13.0".
- (3) Load the filter coefficients and set the appropriate coefficient quantization bit width. This paper sets 13Bit quantization.
- (4) Create a new Verilog HIL File type resource file and instantiate the generated IP core component.
- (5) Compile the program all the way, after downloading the filter program to the FPGA.

5. Filter denoising experiment of gearbox fault signal

The experimental scheme used in this paper is shown in figure 5.

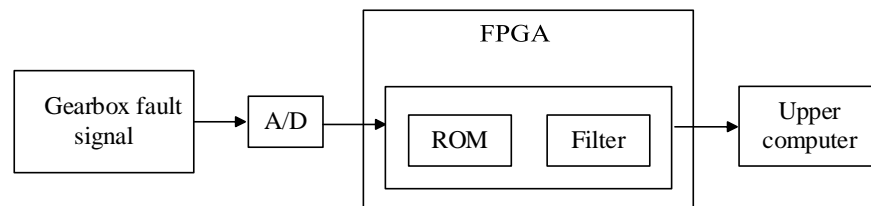


Figure 5 Experiment scheme.

The data of the gear fault vibration signal of this time is generated by the mathematical model of equation (1), the signal-to-noise ratio is 0.1206 and the mean square error is 4.2617. To verify the performance of the filter implemented in FPGA, the gearbox fault signal data of the model simulation needs to be stored in the ROM. This paper creates a ROM in the FPGA. The word length and word width of the created ROM are 4096 and 13 bits, respectively.

After storing the data of the gearbox fault signal in the ROM, verify the filter designed in the current Matlab environment with the IP in the FPGA. Figure 6 shows the RTL schematic for implementing ROM and filters in an FPGA.

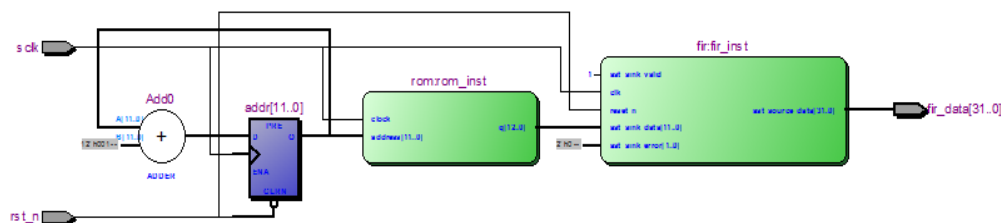


Figure 6 Schematic diagram of filter experiment.

As show in Fig. 1 and Table 1, three scheme comparing.As shown in Figure 6, Add0 and addr together form a 12-bit address counter,The address of the ROM is connected to it. Whenever a system clock is coming, the address counter sends an address signal to the ROM. Whenever a system clock is sent, the address counter sends an address signal to the ROM, and the data stored in the ROM in the address is input to the filter. The designed filter is processed and then output in parallel.

In the experiment, the pins of the FPGA device are assigned to the input and output ports in Figure 6, download the program to the FPGA and run. The filter filters the gearbox fault signal stored in the ROM, and the processed signal is processed. The port fir_data[31..0] output is read into the host computer through the JTAG port on the FPGA board. Figure 7 is a time domain, and frequency diagram of the signal read into the host computer. Compared with the original signal (i.e. Figure 3), the fault characteristics of the time domain signal amplitude modulation are improved, and the high-

frequency signal in the frequency domain diagram is filtered out. Indicating that the denoising effect of the FPGA on the gearbox fault vibration signal is significant.

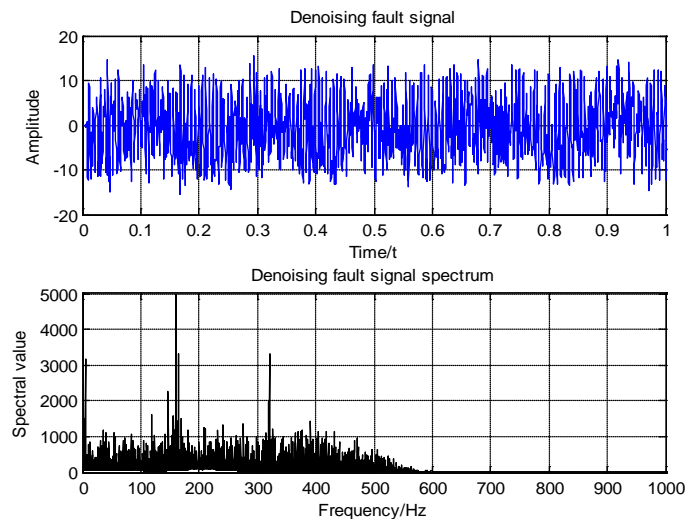


Figure 7 Time and frequency domain of the signal processed by FPGA.

6. Conclusion

Using Matlab software to solve the filter coefficients of a given technical parameter. Under the FPGA environment, the direct-type structural filter design with given filter coefficients is realized. The signal-to-noise ratio of the simulation is 0.1206 and the mean square error is 4.2617. The gear fault signal is processed by the filter implemented by the FPGA. The time domain and frequency domain diagrams of the signals before and after processing are compared to prove the effectiveness of using FPGA to denoise the gear fault vibration signal. This result is to diagnose the gearbox fault. The miniaturization and real-time of the system have strong practical significance.

Acknowledgments

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