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PAPER

A VLSI implementation method of a compressor for audio systems

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Abstract: In this paper, we present a VLSI implementation method on a dynamic range controller, audio level compressor, which is used to make sound effects as an important functional part in a digital audio system on a chip. To implement the gain calculation in a digital dynamic range controller, a power calculation with fractional numbers is required and it is difficult to be performed directly in a digital audio system. We introduce a polynomial expression to approximate the power operation, then the gain calculation is easily performed with a number of additions, multiplications and a division. Based on the gain calculation method of the gain, an efficient VLSI architecture with some arithmetic circuits is proposed. We designed the circuit of a 16-bit audio level compressor by using a hardware description language, VHDL. As a result of the compact circuit design, the 16-bit compressor has only 5,688 gates by 1 μm CMOS gate array technology. The design and simulation results show that the presented audio level compressor has high performance and can be integrated into an audio system on a chip for practical use.

Keywords: Audio signal, Dynamic range controller, Compression ratio, Gain calculation, Attack time and release time.

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1. INTRODUCTION

Digital audio systems have advantages in audio signal transferring, recording and delay controlling over the conventional analog systems. Various digital filters on digital signal processors (DSPs) for getting the frequency responses have been proposed [1–3]. Because of the development of VLSI (Very Large Scale Integration) technology, more and more conventional analog circuits for audio signal processing have been replaced by high performance integrated circuits (ICs), and the audio world has been continuously moving toward a more complete digital system on a VLSI chip. For example, it is desired that an audio system with a number of functional modules such as analog-to-digital and digital-to-analog converters, CPU, DSPs, memory and dynamic range controllers is implemented on a VLSI chip, called audio system on a chip [4]. To realize such a digital audio system with high performance and low cost, it is important to develop an efficient VLSI implementation method for the audio signal processing.

Dynamic range control of audio signal levels is a general requirement to get sound effects [5]. Compressors and limiters are such dynamic range controllers. Compressors and limiters may be used to prevent peaks exceeding the maximum usable value, and expanders and noise gates can be applied to reduce background noise in an audio system. As shown in Fig. 1, a dynamic range controller performs the peak detection, gain calculation, attack time and release time control in the functional block, GAIN CONTROL, and then applys the gain to control the signal level. In a conventional dynamic range controller with analog circuits, voltage-controlled amplifier (VCA) is used [6,7] to control signal level. In general, the VCA circuit has the nonlinear input-output characteristics, which result in the harmonic distortion in the output signal.

Digital dynamic range controllers may implement the same functional blocks as the analog circuits. Thus, the harmonic distortion arisen by VCA may be avoided by using the multiplication. However, the main problem is to perform the calculation for the power transformation, that is, how $x^y (0 < x, y < 1)$ is calculated efficiently with few operations and less hardware. So far, we have presented a number of methods for implementing digital dynamic range controllers on a digital signal processor [8–10]. For the realization of dynamic range controllers on DSP, a polynomial expression is applied for the power transformation in the proposed methods, by which the efficient

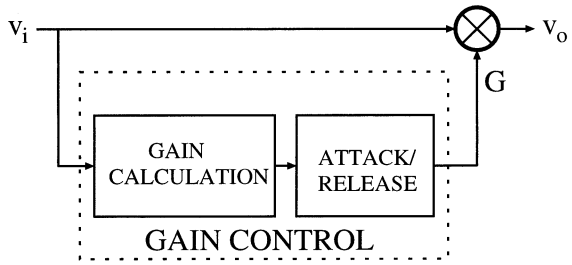

Fig. 1 Dynamic range controller.

implementations on DSP are achieved comparing with another methods [11,12]. For a high performance of digital audio system with low cost, it is necessary to integrate multiple functions including such dynamic range controllers into a VLSI chip to result in a desired audio system on a chip.

In this paper, we present a VLSI architecture of the compressor which is based on the approximation algorithm using a polynomial expression. Thus, the logic circuits in the compressor are easily implemented by using a hardware language, VHDL, to perform the subfunctions for compressing audio signal levels. Based on this method, other dynamic controllers, such as expanders and noise gates, can be also implemented efficiently into a VLSI chip. In the following section we describe the compression characteristics and the attack time and release time control of a compressor. The attack time and release time control circuit is also given, which makes the audio signal smooth and can be also used to produce sound effects. In section 3, a method on the gain calculation using a polynomial expression is derived. Therefore, the gain calculation can be easily implemented with some arithmetic circuits. Based on the gain calculation method, in section 4 the architecture of a compressor including some arithmetic circuits such as adders, multipliers and a divider is proposed. We also give the detail idea on the circuit design by using a hardware description language, VHDL. To evaluate the presented compressor, the VLSI implementation of a 16-bit compressor is proposed and the simulation is performed by using 1 μm CMOS gate array VLSI technology in section 5. By a compact design, the 16-bit compressor can be implemented only with 5,688 gates. The design and simulation results show that the approximation precision to the gain computation of the compressor is determined mainly by the order of the polynomial expression, and by the proposed method, a high performance compressor can be integrated into an audio system on a chip for practical use.

2. CHARACTERISTICS OF COMPRESSOR

2.1. Level Compression Characteristics

The audio signal levels are usually expressed by multiples of the reference voltage and are represented by decibels (dB). For a compressor, the input and output signal levels are denoted as V_i and V_o, respectively, and they have the following relationships:

$$V_i = 20 \log_{10}(A_i), \tag{1}$$

$$A_i = |v_i|, \tag{2}$$

$$V_o = 20 \log_{10}(A_o), \tag{3}$$

$$A_o = |v_o|, \tag{4}$$

where v_i and v_o are the input and output signals as shown in Fig. 1, respectively. A_i and A_o have the values relative to the maximum magnitude of input signal which is the reference value in a digital audio system. Without loss of generality, we can suppose $-\infty \leq V_i, V_o \leq 0$ (dB), then v_i and v_o are real numbers in $[-1,1]$ and A_i, A_o are real numbers in $[0,1]$.

The compression characteristics are defined in Fig. 2, which are measured with the RMS (root mean square) values of the signal's magnitudes. When the audio level V_i of input signal of a compressor is greater than a threshold level V_T, the signal level is compressed with a compression ratio p. That is, if $V_i > V_T$ then $\Delta V_i : \Delta V_o = p : 1$ ($p \geq 1$). When $p = \infty$, the compressor becomes a limiter. The relationship between the input and output levels is represented by the following equation:

$$V_o = \begin{cases} (1/p)(V_i - V_T) + V_T & (V_i > V_T) \\ V_i & (V_i \leq V_T) \end{cases} . \tag{5}$$

2.2. Attack Time and Release Time Control

The attack time and release time control is a very important function to make the dynamic sound effects. In our approach, as shown in Fig. 1, an ATTACK/RELEASE functional block is designed not only to make the sound effects but also to smooth the gain obtained in the GAIN CALCULATION block. The input and output signals and the gain have the following relationship,

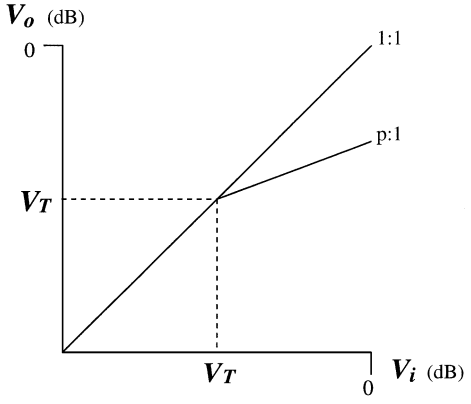

Fig. 2 Compression characteristics.

$$v_o = G \times v_i. \tag{6}$$

Let the input and output of ATTACK/RELEASE block be G_I and G, respectively. G_I is the gain obtained from the GAIN CALCULATION block, where $0 < G_I \leq 1$. The attack time and release time are defined as follows.

Definition Let $G = G_I = G_0$ initially. At the time $t = 0$ G_I changes into a new value ($G_I \neq G_0$), then G is changing from G_0 to G_I by the following equation,

$$G = G_I + (G_0 - G_I) \times \exp(-t/T). \tag{7}$$

When $G_I < G$, $T_a = T$ is defined as the attack time, while $T_r = T$ is the release time when $G_I > G$.

From Eq. (7), we have

$$\Delta G/\Delta G_I = 1 - \exp(-t/T), \tag{8}$$

where $\Delta G = G - G_0$ and $\Delta G_I = G_I - G_0$. Thus, the attack time and release time are the intervals, while the changed value on the output of ATTACK/RELEASE has become 63.2% of that on the input of the ATTACK/RELEASE block. Figure 3 illustrates the operation of the attack time and release time control, and in general, $T_r \gg T_a$.

3. COMPUTATION METHOD OF THE GAIN WITH A POLYNOMIAL EXPRESSION

We begin the computation by considering the compression characteristics with a compression ratio p ($p \geq 1$) as shown in Fig. 1. From Eqs. (1), (3) and (5), we have the following relationship between the input and output signals of the compressor with a compression ratio p:

$$A_o = \begin{cases} {v_t}^{(p-1)/p} \cdot {A_i}^{1/p} & (A_i \geq v_t) \\ A_i & (A_i < v_t) \end{cases}, \tag{9}$$

where v_t is the signal threshold having a positive value with respect to the level threshold V_T satisfying $V_T = 20 \log_{10}(v_t)$. The representation of the gain, G, may be obtained by

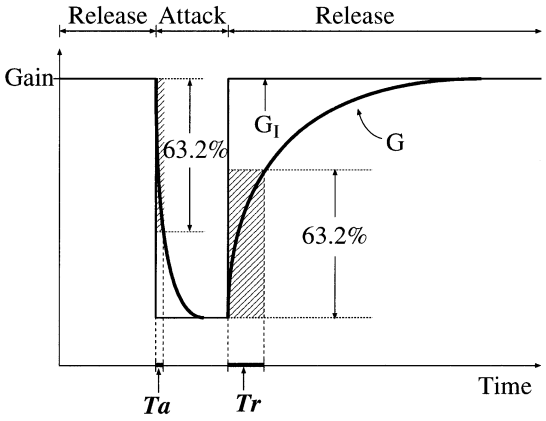

Fig. 3 Attack/release characteristics.

$$G = \begin{cases} (v_t/A_i)^{(p-1)/p} & (A_i \geq v_t) \\ 1 & (A_i < v_t) \end{cases}, \tag{10}$$

$$A_o = G \cdot A_i. \tag{11}$$

Because of the same signs of v_i and v_o, Eq. (6) is a general form of Eq. (11).

It is difficult to obtain the gain by Eq. (10) directly, which has the power calculation with fractional numbers. To simplify the power calculation, a polynomial expression is derived to approximate the compression characteristics [8]. In the case of $A_i \geq v_t$, the gain may be represented by the following equation:

$$G = 1 - (1/A_i) \cdot f, \tag{12}$$

where,

$$f = A_i - {v_t}^{(p-1)/p} \cdot {A_i}^{1/p}. \tag{13}$$

Obviously, $0 \leq f < A_i$ and $0 < G \leq 1$.

Let $\alpha = A_i - v_t$, then Eq. (13) may be expressed by a polynomial of degree m of α to approximate the gain calculation as follows:

$$f_m(\alpha) = b_0 + b_1\alpha + b_2\alpha^2 + \ldots + b_m\alpha^m. \tag{14}$$

Since $f_m(0) = 0$, then $b_0 = 0$. Substituting the polynomial expression and a two-value variable $\delta \in \{0, 1\}$ into Eq. (10),

$$\delta = \begin{cases} 1 & (\alpha > 0) \\ 0 & (\alpha \leq 0) \end{cases}, \tag{15}$$

and let

$$x = \delta \cdot \alpha, \tag{16}$$

then the gain can be expressed as follows:

$$\begin{aligned} G &= 1 - (\delta/A_i) \cdot f_m(\alpha) \\ &= 1 - f_m(x)/A_i. \end{aligned} \tag{17}$$

Thus the power calculation with fractional numbers for getting compression characteristics is equivalent to the calculation of a division and the polynomial expression with parameters $(b_1, b_2, \ldots, b_m)$, which is easily performed by using arithmetic circuits such as adder, multiplier and divider. If the parameters are set to $b_1 = 1$ and $b_i = 0$ $(i = 2, \ldots, m)$, for $\alpha > 0$

$$G = 1 - \alpha/A_i = v_t/A_i$$

and

$$A_o = G \cdot A_i = v_t.$$

Thus a limiter characteristic, $p = \infty$, is obtained. Obviously, the larger the degree of the polynomial expression, m, the closer to the ideal the approximation characteristic is. We have proposed an approximation algorithm based on the least squares method to obtain the parameters

$(b_1, b_2, \ldots, b_m)$ for a given compression characteristics [8], and attach the approximation algorithm in the appendix.

4. VLSI IMPLEMENTATION OF COMPRESSOR

4.1. Architecture of Compressor

In this paper, we suppose that the input and output audio signals are represented in a fixed-point binary number representation, called the two's complement representation, as follows,

$$x = x_0.\, x_1 x_2 \cdots x_{n-1}, \tag{18}$$

where $x_i \in \{0, 1\}$ for $i = 0, 1, 2, \cdots, n-1$, and x_0 expresses the sign of x. The value of x is obtained by using the following equation,

$$x = -x_0 + \sum_{i=1}^{n-1} x_i 2^{-i}. \tag{19}$$

Obviously, x has a value range of $[-1, 1)$. This number representation is also applied to each arithmetic circuit in the proposed compressor.

Figure 4 shows a pipeline-type architecture for the compressor implementation to perform the functional operations described in the above sections. In these arithmetic circuits, all signals are represented in n-bit binary number representations by Eq. (18). The circuit ABS performs the calculation of the absolute value on the input signal v_i shown in Eq. (2). Then the difference of A_i and v_t, $\alpha = A_i - v_t$, is calculated by inputting $-v_t$ to an adder, ADD. The comparator CMP performs Eqs. (15) and (16), and when $\alpha < 0$, $x = 0$. In the circuit $F_m(x)$, a degree m polynomial expression of Eq. (14) is computed. The result of the computation of the polynomial expression is kept in a pipeline register REG-P to shorten the execution time. Figures 5 and 6 show the block diagrams with the

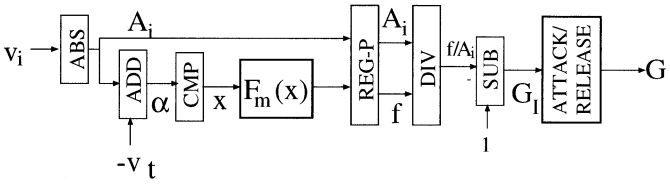

Fig. 4 Architecture of compressor.

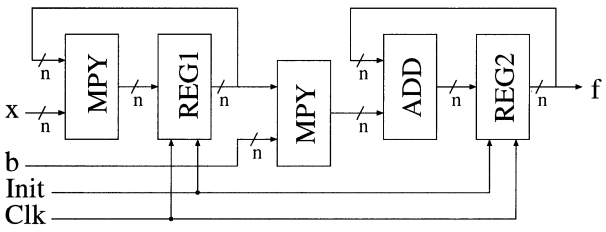

Fig. 5 Arithmetic circuit for computing a polynomial expression.

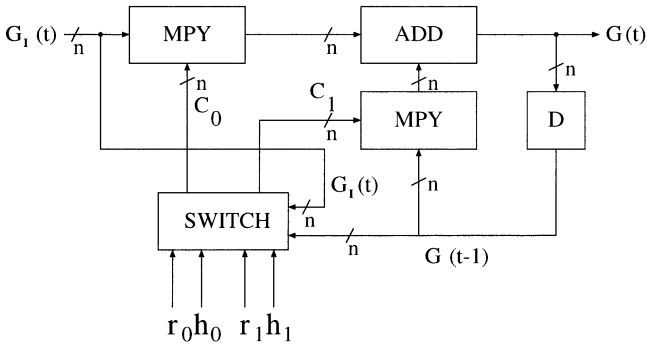

Fig. 6 Attack/release circuit.

Table 1 Calculation of a polynomial of degree three.

i	0	1	2	3	4
x	x	x	x	0	0
REG1	1	x	x^2	x^3	0
b	0	b_1	b_2	b_3	0
REG2	0	0	$b_1 x$	$b_1 x + b_2 x^2$	$\sum_{i=1}^{3} b_i x^i$

arithmetic circuits for the polynomial expression and the attack time and release time control, respectively. As shown in Table 1, the computation of a polynomial expression is started at the time $i = 0$, and registers REG1 and REG2 are initially set to 1 and 0, respectively. Then the parameters $(0, b_1, b_2, \cdots, b_m)$ are inputted sequentially, and the following calculations with multiplications and addition are executed repeatedly,

$$Reg1(i) = Reg1(i-1) \cdot x, \tag{20}$$

$$Reg2(i) = Reg2(i-1) + b_i \cdot Reg1(i-1), \tag{21}$$

where $Reg1(i)$ and $Reg2(i)$ denote the data stored in REG1 and REG2 at the time i, respectively. Table 1 shows the computing scheme of a polynomial expression and the circuit is constructed with two multipliers, an adder and two registers.

The attack/release circuit performs the function of Eq. (7). The circuit SWITCH switches parameters (C_0, C_1), by comparing $G(t-1)$ with $G_I(t)$, between (h_0, h_1) for the attack time control and (r_0, r_1) for the release time control, respectively.

$$(C_0, C_1) = \begin{cases} (h_0, h_1) & (G_I(t) > G(t-1)) \\ (r_0, r_1) & (G_I(t) \le G(t-1)) \end{cases}, \tag{22}$$

where t denotes a sampling time. The parameters, (h_0, h_1) and (r_0, r_1), are obtained by the following equations.

$$h_1 = \exp(-1/(f_s \cdot T_a + 1)), \tag{23}$$

$$h_0 = 1 - h_1, \tag{24}$$

$$r_1 = \exp(-1/(f_s \cdot T_r + 1)), \tag{25}$$

$$r_0 = 1 - r_1, \tag{26}$$

where f_s is the sampling frequency of a digital audio system. In the circuit, there are two multipliers, one adder and a latch D.

4.2. Circuit Design

One aim of the circuit design is to implement each functional circuit in the compressor with less hardware and a small delay time. For the purpose, we use VHDL, which covers several levels of abstraction in the behavioral and the structural domain of description [13,14], to design the circuits of the presented compressor. The arithmetic circuits such as an adder and a multiplier are described easily and implemented with compact design by a VHDL-based design tool, and a VHDL-based simulator is used to confirm the performance of the design results.

To simplify the circuit ABS, we apply the one's complement representation to the circuit instead of the two's complement representation to obtain the absolute value of a negative number. Thus, the logic circuit is only implemented with $n-1$ EXCLUSIVE-OR gates performing the following operations in parallel:

$$A_{i0} = 0, \tag{27}$$

$$A_{ij} = v_{i0} \oplus v_{ij}, \quad \text{for} \quad j = 1, 2, \cdots, n-1 \tag{28}$$

where v_{ij} and A_{ij} denote jth bit of v_i and A_i using the number representation as shown in Eq. (18), respectively. In this case, the calculation error for a negative number is $2^{-(n-1)}$, which can be ignored by selecting a suitable wordlength.

An n-bit adder is used to calculate $\alpha = A_i + (-v_t)$, where $-v_t$ is in the two's complement representation. In the circuit CMP, there are $n-1$ two-input AND gates performing the following operations:

$$x_0 = 0, \tag{29}$$

$$x_j = \overline{\alpha_0} \wedge \alpha_j, \quad \text{for} \quad j = 1, \cdots, n-1, \tag{30}$$

where $\alpha = \alpha_0 \cdot \alpha_1 \alpha_2 \cdots \alpha_{n-1}$. The divider, multiplier and adder in the circuits $F_m(x)$ and ATTACK/RELEASE are normal arithmetic circuits with combinational logic gates and all of them have two 16-bit length inputs and one 16-bit length output. To calculate $G_I = 1 - f/A_i$, we use $(0.11\cdots11)$ to represent the closest value to 1. Therefore, let f_A denote f/A_i, and since f_A and G_I are two n-bit numbers, the subtraction circuit is simply implemented by using $n-1$ NOT gates performing the following operations:

$$G_{I0} = 0, \tag{31}$$

$$G_{Ij} = \overline{f_{Aj}}, \quad \text{for} \quad j = 1, 2, \cdots, n-1. \tag{32}$$

We use the round-to-nearest method to result in the 16-bit output of a multiplier and a divider.

5. PERFORMANCE EVALUATION

To evaluate the performance of a compressor based on the implementation methodologies described above, we designed a 16-bit compressor by VHDL coding and used a VHDL-based simulator to simulate the compression characteristics and the attack time and release time control operations. The input and output audio signals, v_i and v_o shown in Fig. 1, may have more longer wordlength such as 24-bit. However, the most significant 16 bits of the input signal can be used to calculate the gain, by which the output signal with the whole wordlength is controlled. In our approach, at first, we encode each circuit with VHDL and make the logic functional tests. Then the compressor is constructed by combining the functional circuits and the simulation for the whole compressor circuit is performed again. Figure 7 shows the compression characteristics by using a polynomial expressions of degree three, in which the threshold level is set to -40 dB and the compression ratios are set to 1, 1.4, 2, 4, 6, 10, respectively. These characteristics have the errors within 0.8 dB compared with the ideal. The approximation error by the polynomial expressions of degree three results in the undulated characteristic curves for the larger compression ratios and for the larger compression range, for example, when the threshold level V_T is -50 dB. Thus, to get the better characteristic for a larger compression range, polynomial expressions with a higher degree have to be used to make the small approximation error.

In general, the sampling frequency used in an audio system is around 48 kHz. Figure 8 illustrates the simulation results on the attack time and release time control under the following conditions, i.e. $f_s = 48$ kHz, $T_a = 1$ ms, $T_r = 200$ ms, $V_T = -40$ dB and $p = 10$, which were used to calculate the paramenters (h_0, h_1) and (r_0, r_1) by Eqs. (23)–(26). The input audio level is changed from $-\infty$ dB to -20 dB at the time 0.5 s, then back to $-\infty$ dB at the time 1 s. The above simulation results show that the presented compressor makes the high quality of the characteristics for the compression and the attack time and release time control.

The whole circuit of the compressor has been synthesized by using a VHDL-based design tool under the condition of 1 μm CMOS gate array technology. There are 15,418 gates in the 16-bit compressor. The longest delay path, which results in the rate of the sampling frequency of a compressor, is arisen from the divider, when a polynomial expression of degree three is used. However, when the higher degree polynomial expression is used, the computation time for the polynomial expression is longer than that of the division. Figure 9 shows the relationship between the maximum sampling frequency and the degree

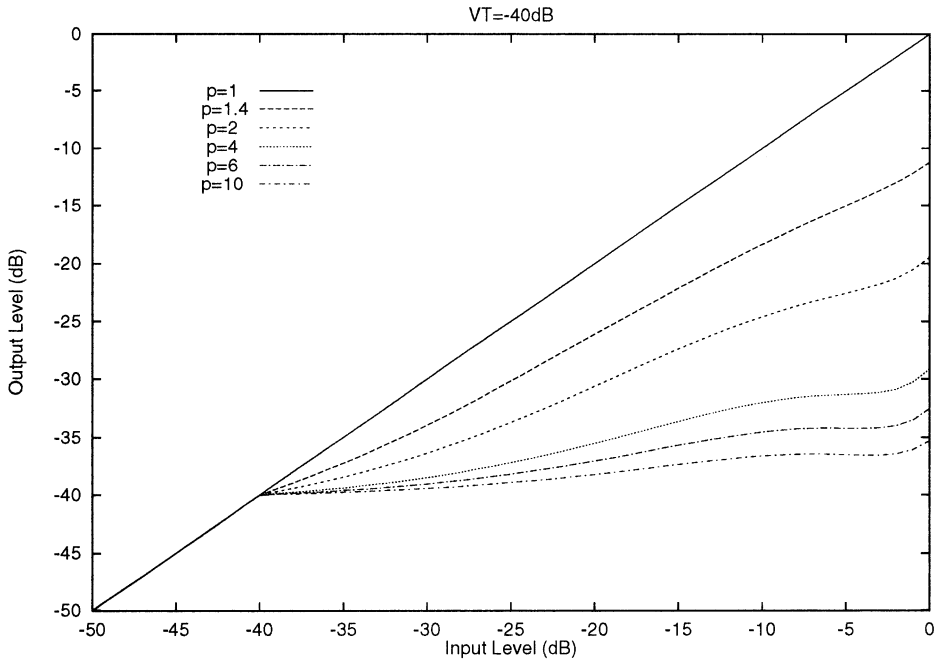

Fig. 7 The compression characteristics obtained by VHDL simulation.

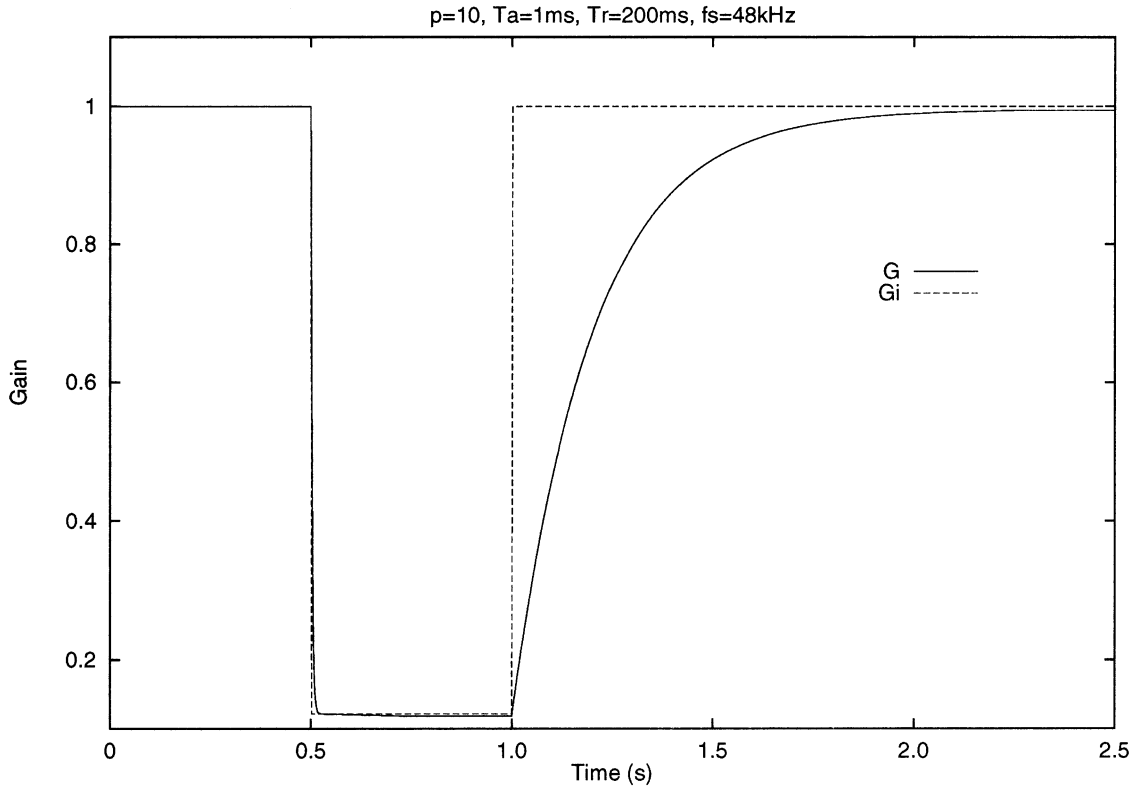

Fig. 8 A simulation result for the attack/release time control.

of the polynomial expression.

In the above implementation, about 80% of gates are dominated by multiplier and divider circuits. Thus, to implement a compact compressor circuit, we have also designed the sequential multiplier and divider by using addition circuits and shift registers. In this case, the number of gates is reduced to 5,688 and the compressor can work in a sampling frequency with 60 kHz, which is enough for the current audio systems.

6. CONCLUSION

A VLSI implementation method of a dynamic range

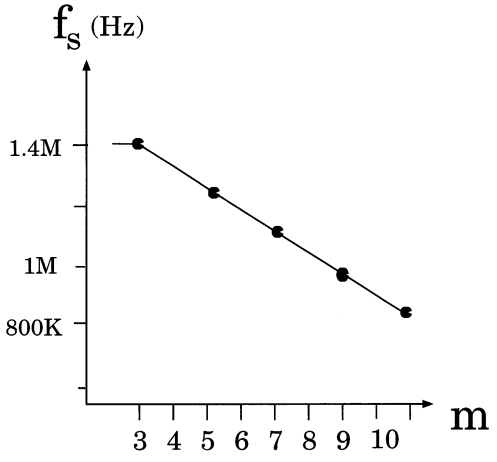

Fig. 9 The maximum sampling frequency with a polynomial of degree m.

controller, compressor, has been presented. By using a polynomial expression, the power transformation for getting the compression characteristics is converted into the calculations of additions and multiplications, which could be easily implemented by arithmetic circuits. An pipeline-type architecture of the compressor and the corresponding functional circuits have been proposed.

To evaluate the performance of a compressor based on the presented implementation method, a 16-bit compressor has been designed and simulated by using a hardware description language, VHDL. The design and simulation results show that the ideal input-output characteristics can be achieved by using a polynomial expression of degree three or a higher degree one, and there are about 5,688 gates in a compressor with the sequential multiplier and divider circuits. The implemented compressor can be integrated into an audio system on a chip for practical use.

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APPENDIX: APPROXIMATION ALGORITHM TO OBTAIN COMPRESSION CHARACTERISTICS

Input: An ideal compression characteristic curve with a threshold level V_T, a compression ratio p ($p \geq 1$) and the order m polynomial expression, $f = b_1\alpha + b_2\alpha^2 + \cdots + b_m\alpha^m$.

Output: $b_1, b_2, \ldots, b_m$.

1) For the ideal compression characteristic curve, we sample V_i on $[V_T, 0]$ with the same interval as $(V_{i1} = V_T, V_{i2}, \ldots, V_{ik} = 0)$, then calculate the corresponding output level data, $(V_{o1}, V_{o2}, \ldots, V_{ok})$ from the compression characteristics. Then by Eqs. (1) and (3), calculate $(A_{i1} = v_t, A_{o2}, \ldots, A_{ok} = 1)$ and $(A_{o1}, A_{o2}, \ldots, A_{ok})$, which is regarded as the target data to be approximated.

2) Determine the approximation error, ε_0. Give the initial values to the coefficients of the m-order polynomial expression:

$$(b_1, b_2, \ldots, b_m) = (b_{10}, b_{20}, \ldots, b_{m0}).$$

3) Let the gain of the compressor be G represented by the m-order polynomial expression, $G = 1 - (1/A_i)f$. Thus, calculate $(A_{om1}, A_{om2}, \ldots, A_{omk})$ by

$$\begin{aligned}(A_{om1}, A_{om2}, \ldots, A_{omk}) &= G \cdot (A_{i1}, A_{i2}, \ldots, A_{ik}) \\ &= (G \cdot A_{i1}, G \cdot A_{i2}, \ldots, G \cdot A_{ik}).\end{aligned}$$

4) Based on the least squares method, calculate the approximation error, as follows:

$$\sigma_j = A_{omj} - A_{oj}, \quad (j = 1, 2, \ldots, k)$$

$$\varepsilon = \sum_{j=1}^{k} {\sigma_j}^2.$$

If $\varepsilon > \varepsilon_0$, then go to 5).
If $\varepsilon \leq \varepsilon_0$, then output the parameters, $b_1, b_2, \ldots, b_m$ and stop.

5) Calculate the partial derivatives of Eq. (11) with respect to the variables, $b_1, b_2, \ldots, b_m$, respectively:

$$w_i = \frac{\delta A_{om}}{\delta b_i} = -\frac{\delta f}{\delta b_i} = -\alpha^i. \quad (i = 1, 2, \ldots, m)$$

where $\alpha = A_i - v_t$.

6) Let the value of w_i for A_{omj} be w_{ij} $(j = 1, 2, \ldots, k)$, then calculate the deviation value of b_i, Δb_i $(i = 1, 2, \ldots, m)$, by the following equation:

$$\Delta b_i = \sum_{j=1}^{k} (\sigma_j \cdot w_{ij}) / \sum_{j=1}^{k} (w_{ij})^2.$$

7) Let $b_i + \Delta b_i$ be the new value of b_i $(i = 1, 2, \ldots, m)$, go to 3).

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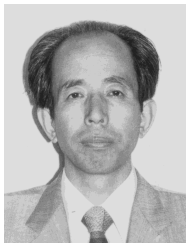

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