

Design of Low Power CMOS Circuits using Leakage Control Transistor and Multi-Threshold CMOS Techniques

U. Supriya^{#1}, K. Ramana Rao^{#2}

[#]Dept. of ECE, Pydah College of Engineering and Technology, Andhra Pradesh, India

¹supriya.undavalli@gmail.com

²ramanadeepu@yahoo.co.in

Abstract

The scaling down of technology in CMOS circuits, results in the down scaling of threshold voltage thereby increasing the sub-threshold leakage current. An IC consists of many circuits of which some circuits consist critical path like full adder, whereas some circuits like multiplexer and decoder has no specified critical path. LECTOR is a technique for designing leakage power reduced CMOS circuits without affecting the dynamic power dissipation, which can be used for circuits with no specified critical paths. MTCMOS, an efficient technique to achieve low power as well as high speed, is used for the circuits which have critical path. This paper presents the analysis for leakage current and propagation delay in CMOS circuits implementing LECTOR and MTCMOS techniques using nanoscale technologies.

1. Introduction

Since the invention of the first Integrated Circuit (IC), silicon technology scaling down continues to meet the increasing demands for higher functionality and better performance at a lower cost. Power dissipation, though not entirely ignored, has been of little concern until recently. The advances in VLSI integration technology have made it possible to put a complete System on a Chip (SoC) which facilitates the development of portable systems. Portable battery powered applications such as notebook computers, cellular phones, Personal Digital Assistants (PDAs), and military equipments profile power dissipation as a critical parameter in digital VLSI design.

With the increasing prominence of portable systems, it is important to prolong the battery life as much as possible, since it is the limited battery lifetime that typically imposes strict demands on the overall power consumption of such systems. Although the battery industry has been making efforts to develop batteries with a higher energy capacity than that of conventional Nickel-Cadmium (NiCd) batteries, a revolutionary increase of the

energy capacity does not seem imminent. Therefore, portable applications have led to rapid and innovative developments in low-power circuit designs.

Power dissipation is also crucial for Deep Sub-Micron (DSM) technologies. To further improve the performance of the circuits and to integrate more functions on a chip, the feature size has to continue to shrink. As a result, the power dissipation per unit area grows, increasing the chip temperature. Although power dissipation is important for modern VLSI design, performance (speed) and area are still the main requirements of a design. However, low-power design usually involves making tradeoffs such as timing versus power and area versus power. Increasing performance, while the power dissipation is kept constant, is also considered to be a low-power design problem.

2. Related work

Many techniques have been come into existence to overcome the leakage power problem in the nanoscale technology, but those techniques have trade off between area, delay and also active power. Some of those techniques are as described in this section.

2.1 Sleep transistor technique

This is one of the techniques proposed for leakage reduction, which turns off the device by cutting OFF the supply voltage. Bulky NMOS and/or PMOS device called sleep transistor is used in a path between supply voltage and ground, creating virtual power and ground rails in the circuit [5]. This creates a negative effect on the switching speed of the circuit when the circuit is operating in active mode. Additional hardware is needed to identify the idle regions of the circuit and the generation of the sleep signal. Even when the circuit is in an idle state, this additional hardware

consumes power throughout the circuit operation to control the sleep transistors and continuously monitor the circuit state.

2.2 Forced stack technique

Forced stacking introduces an additional transistor for every input of the gate in both N-network and P-network. This ensures that two transistors are OFF instead of one for every OFF-input of the gate and hence makes a significant savings on the leakage current [6]. However, the loading requirement for each input introduced by the forced stacking reduces the drive current of the gate significantly. This results in a detrimental impact on the speed of the circuit.

2.3 Sleepy stack technique

The sleepy stack technique has a merging structure of both the forced stack technique and the sleep transistor technique. In this technique, each transistor is replaced with two half sized transistors and one extra sleep transistor [8]. The leakage reduction of the sleepy stack structure occurs in two ways. One is the leakage power is suppressed by high- V_{th} transistors and the other is two stacked and turned off transistors induce the stack effect. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. The price for this is drastically increased area. And the main disadvantage of having controlling circuitry for sleep transistors is also carried here. As the sleep transistors are bulky, the dynamic power.

2.4 Sleepy keeper technique

Sleepy Keeper, a better leakage reduction technique compared to sleepy stack in terms of reducing the area overhead since it does not need one transistor to be replaced with three transistors. Sleep transistors are connected to the circuit along with NMOS connected to V_{dd} and PMOS connected to Gnd [7]. This arrangement creates virtual power and ground rails in the circuit, causing detrimental effect on the switching speed in active mode. The identification of the idle regions of the circuit and the generation of the sleep signal needs an additional hardware capable of predicting the circuit states, leads to area overhead. The limitation in the sleep technique comes here due to the additional hardware.

3. LECTOR and MTCMOS techniques

An IC consists of many circuits of which some circuits have critical path, whereas some circuits have no specified critical path. LECTOR technique is used to design circuits with no critical path and MTCMOS technique is used to design circuits with critical paths.

3.1 LECTOR technique and its applications

The Leakage Control Transistor (LECTOR) technique is based on the effective stacking of transistors in the path from supply voltage to ground. The idea behind this technique from [1], [2] and [3] is that “a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path.” In this method, for each CMOS gate, two leakage control transistors (LCTs) were introduced, a PMOS added to the pull-up network and a NMOS added to the pull-down network. The gate terminal of each LCT is controlled by the source of the other, such that one of the LCTs is always near its cutoff region of operation. Because of this arrangement, additional resistance is provided in the path, decreasing the sub-threshold leakage current. This paper illustrates LECTOR technique with the case of CMOS logic circuit, viz., Decoder.

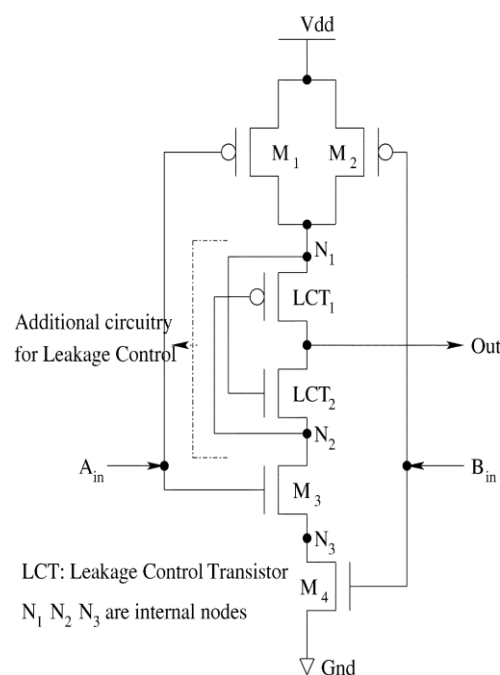


Figure 1. LECTOR based NAND Gate

A LECTOR NAND gate is shown in Figure 1. Two leakage control transistors LCT1 (PMOS) and LCT2 (NMOS) are introduced at the nodes N1 and N2 respectively of the pull-up and pull-down logic of the NAND gate. The source nodes of the transistors are connected to nodes N1 and N2 of pull-up and pull-down logic, respectively. The voltage potentials at nodes N2 and N1 controls the switching of transistors LCT1 and LCT2 respectively. This wiring configuration ensures that one of the LCTs is always *near its cutoff region*, irrespective of the input vector applied to the NAND gate.

Table 1. LCT NAND State matrix

Transistor Reference	Input Vector – (A_{in} , B_{in})			
	(0,0)	(0,1)	(1,0)	(1,1)
M1	On state	On state	Off state	Off state
M2	On state	Off state	On state	Off state
LCT1	Near Cut-Off state	Near Cut-Off state	Near Cut-Off state	On state
LCT2	On state	On state	On state	Near Cut-Off state
M3	Off state	Off state	On state	On state
M4	Off state	On state	Off state	On state

Providing a supply voltage of 1V, When $A_{in} = 1$ and $B_{in} = 0$, the voltage at the node N2 is 800 mV. This voltage is not sufficient to turn LCT1 completely to OFF state. Hence, the resistance of LCT1 will be lesser than its OFF resistance, allowing conduction [4]. Even though the resistance of LCT1 is not as high as its OFF state resistance, it increases the resistance of supply to ground path, controlling the flow of leakage currents, resulting in leakage power reduction.

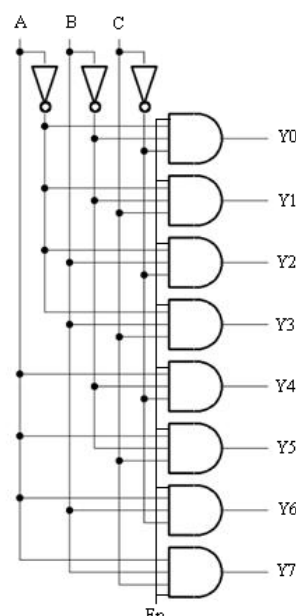


Figure 2. Gate level schematic of 3 to 8 decoder

Similarly, when $A_{in} = 1V$ and $B_{in} = 1V$, the voltage of node N1 is 200 mV, operating the transistor LCT2 near its *cutoff region*. For all the combination of inputs of NAND, the states of transistor are shown in Table 1.

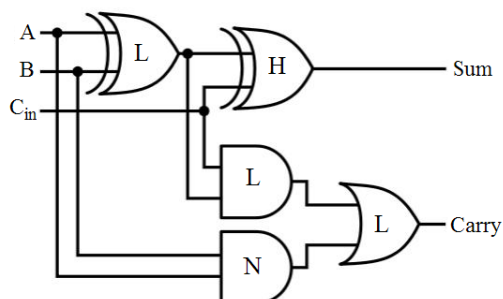
The gate level schematic of a 3 to 8 Decoder is shown in Figure 2. Two LCTs were added to each gate for the LECTOR decoder implementation.

3.2 MTCMOS Technique

The low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. This technique uses low, normal and high threshold voltage transistors in designing a CMOS circuit.

The low-threshold voltage transistors which have high performance are used to reduce the propagation delay time in the critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path [9], [10]. Since no additional circuitry is added to the design, there is no area overhead in this technique.

This paper describes a low power and high speed design for 1-bit full adder cell. The logic diagram of full adder is shown in figure 3.



L - Low Vt N - Normal Vt H - High Vt

Figure 3. Logic diagram of full adder using MTCMOS

It can be observed from the logic diagram of full adder that the carry path is the critical path or the longest path and sum path is the shortest path in the circuit. Since carry path is the critical path, low-Vth transistors are used in this path to reduce the propagation delay time. High-Vth transistors are used in the shortest path to reduce the static power dissipation of the circuit. The remaining AND gate is designed with normal threshold transistors.

4. Experimental Results

The HSPICE tool of Synopsys is used to calculate the leakage power. Leakage power dissipation is taken as the average of power dissipations obtained at all the possible input vectors of the CMOS circuit. For 3 to 8 decoder, the average of 8 power dissipations is considered to be as the static power dissipated. In this case, the leakage power is measured by exciting both the circuits (Conventional and LECTOR) with same set of input vectors. The result for the decoder is shown in Table 2.

Table 2. Results for 3 to 8 Decoder using 90nm technology

		3 to 8 Decoder
Leakage Power(nW)	CONVENTIONAL	49.344
	LECTOR	27.608
Percentage decrease in Power Dissipation		44.05

The full adder circuit is designed using MTCMOS technique to achieve low power and high speed design requirements. Since there are 8 different input combinations for a 1-bit full adder circuit, the average of 8 power dissipations is considered in calculating the static power dissipation. To calculate the propagation delay of

the circuit, the time taken for the Carry to change its state for the corresponding input change is calculated.

The full adder circuit is designed both conventionally and using MTCMOS technique for 90nm technology and the results are shown in the Table 3.

Table 3. Results For Full Adder Using Mtcmos For 90nm Technology

	Conventional circuit	MT-CMOS	% reduction
Static power (Watts)	4.24E-8	3.35E-8	20.99%
Delay in critical path(Sec)	1.21E-10	1.15E-10	4.95%

5. Conclusions

An IC consists of many circuits of which some circuits have critical path, whereas some circuits have no specified critical path. LECTOR technique is used to design circuits with no critical path and MTCMOS technique is used to design circuits with critical paths. When applied to generic logic circuits, the LECTOR technique achieves up to 40-45% leakage reduction over the conventional circuits without affecting the dynamic power. The proposed full adder circuit designed with MTCMOS technique achieved 20.99% power reduction and 4.95% delay reduction without any area overhead for 90nm technology.

REFERENCES

- [1] P. Verma, R. A. Mishra, "Leakage power and delay analysis of LECTOR based CMOS circuits", *Int'l conf. on computer & communication technology ICCCT* 2011.
- [2] H. Narender and R. Nagarajan, "LECTOR: A technique for leakage reduction in CMOS circuits", *IEEE trans. on VLSI systems*, vol. 12, no. 2, Feb. 2004.
- [3] B. Dilip and P. Surya Prasad, "Design of Leakage Power Reduced Static RAM using LECTOR", *International Journal of Computer Science and Information Technologies, IJCSIT*, vol. 3 (3), 2012.
- [4] John F. Wakerly, "Digital Design- Principles and Practices", fourth edition.
- [5] M. D. Powell, S. H. Yang, B. Falsafi, K. Roy, and T. N. Vijaykumar, "Gated-Vdd: A circuit technique to reduce leakage in deep submicron cache memories," in *Proc. IEEE ISLPED*, 2000, pp. 90-95.

- [6] S. Narendra, S. Borkar, V. De, D. Antoniadis, and A. P. Chandrakasan, "Scaling of stack effect and its application for leakage reduction," *Proc. IEEE ISLPLED*, pp. 195–200, Aug. 2001.
- [7] S. H. Kim and V. J. Mooney, "Sleepy Keeper: a new approach to low-leakage power VLSI design," *IFIP*, pp. 367-372, 2006.
- [8] J. C. Park, "Sleepy Stack: A new approach to Low Power VLSI logic and memory," Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2005.
- [9] Phanikumar M and N. Shanmukha Rao, "A Low Power and High Speed Design for VLSI Logic Circuits Using Multi-Threshold Voltage CMOS Technology", *International Journal of Computer Science and Information Technologies (IJCSIT)*, Vol. 3(3), 2012, 4131-4133
- [10] Dong Whee Kim, Jeong Beom Kee, "Low-Power Carry Look-Ahead Adder With Multi-Threshold Voltage CMOS Technology", in *Proceeding of ICSICT International Conference on Solid-State and Integrated-Circuit Technology*, pp. 2160-2163, 2008.