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Low Power Analysis of Network-Level On-chip communication using Asynchronous AMBA protocol

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ABSTRACT:

Network on-chip (NoC) is a novel structural design template, which can be defied for complicated system level on-chip design. NoC has a potential to limit and present the bus-based communication. In this paper, the crisis to discuss is Low power consumption in an Asynchronous Network on-chip (NoC) level communication. NoC is implemented using FPGA which has less fabrication cost and reduces the complexity. An Asynchronous NoC has been implemented in Spartan kit using Xilinx FPGA ISE tools and its network interface is Advanced Microcontroller Bus Architecture (AMBA) which features numerous bus masters and a sole clock edge evolution and so on. Here the AMBA high performance 32-bit AHB bus is employed in which it has a high clock frequency system and it is the heart of our bus system. To accomplish low power consumption by interfacing SoC with AMBA- AHB protocol. The AHB model and an Asynchronous NoC are employed and executed using VHDL programming module.

I) INTRODUCTION:

In modern technology with the high complexity in VLSI design like System level on-chip which has a resolution problem and the number of masters is trying to reach a single data bus and interconnect issues are faced during SoC designs, but to conquer this kind of issues Asynchronous NoC architecture was proposed it creates communication architecture with System on-chip [1]. In General NoC architecture outlines about the communication infrastructure, network services and the reserves to network interface and it also monitors the power consumption and utilizes the resources [2]. It providers higher over-all bandwidth and more scalability with less power consumption [3]. To achieve lower power consumption and high operating speed designers prefer asynchronous circuit than synchronous one[4]. It can also be implemented in FPGA by using AMBA protocol as a network interface [5]. The following are the general properties of NoC, It has a higher Bandwidth, reliable and predictable.

Here the reusable components like buffers, arbiter, router, protocol stacks and so on. Typically FPGA devices are designed in synchronous digital designs. In this paper, it is designed to work in Asynchronous mode [6] and it can be implemented using Spartan kit by using Xilinx FPGA ISE software tool and it is programmed using VHDL. The paper is based on the High performance 32-bit AHB bus as a network interface and the memory as a master [7], VGA controller as a slave and interface this two using AMBA-AHB bus protocol [8]. The following section explains about the Review of state of the Art of Network On-chip and their processing elements, network interface and router concepts and so on. The next section is about Asynchronous and synchronous NoC, The proposed work of Asynchronous AMBA-AHB Bus and Simulation Results and its comparison. The last section is about Experimental results and verification and Conclusion.

II) REVIEW THE STATE OF ART OF NETWORK ON-CHIP:

A single node in system or network on-chip consist of three nodes i.e., A) Processing element, B) Network Interface, C) Router.

A) PROCESSING ELEMENT:

An emerging and a novel trend design pattern of processing element in NoC and using this communication network we can transmit the data and signal between the processing elements. In general, processing elements have different kinds of processor, memory cells or Cores. The data transmission occurs between the processing elements (PE) is accomplished by the router and its performance determines the competence of Network on-Chip [9]. Here the device is targeted by the Xilinx product particularly Spartan 3 and 3e families. The Network topology going to use is Mesh topology to design an Asynchronous NoC router using this mesh analysis. For regular structure, simplicity and planar geometry, the designers go with mesh topology.

B) NETWORK INTERFACE:

In general, Network Interface provides a customary interface for effortless integration of new processing elements in Network on-chip. It connect all the IP cores to the network, mapping the bus type transitions coming from the IPs into packets that can be publicized inside the Network on chip and, on the opposite side, building the bus transactions that correspond to packets that need to exit the NoC[10]. Then it decouples the communication element and computation element of the system and each part of design is consummated separately [11]. In this paper, the design is based on Network Interface for the Asynchronous AMBA system. Typically Advanced Microcontroller Bus Architecture (AMBA) determines the on-chip communication for manipulating high performance embedded controller. It has different categories 1) The Advanced High-performance Bus (AHB), 2) The Advanced System Bus, 3) The Advanced Peripheral Bus. From this we execute the concept using AHB it features has a high clock frequency system and it can act as a backbone of the system bus. It supports both On-chip and Off-chip external memories and I/O processor.

C) ASYNCHRONOUS AND SYNCHRONOUS NoC:

It is quite difficult to compare both Asynchronous and synchronous circuit and it is difficult to isolate the timing style, circuit style, technology and their architecture[12]. It is complicated to reproduce and simulate the asynchronous designs from the proposed work and it often lacks data path delays and detailed control. Typically synchronous designs have lots of pros like predictability, Determinism can be exploited and single cycle router is faster possible. Here for Low power analysis designers prefer Asynchronous design the major factor is reduces the power consumption but it requires more space for implementation when compare with the synchronous design[13]. Here the designer uses Asynchronous based AMBA-AHB system it has 32 –bit bus architecture and separate the READ and WRITE data bus features of the AMBA –AHB bus architecture is i) It has a multiple bus masters, ii) Pipelining operation, iii) Split transaction, iv) Burst and line transfer.

III) **PROPOSED WORK OF ASYNCHRONOUS AMBA-AHB BUS:**

In this paper, the design architecture of Network on-chip using AMBA-AHB based network interface in an Asynchronous mode. In existing work, they can design a NoC architecture using different protocols like wishbone, OCP etc in a synchronous design to achieve low power consumption. But here the proposed is to design a network on-chip communication using AMBA protocol in an Asynchronous mode to achieve better performance in low power analysis.

IV) **SIMULATION RESULTS AND RESULT COMPARISON:**

In this Asynchronous NoC design, NoC can be adopted to support communication among the multiple IP's over the multi-processor system on-chip (SOC's). In this paper, the simulation based analysis of some architecture for NoC like mesh topology under some load assumption in SOC. The main advantage of NoC is throughput and latency; here the mesh topology is better trade-off performance, scalability of most efficient architecture, small energy requirement and simple management constraints etc for SOC's. Here the simulation takes place in both hardware and software platform and the results have been analyzed in both platforms. For software simulation Xilinx ISE FPGA tool is implemented and interface with the hardware like Spartan 3e FPGA kit. The following table is the power analysis reporting table for different FPGA Family,

Family	Device	GClk	F.F	I/O's	Slices	Slice F.F	I/O Bonds
Spartan							
3	3s200-5-tq144	62%	166	251	5%	3%	69%
3A	3s50a-5-tq144	20%	166	251	14%	12%	62%
3E	3s100e-5-tq144	20%	166	251	10%	9%	62%
6	6slx100t-3- fgg484	22%	136	251	0%	43%	22%
Virtex							
5	5vlx50-3-ff676	--	166	251	0%	52%	15%
6	6vlx75t-3-ff484	--	136	251	0%	54%	27%

TABLE: 1A. POWER ANALYSIS TABLE FOR DIFFERENT XILINX FAMILY

V) EXPERIMENTAL RESULTS AND VERIFICATION:

The performance of AMBA AHB, AMBA AXI and STBus within the framework. Traffic workload and pattern can easily be tuned by running different benchmark code on the cores, by scaling the number of system processors, or by changing the amount of processor cache, which leads to different amounts of cache refills. For the simulations in this paper

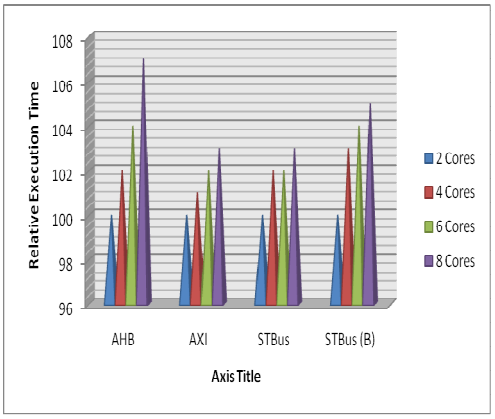

Fig 2. Execution times with 1kB caches.

the assumption of slave devices to introduce one wait state before responses. The AMBA AHB and AMBA AXI modeling was based upon SystemC libraries provided within the Synopsys Co Centric /Design ware R ([21]) suites, while the STBus model was provided by STMicroelectronics. For the STBus model, we also tested a configurable parameter, which is the depth of FIFOs instantiated by the target side of the interconnect; their impact can be noticed on concept waveforms in Fig. 1. We benchmarked with 1-stage ("STBus" in captions) and 4-stage ("STBus (B)") FIFOs. The whole system was simulated with cycle accuracy. To assess interconnect scalability, we chose to independently but concurrently run on every system processor a benchmark which performs accesses towards a single and private slave. This means that, while producing real functional traffic patterns, the test setup was not constrained by bottlenecks due to shared slave devices. Scalability results are shown in Fig. 2 and Fig. 3 in terms of execution time variation when attaching an increasing amount of system cores to a single shared interconnect. Fig. 2 reports figures for a system with 1 kB caches.

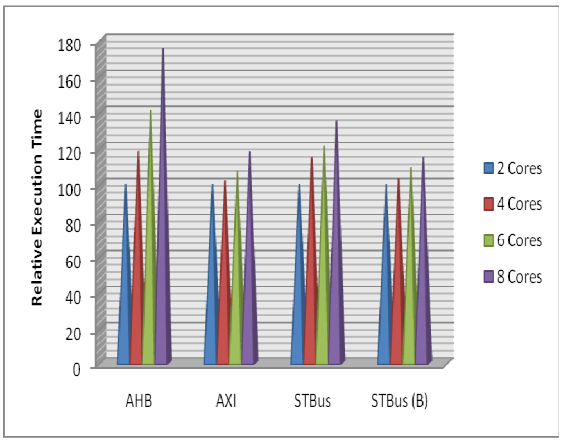

Fig 2. Execution times with 256B caches

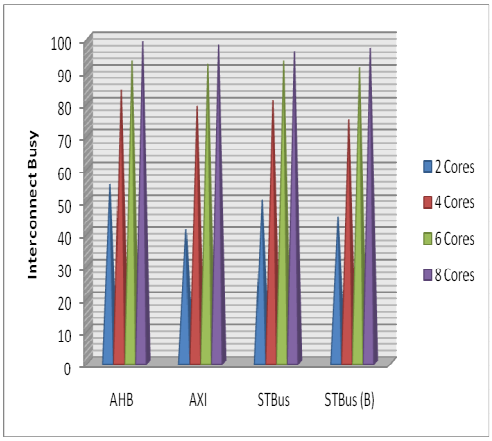

Fig 3. Bus busy time with 256B caches.

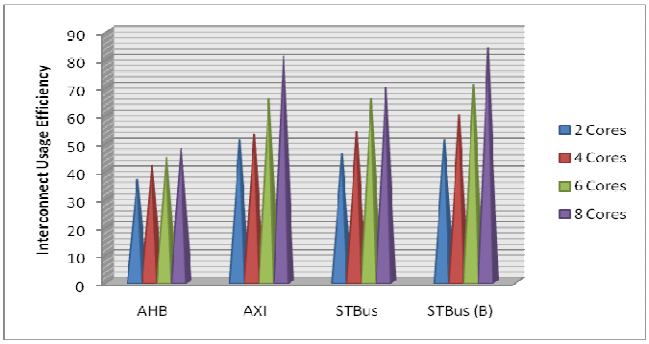

Fig 4. Execution times with 256B caches

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while in Fig. 3 caches were reduced to 256 bytes, thus causing many more cache misses and greater interconnect congestion. Execution times are normalized against those for a two-processor system, trying to isolate the scalability factor alone. Simulations show that, as long as traffic is relatively light (1 kB caches), all of the interconnects perform very well, with only AHB showing a moderate performance decrease of 6% moving from two to eight running processors. With 256 B caches and many processors, interconnect saturation took place, as can be seen from Fig. 4, which reports the fraction of cycles during which some transaction was pending on the bus with respect to total execution time. In such a congested environment, as can be seen in Fig. 5, AMBA AXI and STBus (with 4-stage FIFOs) were able to achieve transfer efficiencies (defined as data actually moved over bus contention time) of up to 80% and 85% respectively, while AMBA AHB reached 49% only - near to its maximum theoretical efficiency of 52% (one wait state per data word). The resulting execution times, as Fig. 3 shows, got 79% worse for AMBA AHB when moving from two to eight cores, while AXI and STBus managed to stay within 15% and 18%. The impact of FIFOs in STBus was noticeable, since the interconnect with minimal buffering showed execution times 36% worse than in the two-core setup. This stresses the impact that comparatively low-area-overhead optimizations can sometimes have in complex systems. It must be pointed out, however, that protocol improvements alone cannot overcome the intrinsic performance bound due to the shared nature of the interconnect resources. While protocol features can push the saturation boundary further, and get near to a 100% efficiency, traffic loads taking advantage of more parallel topologies will always exist. The charts reported here already show some traces of saturation even for the most advanced interconnects. According to simulation results, some of the advanced features in AMBA AXI provided highly scalable bandwidth, but at the price of latency in low-contention setups. Fig. 6 shows the minimum and average amount of cycles required to complete a single write and a burst read transaction in STBus and AMBA AXI. STBus has a minimal overhead for transaction initiation, as low as a single cycle if communication resources are free. This was confirmed by figures showing a best-case three-cycle latency for single accesses (initiation, wait state, data transfer) and a nine-cycle latency for 4-beat bursts. AMBA AXI, due to its complex channel management and arbitration, requires more time to initiate and close a transaction.

VI) **CONCLUSION:**

In this paper, the architecture of AMBA Based Network Interface (NI) in an asynchronous NoC is implemented. We can also implement this architecture in a synchronous NoC it will less area require to implement and it determines the clock distribution and predictability etc., but for low power consumption the designers prefer Asynchronous NoC, even though it require large area and there is no clock distribution and so on such drawbacks are there, but we can gain low power consumption and high operating speed, so designer prefers Asynchronous NoC. To achieve a high speed while transferring the data we use memory as a master and AHB as a slave. Based on this Concept Asynchronous AMBA-AHB based network interface we are going to design an Asynchronous NoC router (4 x 4 Mesh Topology) as future work to accomplish low power consumption and high speed which can improve the system performance.

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