

## Channel length scaling and the impact of metal gate work function on the performance of double gate-metal oxide semiconductor field-effect transistors

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**Abstract.** In this paper, we study the effects of short channel on double gate MOSFETs. We evaluate the variation of the threshold voltage, the subthreshold slope, the leakage current and the drain-induced barrier lowering when channel length  $L_{CH}$  decreases. Furthermore, quantum effects on the performance of DG-MOSFETs are addressed and discussed. We also study the influence of metal gate work function on the performance of nanoscale MOSFETs. We use a self-consistent Poisson–Schrödinger solver in two dimensions over the entire device. A good agreement with numerical simulation results is obtained.

**Keywords.** Nanotransistor; metal oxide semiconductor field-effect transistors; silicon-on-insulator; work function; quantum effects; self-consistent.

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### 1. Introduction

Double gate silicon-on-insulator (DG SOI) devices have recently been of great interest, particularly for the investigation of sub-10 nm field-effect transistors [1–3]. As the channel length is reduced from one transistor generation to the next, there is more and more interest in device behaviour and performance at the ballistic limit. The ballistic MOSFET was first examined by Natori [4]. Later, Harrison *et al* [5] showed an excellent fit by comparison with numerical simulation of ballistic transport and experimental data extracted in DG-MOSFETs devices. At these channel length limits, the susceptibility of the transistor to short-channel effects (SCE) is monitored in several ways such as threshold voltage ( $V_{TH}$ ), subthreshold voltage slope ( $S$ ), leakage current ( $I_{OFF}$ ) and the drain-induced barrier lowering (DIBL).

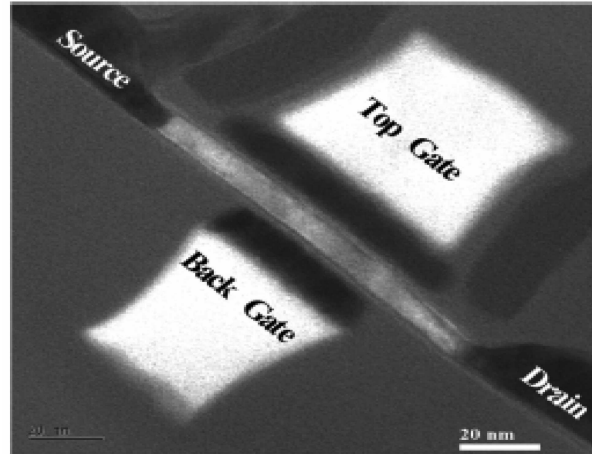
Channel length decreases and becomes crucial in deep-submicrometre technologies. In this work, we study the effect of short channel and the influences of quantum mechanical on nanoscale DG-MOSFETs.

As CMOS technology continues to scale, metal gate electrodes need to be introduced to overcome the deleterious effects of doped polysilicon, namely gate electrode depletion, high resistance, and compatibility with high-k-gate dielectrics. In order to reduce the degree of SCEs, metal gate electrodes will require work functions that can be tuned to a desired value. Many approaches including implanted metals [6], fully silicided gates [7], and alloy metals [8] have been studied in an effort to achieve metal gates with tunable work function. Recently, the use of metal bilayers has been reported as another method to set the work function [9]. In this study, we investigate also the impact of metal work function on the SCEs in double-gate SOI transistor.

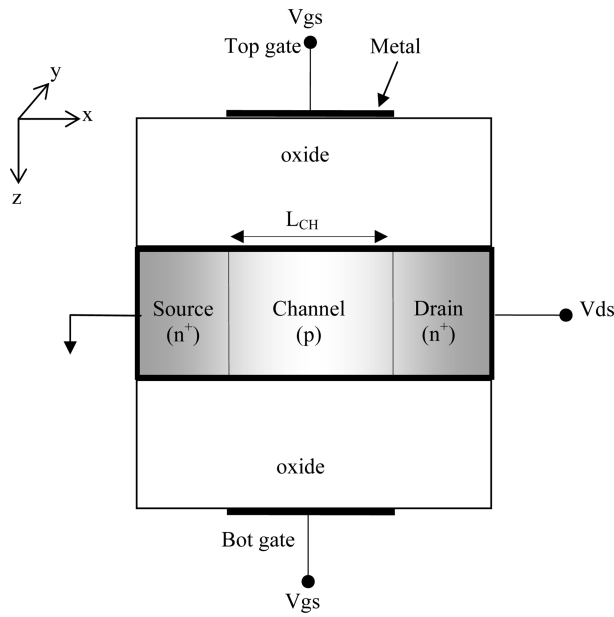
Two classes of simulation tools have been developed for this work. The first solves the continuity equation and Poisson equation in 2D using a finite difference scheme with a non-uniform mesh size. As critical transistor dimensions scale below the 10 nm (nanoscale) regime, quantum mechanical effects begin to manifest and affect important device performance [2,10]. Therefore, the second simulation tools which can be applied to design nanoscale transistor in the future, require new theory and modelling techniques that capture the physics of quantum transport accurately and efficiently in ballistic regime. This model is based on the self-consistent solution in two dimensions to the Poisson equation and Schrödinger equation system using the Newton–Raphson algorithm. In addition, the model is continuous over all gate and drain bias ranges, which makes it very suitable to simulate novel silicon transistor structures.

## **2. Simulated device**

There are two primary device structures that have been widely studied and used in CMOS (complementary MOS) technology. The first is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate and the second is called SOI (silicon-on-insulator), where a transistor is built on a thin silicon layer which is separated from the substrate by a layer of insulator (figure 1). The SOI MOSFET process has been described in [11]. The main technological step is the silicon selective epitaxial growth (SEG). The simulated device structure (figure 2) is a symmetric DG-MOSFET with S/D regions doped at  $10^{20} \text{ cm}^{-3}$  and an intrinsic channel. No gate-to-S/D overlap is assumed. The source/drain lengths are 5 nm, the top and bottom gate oxide thickness are  $t_{\text{ox}} = 1.5 \text{ nm}$ , the silicon body thickness  $t_{\text{si}}$  is taken as 1.5 nm and the transistor is assumed to be wide ( $y$ -dimension is treated as infinite). The metal gate work function  $\phi_m$  is 4.25 eV unless otherwise noted. The same gate voltage  $V_{gs}$  is applied to both gates. All calculations have been done at room temperature.



**Figure 1.** SEM picture of a 50-nm gate length DG transistor [12].



**Figure 2.** Symmetrical DG-MOSFET considered in this work.

### 3. Transport descriptions

#### 3.1 Drift diffusion model

The conduction in this model is governed by the Poisson's equation (1) and the equations of continuities of the carriers (2), (3). The Poisson's equation which

couples the electrostatic potential  $V$  to the density of charge is given by

$$\nabla^2 V = \frac{-q}{\varepsilon} [p - n + N_D^+ + N_A^- + n_T], \quad (1)$$

where  $n$  and  $p$  represent the densities of the electrons and the holes, respectively,  $N_D^+$  and  $N_A^-$  are the ionized donor and acceptor impurity concentrations, respectively,  $n_T$  is the density of carriers due to the centre of recombination [13] and  $\varepsilon$  is the dielectric constant. The transport equations express the current densities of the electrons and the holes; they are composed of two components, drift and diffusion [13].

$$\vec{J}_n = q \cdot \mu_n \cdot n \cdot \vec{E} + q \cdot D_n \cdot \vec{\nabla}_n, \quad (2)$$

$$\vec{J}_p = q \cdot \mu_p \cdot p \cdot \vec{E} - q \cdot D_p \cdot \vec{\nabla}_p, \quad (3)$$

where  $\mu_n$  and  $\mu_p$  are the electron and hole mobilities,  $D_n$  and  $D_p$  are the diffusion coefficients of electrons and holes and  $\vec{\nabla}_n$  and  $\vec{\nabla}_p$  are the two-dimensional gradients of concentration of electrons and holes.  $\vec{E}$  is the electric field applied. The equations of continuities represent the carriers conservation in a volume element for the electrons and the holes, respectively.

$$\frac{\partial n}{\partial t} = GR_n + \frac{1}{q} \vec{\nabla} J_n \quad (4)$$

$$\frac{\partial p}{\partial t} = GR_p - \frac{1}{q} \vec{\nabla} J_p. \quad (5)$$

The  $GR_n$  and  $GR_p$  terms describe the phenomena of recombination-generation and  $J_n$  and  $J_p$  are the current densities [13]. In a steady state regime, electron concentrations  $n$ , holes  $p$ , electrostatic potential  $V$ , and electrical current  $I$  are obtained from the solutions of eqs (1)–(5) using the finite differences method [13,14]. The solution of the equations consists of the discretization of the field in a finite number of points and the approach of the partial derivative, using finite differences method, in all the interior nodes of the field while taking in account the boundary conditions in order to obtain a linear system of equations in the following matrix form:

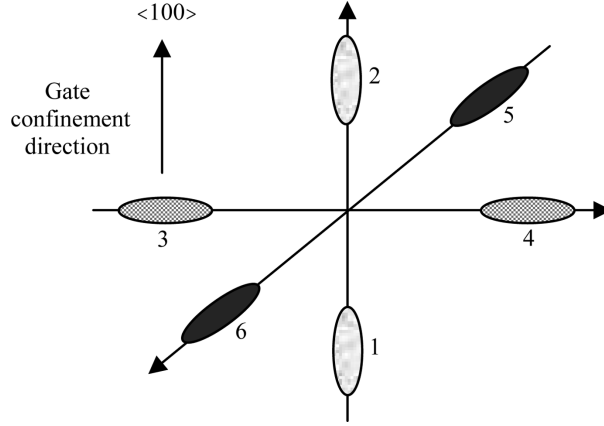
$$[M] \cdot [X] = [b],$$

where  $M$  is the total matrix and  $b$  is the vector source.

To solve this system, we use the iterative method of Gausse–Seidel. It is particularly well adapted to the matrices of this type because they do not require additional storage and also present a good numerical convergence [14].

### 3.2 Self-consistent Poisson–Schrödinger model

In the following section, we present a self-consistent Poisson–Schrödinger model with coupled system of equation, while charge transport has been self-consistently



**Figure 3.** Six equivalent conduction band ellipsoids in bulk silicon. Ellipsoids 1 and 2 respond with a longitudinal effective mass in the gate confinement direction, while ellipsoids 3 to 6 respond with a transverse effective mass in the gate confinement direction.

included adopting a classical model. This approach is justified by several results presented in the literature [2,15–17]. The potential profile in the two-dimensional simulation domains obeys the Poisson equation (1). Schrödinger’s equation is solved assuming an effective mass approximation for each  $x$  independently across the device. In all the calculations presented here, we assume that the  $\text{SiO}_2/\text{Si}$  interface is parallel to the  $\langle 100 \rangle$  plane. For this particular case, six equivalent minima of the bulk silicon conduction band split into two sets of sub-bands (figure 3). The first set consists of two equivalent valleys with in-plane effective mass  $m_l = 0.91m_0$  and perpendicular effective mass  $m_t = 0.19m_0$ . The second set consists of the other four equivalent valleys, where  $m_0$  is the free electron mass. Note that, only those electrons in the first set are treated in the simulation.

At each iteration step, one needs to solve the Schrödinger equation of the form

$$\frac{\hbar^2}{2m_z^*} \frac{\partial^2}{\partial z^2} \Psi_i(x, z) - qV(x, z)\Psi_i(x, z) = E_i(x)\Psi_i(x, z) \quad (6)$$

two times, i.e. for each equivalent valley pair where  $m_z^*$  is the electron effective mass in the  $z$ -direction,  $q$  is the electron charge,  $\hbar$  is the Planck’s constant,  $\Psi(x, z)$  is the wave function corresponding to the eigenvalue  $E_i$  for the  $i$ th sub-band, and  $V(x, z)$  is the electrostatics potential. Once the energy eigenstates and the corresponding eigenfunctions are known, the 2D electron density with energy lower than the peak sub-band energy is obtained as [18]

$$n_{\text{left}} = n_{2Di} \left[ \ln(1 + e^{\mu_S}) + \frac{1}{\sqrt{\pi}} \int_0^{E_{\text{peak}}} \frac{dE}{\sqrt{E}} \mathfrak{S}_{-1/2}(\mu_S - E) + \frac{1}{\sqrt{\pi}} \int_{E_{\text{peak}}}^{\infty} \frac{dE}{\sqrt{E}} \mathfrak{S}_{-1/2}(\mu_D - E) \right] \quad (7)$$

and the electron density with energy higher than the peak sub-band energy  $E_{\text{peak}}$  is obtained as

$$n_{\text{right}} = n_{2Di} \left[ \ln(1 + e^{\mu_D}) + \frac{1}{\sqrt{\pi}} \int_0^{E_{\text{peak}}} \frac{dE}{\sqrt{E}} \mathfrak{S}_{-1/2}(\mu_D - E) + \frac{1}{\sqrt{\pi}} \int_{E_{\text{peak}}}^{\infty} \frac{dE}{\sqrt{E}} \mathfrak{S}_{-1/2}(\mu_S - E) \right] \quad (8)$$

$$n_{2Di} = \frac{\sqrt{m_x^* m_y^*} k_B T}{\pi \hbar^2} \frac{1}{2}, \quad (9)$$

where  $m_x^*$ ,  $m_y^*$  are the electron effective mass in the  $x$ - and  $y$ -direction respectively, and  $T$  is the temperature. Then the electron density is fed back to the Poisson equation solver for the self-consistent solution. Once self-consistency is achieved, the current can be expressed as [18]

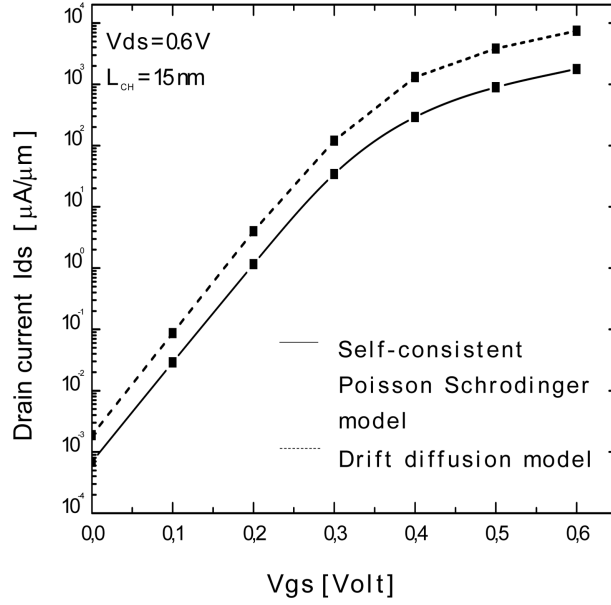
$$J = \frac{2q}{h^2} \sqrt{\frac{m_y^*}{2}} \left( \frac{k_B T}{\pi} \right)^{3/2} [\mathfrak{S}_{1/2}(\mu_S - E_{\text{peak}}) - \mathfrak{S}_{1/2}(\mu_D - E)] \quad (10)$$

The total current is the sum of contributions from all relevant valleys and sub-bands.  $E_{\text{peak}}$  is the peak sub-band energy,  $\mu_S$  and  $\mu_D$  are the Fermi potential energies of the source and drain, respectively, and  $k_B$  is the Boltzmann constant.  $\mathfrak{S}_{-1/2}$  and  $\mathfrak{S}_{+1/2}$  are the Fermi-Dirac integral of the order  $(-1/2, +1/2)$  respectively (see [19] and [20] for analytical approximation of  $\mathfrak{S}_{-1/2}$  and  $\mathfrak{S}_{+1/2}$ ).

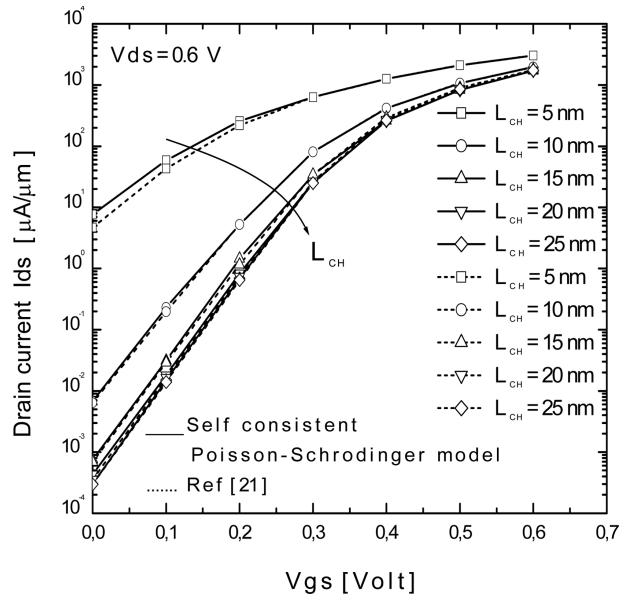
#### 4. Simulation results

We first compare the electrical characteristics obtained by both models, classical model (without quantum effects) and self-consistent model (with quantum effects). Figure 4, which represents the currents of drain  $I_{ds} - V_{gs}$  for  $V_{ds} = 0.6$  V, clarifies well the difference between the two curves. Therefore, a self-consistent Poisson-Schrödinger model, which takes into account quantum mechanical effects, is used in this work. To check the accuracy of our numerical calculations, the drain current  $I_{ds}$  vs.  $V_{gs}$  was calculated using self-consistent Poisson-Schrödinger model (solid lines) and compared with simulated results presented in [21] (dotted lines) in which the non-equilibrium Green's function (NEGF) formalism is used to simulate the DG-MOSFET. Good agreement has been found in figure 5.

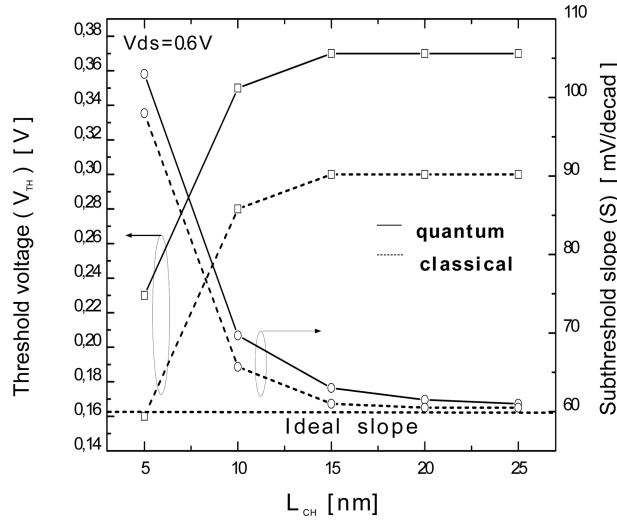
Figure 5 presents the drain current against gate voltage ( $I_{ds} - V_{gs}$ ) characteristics of the double gate SOI transistor obtained from eq. (10) for different channel lengths. It can be seen that the reduction of the channel length results in shifting the characteristics to the left and it is clear that as the channel length gets below 10 nm, the subthreshold current rises dramatically. Since the drain current depends on the channel length, the threshold voltage of the double gate SOI transistor should



**Figure 4.**  $I_{ds}$  vs.  $V_{gs}$ , comparison between drift diffusion and Poisson–Schrödinger models. The quantum mechanical effect is distinctly visible.



**Figure 5.** Comparison of the output characteristics between our model (solid lines) and the model presented in [21] (dotted lines).



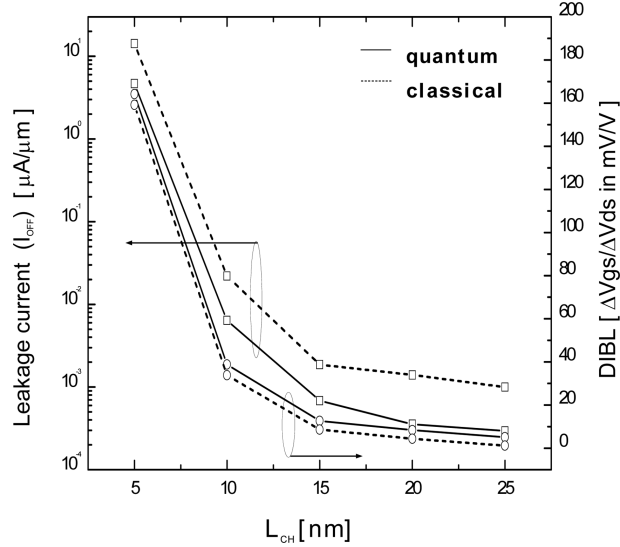
**Figure 6.** Threshold voltage and subthreshold slope vs. different channel lengths (obtained from the quantum (solid line) and classical (dotted line) transport models).

also be channel length dependent. Figure 6 shows that the threshold voltage ( $V_{TH}$ ) is proportional to  $L_{CH}$ . In the range of channel length under 15 nm the threshold voltage decreases with reduction of the  $L_{CH}$ . In 5 nm channel length device, there is significant reduction in the  $V_{TH}$ . After that even if  $L_{CH}$  increases,  $V_{TH}$  remains practically constant. A  $V_{TH}$  shift (about 70 mV) which is due to quantum effects can be easily observed. The quantum effects are associated with the quantum confinement in DG-MOSFET, which cannot be captured in classical simulation. Noting that  $V_{TH}$  is defined by  $V_{gs}$  at  $I_{ds} = I_{do} \cdot (W/L_{CH})$  [22],  $I_{do} = 1 \mu A$ , where  $W$  is the channel width.

Another important parameter characterizing the short channel performance is the subthreshold slope. Figure 6 represents the evolution of subthreshold slope ( $S$ ) with and without quantum effects as a function of the channel length ( $L_{CH}$ ) for  $V_{ds} = 0.6$  V. It can be observed that when  $L_{CH}$  decreases,  $S$  increases and moves away from the ideal value 60 mV/decade [23]. Figure 6 also shows that  $S$  shifts to slightly higher values due to quantum effects. The variation of the leakage current ( $I_{OFF}$ ) showed in figure 7, obtained from the  $I_{ds}-V_{gs}$  characteristics (using classical and quantum simulation), shows the adverse effect of short channels which appears with significant values of  $I_{OFF}$  when  $L_{CH}$  is decreased. We also observe that classical simulation provides higher  $I_{OFF}$  compared to quantum simulation. This is due to the higher threshold voltage anticipated in quantum simulation.

For short channel devices, application of a high drain-to-source bias can shorten the threshold voltage and increase the off-currents. This is known as drain-induced barrier lowering (DIBL), and it is another manifestation of the short channel effects. Figure 7 shows the effect of varying the channel length on the DIBL for low ( $V_{ds} = 50$  mV) and high ( $V_{ds} = 1$  V) drain bias and according to classical and quantum simulations. Above 15 nm, the DIBL are relatively small, but the DG-MOSFETs





**Figure 7.** Leakage current and DIBL vs. different channel lengths (obtained from the quantum (solid line) and classical (dotted line) transport models).

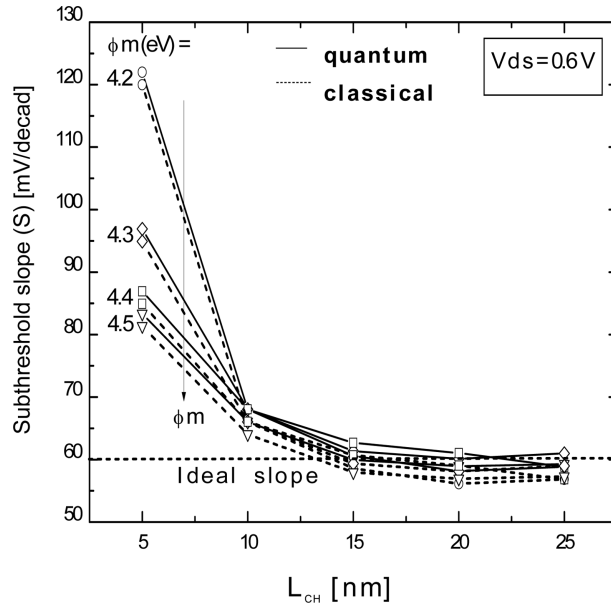
with  $L_{CH}$  less than 15 nm present significant DIBL effect. It can also be seen from the same figure that the impact of quantum mechanical on the DIBL in undoped DG-MOSFET is slight.

For advanced CMOS with low doping body DG-MOSFET, metal gate electrodes are required to replace poly-Si gate in order to eliminate poly-depletion and boron penetration effects. Metal gate with work function varying from 4.1 to 5 eV have been demonstrated by several groups [24,25], making them attractive candidates for future generation CMOS gate electrodes.

In this section, we focus on the impact of metal gate work function on nano DG-MOSFET performances. The effect of gate metal work function ( $\phi_m$ ) on the threshold voltage  $V_{TH}$  and hence on the leakage current  $I_{OFF}$  is well known. Therefore, it is sufficient to only state the following comment: when ( $\phi_m$ ) is raised,  $I_{OFF}$  decreases significantly and  $V_{TH}$  increases.

In figure 8, we examine the effect of varying the metal gate work function on the subthreshold slope for different channel lengths. The most significant effect is observed at  $L_{CH} = 5$  nm. One notes a reduction around 54% of  $S$  when  $\phi_m$  varies from 4.2 to 4.5 eV. As  $L_{CH}$  becomes greater than 10 nm, it has a less dependency on  $\phi_m$ . It is clear that high metal gate work function  $\phi_m$  leads to a better subthreshold slope when the MOSFETs are scaled down.

The DIBL is calculated as a function of  $L_{CH}$  for different  $\phi_m$ . This is illustrated in figure 9. For channel lengths below 10 nm ( $L_{CH} = 5$  nm), a reduction in DIBL around 20% can be observed when metal gate work function changes from 4.2 to 4.5 eV. On the other hand, for  $L_{CH}$  greater than 10 nm, the DIBL is not affected by  $\phi_m$ . We can observe from the same figures, i.e. figures 8 and 9, that the influence of quantum mechanical on the subthreshold slope and the DIBL remains slight whatever the value of metal gate work function is.



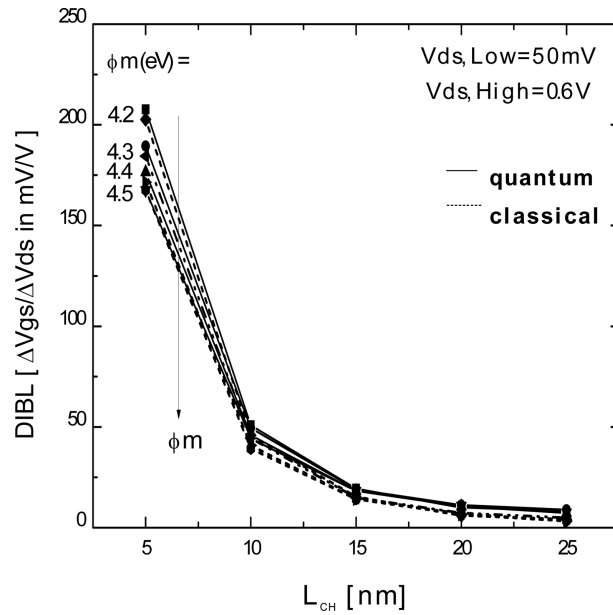
**Figure 8.** Subthreshold slope vs. different channel lengths and at different metal gate work functions. The quantum (classical) simulation results are plotted in solid (dotted) line.

In order to maintain  $I_{\text{OFF}}$  very low, it is necessary to increase the metal work function. In addition, the rise in metal work function is accompanied by an increase in threshold voltage. For this sake, the choice of the metal work function must be a delicate compromise between electric performance (reduction of the  $I_{\text{OFF}}$  current) and commutation rate (shift from the blocked state to an active state) associated to  $V_{\text{TH}}$ . Figure 10 shows the evolution of the  $I_{\text{OFF}}$  current and the threshold voltage  $V_{\text{TH}}$  resulting from the quantum and classical models and according to the metal work function. The value  $\phi_m = 4.35$  eV seems to ensure a weak leakage current  $I_{\text{OFF}}$  ( $= 1.46 \times 10^{-5} \mu\text{A}/\mu\text{m}$ ) while preserving a reasonable  $V_{\text{TH}}$  ( $= 0.42$  V) when using quantum model. On the other hand, when using classical model, the value of the metal work function is 4.41 eV (the error is about 0.06 eV).

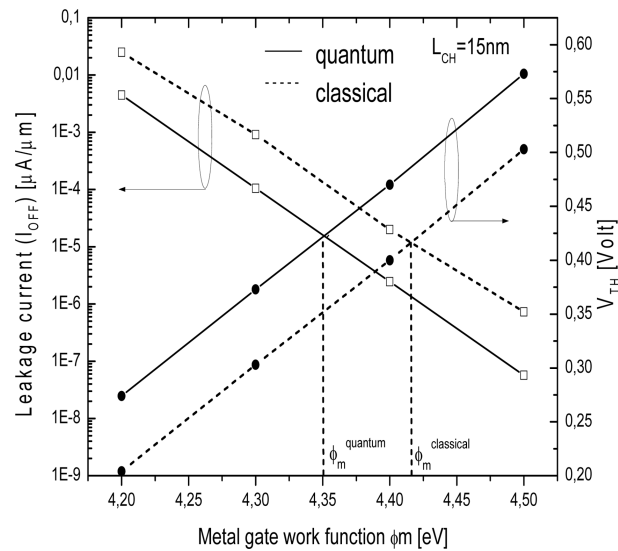
## 5. Conclusion

A two-dimensional self-consistent Poisson-Schrödinger model which takes into account the quantum mechanical effects are used with appropriate boundary conditions to explore the short channel effects and the influences of QM in double gate MOSFET as channel length varies in the range of 25 nm down to 5 nm. The model is particularly dedicated to ultra-scaled devices. We also carry out the comparison by means of a drift diffusion model.

Based on the threshold voltage, subthreshold slope, leakage current and DIBL variation with channel length, the short channel behaviour of the double gate



**Figure 9.** DIBL vs. channel length for metal gate work functions between 4.2 and 4.5 eV. The quantum (classical) simulation results are plotted in solid (dotted) line.



**Figure 10.** Leakage current and threshold voltage vs. work function (the  $\phi_m$  deduced from the quantum and classical models are illustrated graphically).

MOSFET is evaluated using self-consistent Poisson–Schrödinger and drift diffusion models.

It is found that these parameters present a significant degradation when channel length is decreased. This results in a reduction of device performance, hence determining the limits of miniaturization. We have also found that QM effects increase the threshold voltage and decrease the leakage current, whereas it has little impact on subthreshold slope and DIBL. As a consequence, the degradation of the device performance due to short channel effects resulting from classical simulation is higher than that of the quantum simulation.

Our codes allow us to simultaneously take into account the effects of the metal gate work function. The results show that the impact of metal gate work function  $\phi_m$  on drain-induced barrier lowering (DIBL) and subthreshold slope ( $S$ ) are negligible, but for channel lengths  $L_{CH}$  less than 10 nm the effect becomes important. It is also found that, for any given channel length ( $L_{CH}$ ), the increase of the metal gate work function ( $\phi_m$ ) results in an increase of the threshold voltage ( $V_{TH}$ ). At the same time, a decrease in the leakage current ( $I_{OFF}$ ) is observed. Furthermore, it can be noticed that a good compromise between performances and commutation rate appears to be well achieved at  $\phi_m = 4.35$  eV obtained from quantum simulation and at  $\phi_m = 4.41$  eV obtained from classical simulation. We can conclude that QM effects should be considered in thin SOI devices to obtain accurate description of carrier transport of the nanoscale devices.

For future work, other issues will be taken in account, such as quantum mechanical (QM) source-to-drain (S/D) electron tunnelling and high-k gate dielectrics effects.

## References

- [1] M S Lundstrom and Z Ren, *IEEE Trans. Electron. Devices* **49**(1), 133 (2002)
- [2] Z Ren, R Venugopal, S Datta, M S Lundstrom, D Jovanovic and J G Fossum, *IEDM Tech. Digest* (2000) pp. 715–718
- [3] Yiming Li and Hong-Mu Chou, *IEEE Trans. Nanotechnol.* **4**(5), 645 (2005)
- [4] N Natori, *J. Appl. Phys.* **76**(8), 4879 (1994)
- [5] S Harrison *et al*, *Proc. ESSDERC* (2004) pp. 373–376
- [6] R Lin, Q Lu, P Ranade, T-J King and C Hu, *IEEE Electron. Device Lett.* **23**(1), 49 (2002)
- [7] C Cabral Jr *et al*, *Symp. VLSI Tech. Dig.* (June 2004) pp. 15–17
- [8] H Zhong, S Hong, Y-S Suh, H Lazar, G Heuss and V Misra, *IEDM Tech. Dig.* (2001) pp. 467–470
- [9] I S Jeon *et al*, *IEDM Tech. Dig.* (2004) pp. 303–306
- [10] A Svizhenko, M P Anantram, T R Govindan, B Biegel and R Venugopal, *J. Appl. Phys.* **91**(4), 2343 (2002)
- [11] Geold W Neudeck, Tai-Chi Su and Jac P Denton, *IEDM* (2000) pp. 169–172
- [12] Julie Widiez *et al*, *IEEE Trans. Electron. Devices* **52**(8), 1772 (2005)
- [13] M Heydemmann, *Résolution numérique des équations bidimensionnelles de transport dans les semi-conducteurs*, Doctorate dissertation (Paris Sud University, 1972)
- [14] S Latreche, *Etude de transistors bipolaire a émetteur polysilicium autoaligné réalisés en technologie CMOS*, Doctorate dissertation (University of Constantine, 1998)

- [15] G Iannaccone, G Fiori and G Curatola, Techniques and methods for the simulation of nanoscale ballistic MOSFETs, *Proc. of IEEE Nanotechnology 2002* (Washington DC, 2002) pp. 193–196
- [16] Agostino Pirovano, Andrea L Lacaita and Alessandro S Spinelli, *IEEE Trans. Electron. Devices* **49**(1), 25 (2002)
- [17] G Fiori and G Iannaccone, *Nanotechnology* **13**(3), 294 (2002)
- [18] Zhibin Ren, *Nanoscale MOSFETS: Physics, simulation and design*, Ph.D. dissertation (Purdue University, October 2002)
- [19] A Abramo, A Cardin, L Selmi and E Sangiorgi, *IEEE Trans. Electron. Devices* **47**(10), 1858 (2000)
- [20] D Vasileska, *J. Modelling and Simulation of Microsystems* **1**(1), 49 (1999)
- [21] Amr A Ahmadain, Kenneth P Roenker and Karen A Tomko, *Sixth IEEE Conference on Nanotechnology*, volume 1, 16–19, 17–20 June 2006
- [22] T Hori, *Gate dielectrics and MOS ULSIs: Principles, technologies, and applications* edited by W Engl (Springer, 1997)
- [23] Marc Bescond, *Modélisation et simulation du transport quantique dans les transistors MOS nanométriques*, Doctorate dissertation (University of Provence, Aix-Marseille I, 2004)
- [24] Ching-Huang Lu *et al*, *IEEE Electron Device Lett.* **26**(7), 445 (2005)
- [25] X P Wang *et al*, *Electron Device Lett.* **27**(1), 31 (2006)