

## Status on the development of front-end and readout electronics for large silicon trackers

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**Abstract.** Final results on a CMOS 0.18  $\mu\text{m}$  front-end chip for silicon strips readout are summarized and preliminary results on time measurement are discussed. The status of the next version in 0.13  $\mu\text{m}$  is briefly presented.

**Keywords.** Silicon; readout; front-end; deep sub-micron.

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### 1. Introduction

In any detector concept foreseen at the ILC, a front-end readout system for tracking silicon detectors has to manage millions of channels. Consequently, the amount of material and power per channel has to be carefully optimized keeping noise and readout speed within the constraints of the experiment. It is therefore essential to look for the best integrated technologies available that allow to avoid as much as possible material added to the detector, such as connexions in terms of connectors, hybrid circuits, kaptons, and lead as well to a manageable amount of dissipated power. These technologies allow also to implement efficient data extraction and signal processing techniques such as analog sampling and on-chip digitization. For detectors that covers of the order of 100 square meters and millions of channels, the multiplexing of several tasks such as analog-to-digital conversion and zero suppression is mandatory.

## 2. Silicon strips detector numbers and detector data

At the ILC, the silicon trackers will have up to ten millions of 10–60 cm long strips [1]. Readout pitch is foreseen to be 50 to 100  $\mu\text{m}$ , DC or AC coupled. The occupancy defined as the percentage of channel hits per bunch crossing will be less than 1% in the outer barrel and end caps layers, less than 5% in the inner barrel and end caps.

The ILC machine is foreseen to run bunches spaced by 150–300 ns for a data taking period of 1 ms followed by a 200 ms idle stage available for readout.

Pulse height will be used to improve the position resolution to a few  $\mu\text{m}$ , 5–10 samples of the detector pulse will be digitized with an 8–10 bits Wilkinson AD converter after storage in an analog pipe-line.

Time will be recorded on two scales:

- Coarse for 150–300 ns beam crossing tagging.
- Fine nanosecond timing, in order to estimate the coordinate along the strip. This is not intended to replace another detector layer, but will provide an estimation of the longitudinal position to a few centimeters.

## 3. On detector electronics

The front-end chip will integrate the following functions:

- Low noise amplification and pulse shaping.
- Pulse sampling: 5–10 samples over two shaping times.
- Buffering: 8-deep 2D analog buffer (5–10 samples and 8 events).
- Analog-to-digital conversion: Wilkinson is optimum in terms of room and power.
- Sparsification/calibration: both implemented on-chip.
- Digital processing: amplitude/time estimation and charge cluster algorithm.
- Power cycling: take benefit of the 1/200 duty cycle of the ILC engine.

### 3.1 *Expected charge measurements*

- Gain: 20 mV/MIP over 1–30 MIP.
- Noise:  $280 e^- + 10.5 e^-/\text{pF}$  (as simulated in CMOS 0.18  $\mu\text{m}$ ).
- Analog buffer: 8-deep (cells of 5–10 0.1 pF capacitors).
- Sparsifier: Threshold an analog sum of three adjacent channels after pulse shaping.
- ADC: 10–12 bits Wilkinson clocked at 96 MHz.

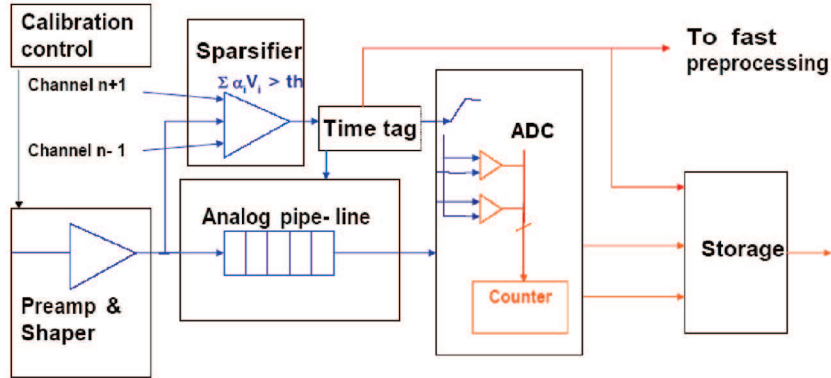


Figure 1. Front-end chip architecture.

### 3.2 Expected time measurements

- Time stamping: 30–50 ns time stamp the sparsifier output a 4\*BCO frequency clock.
- Fine time measurement: 1–3 ns 32\*BCO frequency clock multiplied on-chip.

Use digital signal processing over 5–10 digitized samples (see figure 2).

Expected fine time resolution: simulation under Matlab using a model of the full electronics chain from the preamplifier up to the ADC using a least squares fit algorithm from Cleland and Stern [2].

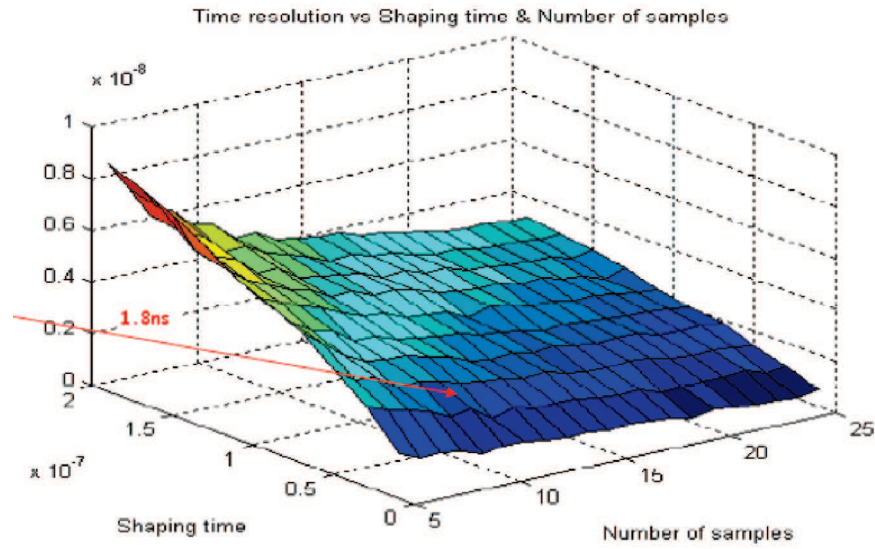
At  $S/N = 25$ , eight samples and 50 ns shaping time, 1.8 ns time resolution is foreseen.

## 4. Overall noise contributions

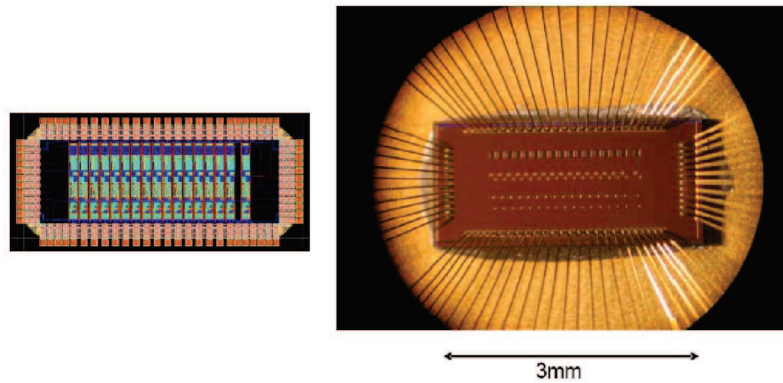
Using CMOS 0.18  $\mu\text{m}$  a signal-to-noise ratio of 25 is foreseen, according to table 1. CMOS 0.13  $\mu\text{m}$  is under investigations.

**Table 1.** Overall noise contributions at 30 pF detector capacitance and 3  $\mu\text{s}$  shaping time.

Source	Value	Noise 0.18 $\mu\text{m}$ CMOS
Input stage (measured)	$g_m = 0.7 \text{ mA/V}$	615 $e^-$ (measured)
m Detector leak	10 nA	588 $e^-$ (from literature)
Biasing resistor	10 M $\Omega$	423 (thermal noise)
Total		950 $e^-$



**Figure 2.** Expected fine time resolution.



**Figure 3.** CMOS 0.18  $\mu\text{m}$  UMC silicon. 16 + 1 channel CMOS (lay-out and picture).

### 5. Front-end test chip in CMOS 0.18 $\mu\text{m}$

The following structure has been submitted to Europractice and measured [3]. The chain comprises a low noise preamplifier, an RC-CR shaper, a sample and hold, a voltage follower and a comparator.

The layout and picture are shown in figure 3.

### 5.1 Preamp test results

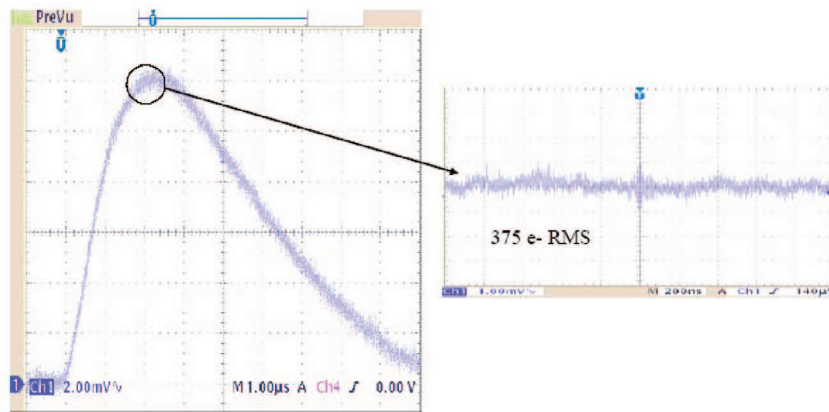
Twelve chips have been tested. One single failure was found in a comparator, and the following numbers were obtained:

- Gain: 8 mV/MIP as expected.
- Linearity:  $\pm 1.5\%$  against  $\pm 0.5\%$  expected due to large resistive transistor poorly modeled.
- Dynamic range: 50 MIP against 90 MIP expected, but within specs.
- Noise @ 70  $\mu$ W power, 3  $\mu$ s–20  $\mu$ s rise–fall times:  $498 \pm 16.5 e^-/\text{pF}$  against  $490 \pm 16.5 e^-/\text{pF}$  expected.

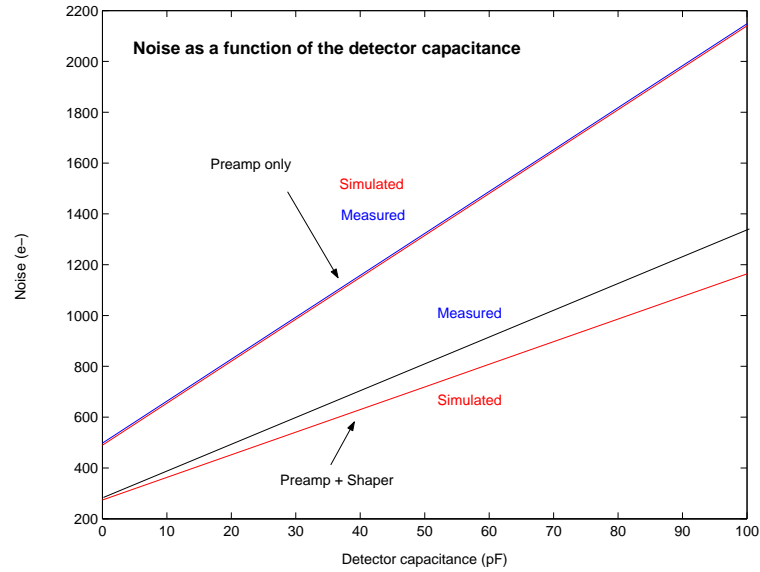
### 5.2 Shaper test results

The noise at the output of the shaper is shown in figure 4, as measured on a chip onboard (wire-bonded) test card, to  $375 e^-$  against 280 simulated, due to a small bump in the frequency response, leading to small oscillations. The following results are obtained:

- Peaking time: 2–6  $\mu$ s tunable against 1–10 targeted.
- 6 MHz bump (650  $e^-$  added noise) show up in the soldered PCB test card, mostly removed using wired onboard version, due to smaller parasitic capacitance (2 pF against 10 pF).
- Noise @ 70  $\mu$ W power, 3  $\mu$ s peaking time.  $375 \pm 10.4 e^-/\text{pF}$  against  $274 \pm 8.9 e^-/\text{pF}$  expected, as shown in figure 5.



**Figure 4.** Preamp + shaper noise (wire-bonded on card).



**Figure 5.** Noise summary.

### 5.3 Sample and hold and comparator

Sample and hold work as expected. On the comparator, the threshold voltage spread of the inputs transistors, of the order of 5 mV, is due to transistors sized too small. Size has been increased from 10/0.5 to 200/10 in the 0.13  $\mu\text{m}$  version.

### 5.4 Test conclusions

The UMC 0.18  $\mu\text{m}$  CMOS process from UMC looks quite mature and reliable. Models are accurate, only one transistor failure on untested chips (Multiproject run), process spreads are of a few per cent only. The preamplifier is almost according to specs, the shaper is somewhat more noisy than expected, but matches simulations, the threshold voltage spread problem is understood. First prototype run delivered functional chips in a relatively new (in our field) deep sub-micron CMOS technology. These results are considered very encouraging.

## 6. Next designs

0.13  $\mu\text{m}$  CMOS is now available from Europractice. A cooperation between LPNHE and LAPP (Annecy le Vieux) has already started. Access to other technologies is envisaged as well with CERN (Marchioro and co-workers), in the mainframe of a EUDET programme. The motivations for 0.13  $\mu\text{m}$  are the following:

### *Development of front-end and readout electronics*

- This VLSI technology will be dominant in the industry in a few years.
- It is basically faster and power consumption is less (in particular for the digital)
- Some drawbacks that can be overcome for the analog.

Future plans in 0.13  $\mu\text{m}$  concern a 4-channel version to be sent by the end of April including preamplifier and shaper, sampler and analog pipe-line, ADC and power cycling. Then, depending on tests results, a 128-channel is foreseen to be sent by the fall of 2006 including digital: chip control (state machine), buffer memory (FIFO), calibrations LSQ estimations, centroids.

## **7. Conclusions**

A CMOS 0.18  $\mu\text{m}$  chip has been tested and the results are very encouraging. A test chip in CMOS 0.13  $\mu\text{m}$  is underway, including a full chain up to the AD converter and power cycling. This prototype should be sent by end of April 2006. In addition, 0.18  $\mu\text{m}$  and 0.13  $\mu\text{m}$  chips beam tests are scheduled at DESY and CERN. Design for 128 channels is scheduled for the end of 2006.

## **References**

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