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A new CAD model of step recovery diode and generation of UWB signals

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Abstract: Nonlinear characteristics of SRD are analyzed. A model of SRD for simulation is proposed based on dynamic capacitor and pn diode, which can be used in ADS software. A method of producing UWB monocycle short pulse based on SRD and Schottky diode is proposed and analyzed theoretically. The UWB signal generation produces monocycle pulse with the width of 400 ps and the p-p amplitude of 15 V. The simulated result meets the tested result, which proves the veracity of the new model of SRD.

Keywords: monocycle pulse, step recovery diode, ultra wide band, model

Classification: Microwave and millimeter wave devices, circuits, and systems

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1 Introduction

In recent years UWB (Ultra Wide Band) technology is widely used in UWB communication and UWB radar systems. The pulse generator is an essential component for these systems. In general, the pulse produced by the pulse generator has the features of monocycle, short width and high amplitude. The spectrum of this kind of pulse is much abundant. So the pulse has the performance of strong penetrability and anti-jamming, which is suitable for short-range communication, through-wall radar, exploring land radar, etc. SRD (Step recovery diode) is widely used in pulse generator. SRD is a kind of strongly nonlinear device. The operation process of pulse production is very complicated, that results in modeling difficulty for SRD. Moll [4] analyzed the features of SRD, but did not propose SRD model for CAD. Zhang [2] proposed a SRD model for CAD, which is not accurate enough.

In this paper, the nonlinear performance of SRD is analyzed in depth. A new model of SRD for CAD is proposed based on nonlinear capacitor and pn diode, which can be co-simulated with other components in ADS software. Then a new method of pulse generation based on SRD and Schottky diode is proposed. The produced pulse is amplified for UWB systems.

2 Analysis in depth for SRD

SRD is a $p-i-n$ diode with thin i layer, which is an energy storage element. A large amount of charge is stored in i layer during the forward conduction period while a dynamic equilibrium is maintained between injection and recombination of carriers. When SRD is stimulated from forward pulse to backward pulse, the forward current of SRD will not turn off immediately, but will turn off when carriers in i layer are exhausted. SRD can be modeled as the parallel connection of a dynamic capacitor and a pn diode. The equivalent circuit of SRD including all factors is shown in Fig. 1. C_p, L_s, R_s, $C_j(V)$ and D_1 represent package capacitance, lead inductance, series resistance, dynamic capacitance and pn diode respectively. The operation process of SRD from forward conduction to backward turn-off can be divided into five stages, shown in Fig. 1.

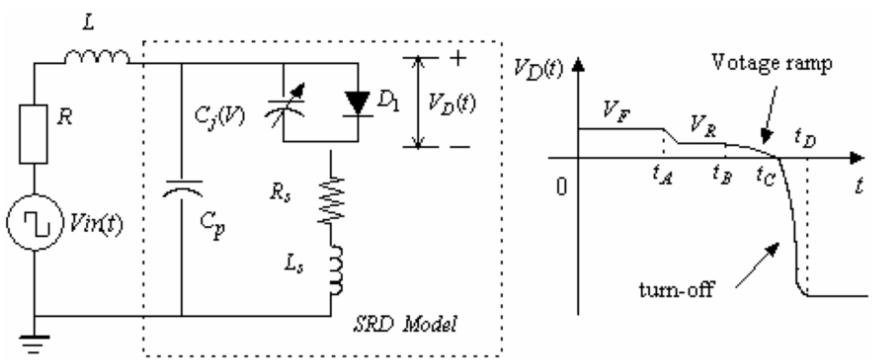

Fig. 1. SRD model scheme and the operation process

2.1 In the first stage (before t_A), the forward current of SRD is maintained

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constantly and the dynamic equilibrium is formed between injection and recombination of carries. The voltage through SRD is V_F. The charge stored in i layer is represented as $Q_A = I_F\tau$. In this stage SRD can be modeled as the parallel connection of a large capacitor and a pn diode.

2.2 In the second stage (between t_A and t_B), $Vin(t)$ steps from V^+ to V^- and the current is opposite. But SRD is still in conduction state because there is no space charge region in i layer. The charge in i layer is drawn out gradually and becomes less and less. In this process the voltage through SRD is slightly changed and the dynamic capacitance gets smaller and smaller according to the relationship $Q = C_j(V_R)V_R$. Thus, in this stage SRD can be modeled as the parallel connection of a pn diode and a capacitor with the capacitance getting smaller and smaller.

2.3 In the third stage (between t_B and t_C), the space charge region appears at t_B. The space charge region becomes wider and wider with the charge in i layer being drawn out gradually. At t_C, the charge in i layer is exhausted and SRD gets into the turn-off period. The nonlinear transition is mainly completed in this stage in which the dynamic capacitor transits from large capacitance to small capacitance, and the transition process is very complicated. Thus, in this stage SRD can be modeled as the parallel connection of a pn diode and a capacitor with the capacitance getting smaller and smaller. The width of space charge region is given by Moll [4]

$$W = 2d - \left(\frac{8DQ}{I_R}\right)^{1/2}. \tag{1}$$

Here, $2d$, D, Q and I_R are the width of i layer, the ambipolar diffusion constant $D \cong 20\,cm^2/V \cdot s$, charge in i layer and current respectively. The voltage through SRD is then

$$V = \frac{W^2 I_R}{4\varepsilon v A} = \frac{I_R}{\varepsilon v A}\left(d^2 - 2d\left(\frac{2DQ}{I_R}\right)^{1/2} + \frac{2DQ}{I_R}\right). \tag{2}$$

Here, v, A and ε are the velocity of electron and hole, working area of SRD and dielectric constant of i layer respectively. The ratio that the third item is divided by the second item in formula (2) is $m = \sqrt{2DQ}/(2d\sqrt{I_R})$. In this stage the charge in i layer is little. If suppose $Q = 10^{-13}C$, $I_R = 100\,mA$, $d = 1\,um$, it can get that $m = 0.03$. So the third item is much smaller than the second item. The third item can be ignored compared with the second item. After simplified the charge in i layer is

$$Q(V) = \frac{I_R}{8Dd^2}\left(d^4 - \frac{2\varepsilon v A d^2}{I_R}V + \left(\frac{\varepsilon v A}{I_R}\right)^2 V^2\right) \quad (\phi > V > 0). \tag{3}$$

By one order differential on formula (3), the dynamic capacitance can be obtained

$$C_j(V) = \frac{dQ}{dV_{SCL}} = \frac{\varepsilon v A}{4Dd^2}\left(\left(\frac{\varepsilon v A}{I_R}V - d^2\right)\right) \quad (\phi > V > 0). \tag{4}$$

Formula (4) indicates that the relationship between the dynamic capacitance and the voltage through SRD is linear.

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2.4 In the fourth stage (between t_C and t_D), SRD turns off and the charge is exhausted. SRD is charged by source. The opposite voltage through SRD is larger and lager and the dynamic capacitance is smaller and smaller. The i layer has little effect on SRD performance so that the function of SRD is similar as a pn varactor diode. In this stage SRD is modeled as a pn varactor diode. The dynamic capacitance is

$$C_j(V) = C_{j0}/\sqrt{1 - V/\phi}. \tag{5}$$

Here, $\phi = 0.7V$. C_{j0} is the dynamic capacitance at $V = 0$.

2.5 In the fifth stage (before t_D), SRD turns off.

3 New model of SRD for CAD

Summarized from above, SRD can be modeled as the parallel connection of a dynamic capacitor and a pn diode. The key of modeling is to educe the dynamic capacitor. The relationship of a dynamic capacitor and V can be defined as follows

$$C_j(V) = \begin{cases} 2K_1V + K_2 & (V > \phi) \\ 2K_4V + K_5 & (\phi \geq V \geq 0) \\ -K_7/\left(2\phi\sqrt{1 - V/\phi}\right) & (V < 0) \end{cases}. \tag{6}$$

By one order integral on formula (6), stored charge can be given as

$$Q(V) = \begin{cases} K_1V^2 + K_2V + K_3 & (V > \phi) \\ K_4V^2 + K_5V + K_6 & (\phi \geq V \geq 0) \\ K_7\sqrt{1 - V/\phi} + K_8 & (V < 0) \end{cases}. \tag{7}$$

Here, K_1, K_2, K_3, K_4, K_5, K_6, K_7 and K_8 can be determined by the boundary conditions and continuity of the charge and the capacitor.

Under certain opposite voltage, the dynamic capacitance is as follows

$$C_j(V_1) = -K_7/\left(2\phi\sqrt{1 - V_1/\phi}\right). \tag{8}$$

K_7 can be determined.

At $V = 0$, the boundary conditions of charge and capacitor are as follows

$$\begin{cases} Q(0) = K_6 = K_7 + K_8 = 0 \\ C_j(0) = K_5 = -K_7/2\phi \end{cases}. \tag{9}$$

K_6, K_8 and K_5 can be determined based on formula (9). Under the condition that SRD is in forward conduction period, Kotzebue [5] gives the relationship $\tau = R_fC_f$, where τ, R_f and C_f is the minority carriers life, forward conduction resistance and forward conduction capacitance respectively. Supposed that SRD is at two forward conduction voltages ϕ and ϕ', two forward conduction resistances can be tested. Then two forward conduction capacitances C_f and C'_f can be calculated at ϕ and ϕ' respectively. At $V = \phi$ and $V = \phi'$

$$\begin{cases} C_j(\phi) = 2K_4\phi + K_5 = 2K_1\phi + K_2 = C_f \\ 2K_1\phi' + K_2 = C'_f \end{cases}. \tag{10}$$

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Based on charge continuity we obtain

$$Q(\phi) = K_1\phi^2 + K_2\phi + K_3 = K_4\phi^2 + K_5\phi + K_6. \qquad (11)$$

So K_1, K_2, K_3, K_4, K_5, K_6, K_7 and K_8 is determined. Formula (6) is then

$$C_j(V) = \begin{cases} \dfrac{C_f' - C_f}{(\phi' - \phi)}V + \dfrac{C_f\phi' - C_f'\phi}{\phi' - \phi} & (V > \phi) \\ \dfrac{C_f - C_j(V_1)\sqrt{1 - V_1/\phi}}{\phi}V + C_j(V_1)\sqrt{1 - V_1/\phi} & (\phi \geq V \geq 0) \\ \dfrac{2C_j(V_1)\phi\sqrt{1 - V_1/\phi}}{2\phi\sqrt{1 - V/\phi}} & (V < 0) \end{cases}. \qquad (12)$$

4 design and realization of UWB Signals generation circuit [3]

UWB Signals generation circuit shown in Fig. 2 includes four parts: pulse production, pulse sharpening, monocycle pulse forming and pulse amplifying. The pulse production circuit produces impulse pulse with amplitude 3 V, where 2SC3356 matches the impedance between the source and SRD. The bottom of pulse is removed by Schottky diode HSCH9101 and the pulse can be more regular. Monocycle pulse forming circuit [1, 6] is made of a closed microstrip.

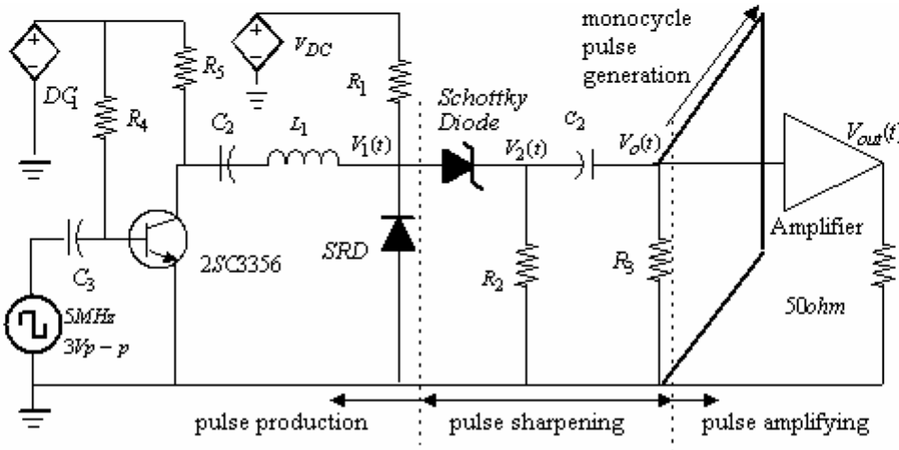

Fig. 2. UWB-Signals production circuit

The characteristic impedance of the microstrip is 50ohm and the length satisfies the formula (13)

$$L = \frac{C_0 P}{2\sqrt{\dfrac{\varepsilon_r + 1}{2} + \dfrac{\varepsilon_r - 1}{2}\left(1 + \dfrac{10h}{w}\right)^{-1/2}}}. \qquad (13)$$

Here, ε_r, C_0 and P are relative dielectric constant of PCB substrate, light velocity in air and the width of pulse sharpened by HSCH9101 respectively. The sharpened pulse (positive pulse) propagates to the end of the closed microstrip, reverses and then reflects. The negative pulse propagates back to

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the start of closed microstrip. When the negative pulse reaches the start of the closed microstrip, it takes a longer period of time (P) than the positive pulse. The negative pulse combines with the positive pulse so that the monocycle pulse forms. The p-p amplitude of the monocycle pulse is about 1.5 V. A UWB amplifier with 22 dB gain (AM012535MM) is used to amplify the UWB signals. As the model of SRD (MP4023) illustrated by formula (12), the UWB Signals production circuit shown in Fig. 2 can be simulated in ADS software. The simulated wave and the tested wave are shown in Fig. 3. The p-p amplitude and the width of the monocycle pulse are 15 V and 400 ps respectively.

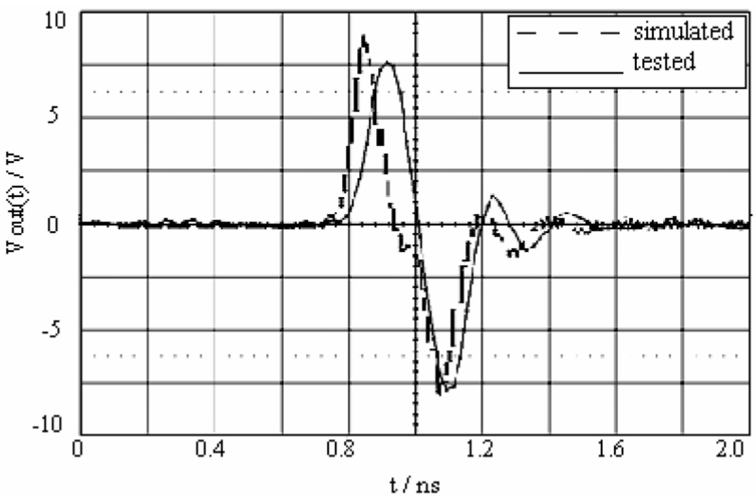

Fig. 3. Simulated and tested monocycle pulse waveform

5 Conclusion

The electronic characteristics of SRD have been analyzed in this paper. SRD is suitable for pulse generation because of its strongly nonlinear characteristic. A new model of SRD is proposed based on dynamic capacitor and pn diode, which can be used in ADS software. A UWB signals generation circuit is designed and realized based on SRD and Schottky diode. The width and the p-p amplitude of tested pulse are 400 ps and 15 V respectively. This kind of monocycle short pulse can be widely used in UWB communication and radar system. We can come to a conclusion by the comparison of simulated and tested waveform that the new model of SRD is exact for pulse generation. In order to validate veracity of the model in other circuits more experiments should be made in the future.

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