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An ultra low-power digitally controlled oscillator using novel Schmitt-trigger based hysteresis delay cells

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Abstract: In this paper, an ultra low power 15-bit digitally controlled oscillator (DCO) is proposed. The proposed DCO is designed based on a segmental coarse-tuning stage which employs novel Schmitt-trigger based hysteresis delay cells (HDC) as well as digitally controlled varactor (DCV) in the fine-tuning stage. Simulation of the proposed DCO using TSMC 180 nm model achieves controllable frequency range of 191 MHz $\sim$ 850 MHz with a wide linearity. Monte Carlo simulation demonstrates that the time-period jitter due to random power supply fluctuation is under 124.8 ps and the power consumption is 137 μW at 215 MHz with 1.8 V power supply.

Keywords: digitally controlled oscillator, low power, high resolution, good linearity, hysteresis delay cells

Classification: Integrated circuits

References

[1] P.-L. Chen, C.-C. Ching, and C.-Y. Lee, "A portable digitally controlled oscillator using novel varactors," *IEEE Trans. Circuit Syst. II*, vol. 52, no. 5, pp. 233–237, July 2005.

[2] C. Chung and C. Lee, "An all-digital phased-locked loop for high-speed clock generation," *IEEE J. Solid-State Circuits*, vol. 38, pp. 347–351, Feb. 2003.

[3] T. Olsson and P. Nilsson, "A digitally controlled PLL for SoC application," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 751–760, May 2004.

[4] D. Sheng, C.-C. Chung, and C.-Y. Lee, "An all-digital phase-locked loop with high-resolution for SoC application," *Proc. IEEE VLSI-DAT*, Hsinchu, Taiwan, doi: 10.1109/VDAT.2006.258161, pp. 207–210, April 2006.

[5] M. Meymandi-nejad and M. Sachdev, "A monotonic digitally controlled delay element," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2212–2219, Nov. 2005.

[6] S.-Y. Hsu, J.-Y. Yu, and C.-Y. Lee, "A sub-10-μW Digitally Controlled Oscillator Based on Hysteresis Delay Cell Topologies for WBAN Application," *IEEE Trans. Circuit Syst. II*, vol. 57, no. 12, pp. 951–955, Dec. 2010.

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1 Introduction

PHASED-LOCKED LOOPs (PLLs) are widely applied in many communication systems for clock and data recovery or frequency synthesis. Recently, PLL designers have approached to fully digital designs. Compared to analog PLLs, fully digital PLLs demonstrate better noise immunity and they are more robust to DC offset and drift phenomena. Digitally controlled oscillator (DCO) is the heart of ADPLL. DCO dominates the major performances of ADPLL such as power consumption and jitter, and thus is the most important component of such clocking circuits. Since 50% of power consumption of an ADPLL comes from the DCO, playing the major bottleneck in total power dissipation. [1, 2, 3], so, power reduction in a DCO design effectively cuts down ADPLL power, especially in low power SoC applications. Many DCOs implemented with standard cells have been proposed to enhance portability [1, 2, 3, 4, 5, 6]. Nevertheless they have a poor performance in terms of linearity or power consumption or LSB resolution.

In this paper, we present an ultra low power high-resolution wide-range 15-bit digitally controlled oscillator. The proposed DCO is designed based on a segmental coarse-tuning stage and employs novel Schmitt-trigger based hysteresis delay cells (HDC) and digitally controlled varactor (DCV) in the fine-tuning stage. This DCO is designed using standard-cells aiming for higher process portability.

2 Proposed DCO architecture

Fig. 1 shows structure of the proposed DCO. The proposed DCO structure is separated into the coarse-tuning stage and the fine-tuning stage. The coarse-tuning stage which is shown in Fig 1 (a) is composed of 31 two-input OR gates and 32-to-1 path selector MUX which can provide 32 different delay values by selecting different delay path organized by these 31 two-input OR. In the conventional coarse-tuning stages, the delay cell is composed of buffers. When delay line is requested to provide higher operation frequency, a shorter delay path is selected and the rest delay cells will not be used. However, these delay cells are not disabled. To reduce power consumption as the operating frequency changes, some enabling input control signals (EN [30:0]) are applied to disable those redundant two-input OR gates, leading to save power consumption.

The coarse-tuning stage uses 32-to-1 path selector MUX for delay-chain selection. This proposed selector is implemented by multistage transmission gates to reduce the loading capacitance of the MUX output and costs less area and lower power consumption compared to the conventional path selector MUXs which use tri-state buffers in their structure [1, 4].

Second in order to increase the resolution of DCO, a fine-tuning stage is added into DCO design as shown in Fig. 1 (b). To achieve better resolution and less power consumption, this fine-tuning stage is divided into three sub stages. The delay steps of these fine-tuning sub stages are different; delay cells of the first stage and third stage have the largest and smallest delay

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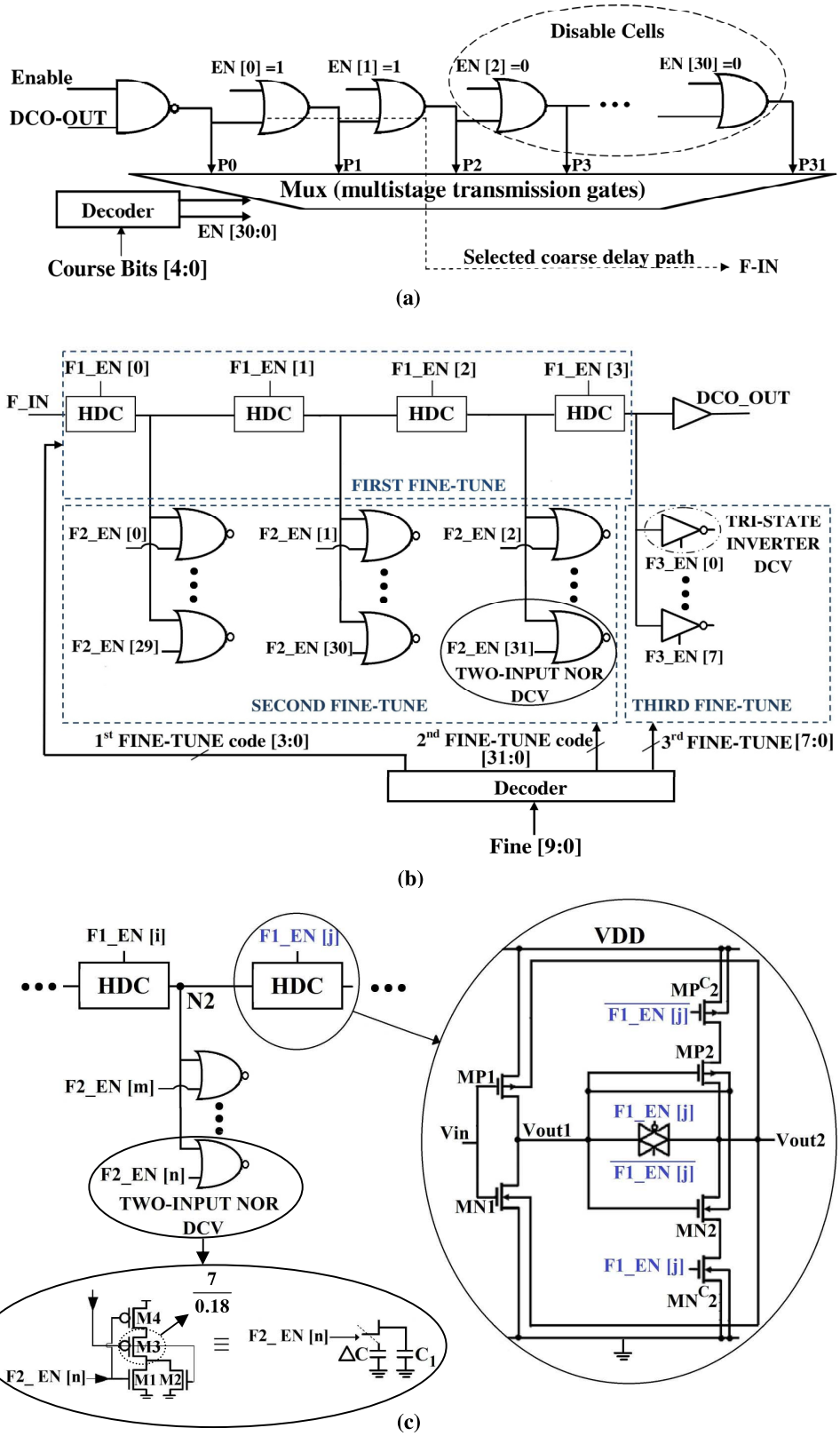

Fig. 1. a) Coarse-tuning-stage with two-input OR gates, b) Fine-tuning stage, c) Novel Schmitt-trigger based HDC and two-input NOR DCV and its equivalent circuit with ΔC capacitance

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step, respectively. So, delay cell of the third fine-tuning stage determines the DCO LSB resolution and controllable range of the first fine-tuning stage can cover delay step of the coarse-tuning stage easily. Since the HDC can provide larger delay step than DCV, the first tuning stage employs 4 HDCs to reduce the number of DCV cells, leading to save power consumption. Finally, the 2^{nd} and 3^{rd} fine-tuning stages are added which employ two input NOR and 8 tri-state inverter DCVs, respectively to improve resolution.

3 DCVs and a novel Schmitt-trigger based HDC structures

Fig. 1 (c) shows digitally controlled varactor cell (DCV) using two-input NOR gate and a novel Schmitt-trigger based hysteresis delay cell (HDC). The operation concept of DCV is to control the gate capacitance of logic gate with input state to adjust the delay time. As shown in Fig. 1 (c), the NOR gate capacitance at node N2 depends on control node F2_EN's value. The total gate capacitance of transistors M2 and M3 varies with F2_EN input states. The equivalent circuit of two-input NOR DCV cell in 2^{nd} fine-tuning stage is also shown in Fig. 1 (c). An initial capacitance (C_I) parallels with a capacitance difference (ΔC). The F2_EN input controls the capacitance difference (ΔC) in the N2 node. Fig. 2 (a) shows the gate capacitance difference characteristic which is simulated using HSPICE circuit simulator. The swing-averaged capacitance $C_{average}(F2\_EN)$, as F2_EN-node is in the 0 state or in the 1 state, is given by

$$C_{average}(F2\_EN) = \frac{1}{VDD}\int_0^{VDD} C(V_{gate}, F2\_EN)dV_{gate} \quad (1)$$

where $C(V_{gate}, F2\_EN)$ denotes the simulated gate capacitance shown in Fig. 2 (a). Based on (1), ΔC denotes the capacitance difference between $C_{average}(0)$ and $C_{average}(1)$. Consequently, the variable delay (ΔT) of the DCV in different F2_EN states can be calculated easily using the following linear equation:

$$\Delta T = K_{load} \times \Delta C \quad (2)$$

where K_{load} denotes the delay factor of driving inverter in HDC structure. The K_{load} value of the driving inverter is 0.498 (ns/pF) in target 0.18-μm TSMC CMOS cell library. The ΔC of Fig. 2 (a) is estimated to be around 7.02 fF. Therefore, ΔT of 3.495 ps (= 0.498×7.02) is easily obtain. Similar calculation such as computing the two-input NOR DCV can perform to obtain the delay (ΔT) of the tri-state inverter DCV in 3^{rd} fine-tuning stage. So the variable delay of the tri-state inverter DCV in different F3_EN states is obtained in 1.25 ps which is equivalent to the resolution of the DCO.

A novel HDC is designed on a Schmitt-trigger circuit basis, as shown in Fig. 1 (c). By adding two controlling transistors MP^C2 and MN^C2, the delay cell can be determined to operate as a normal inverter or hysteresis inverter. Therefore, a delay difference is derived between these two modes. The concept of maintaining or destroying hysteresis property can be applied to various forms of Schmitt-trigger circuits. The Schmitt-trigger which is used

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in our HDC circuit is the four transistor bulk driven Schmitt-trigger and has low power consumption. The HDC operation of Fig. 1 (c) can be described as follows. When the HDC is in the Schmitt-trigger mode (F1_EN = 1) and a high value signal is applied to Vin, Vout2 goes high. Where it provides 1.8 V forward body-bias to the transistors of MN1 and a zero forward body bias of MP1. Transistor MP1 is now off and MN1 remains on until Vin decreases to a certain voltage V_{lh}, where the output, Vout2 switches from high to low. Since MN1 has forward substrate body bias, a lower voltage is now needed to turn it off. This result in time delay t_1 for ramp input. The same happened occurs when a low value signal is applied to Vin and higher voltage is needed to turn MN1 on. This results in time delay t_2 for ramp input. The different switching voltage or switching time causes the hysteresis. Vout1 is buffered by MP2-MN2 inverter, which provides high fan-out capability.

4 Simulation and performance comparison

In order to compare the performance, the previously published approaches were designed and simulated using TSMC 180 nm model and then were compared with our proposed DCO. The performance comparisons are divided into three parts: coarse-tuning stage, path selector MUX, and fine-tuning stage. In the coarse-tuning stage, we design and simulate the conventional delay line of path-selection type by two-inverter delay cells for power consumption comparisons. For fair comparisons, both conventional and the proposed coarse-tuning stages have the same operation range. The simulation results of power consumption in different operation frequencies are shown in Table I. As compared with conventional approaches, the proposed coarse-tuning stage can reduce 88.3% and 10.8% of power consumption at 750 MHz and 215 MHz, respectively. Because the number of disable redundant delay scheme has different power reduction ratio in different operation frequencies.

In the cell-based design approach, many designs apply DCM or DCV to construct fine-tuning stage [1, 4]. For fair comparisons, these designs are simulated under the similar operation range and number of control bit. The simulated fine-tuning stages by different approaches are: DCV type

Table I. Power performance of different tuning-stages and path selector MUX

Tuning Stage	Design	Power @ 215 MHz	Power @ 750 MHz
Coarse Tuning	Conventional	86.55 µW	245.75 µW
	Proposed	77.21µW	28.86 µW
	Improvement Percent	10.8%	88.3%
Path Selector MUX	Conventional	6.617µW	-
	Proposed	3.91µW	-
	Improvement Percent	45.8%	-
Fine Tuning	Approach I [1]	465.92µW	-
	Approach II [4]	207.64µW	-
	Proposed	56.22µW	-

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(Approach I) [1], and combination of DCM and DCV type (Approach II) [4]. The performance comparisons simulated at 215 MHz at 1.8 V and typical corner cases, are summarized in Table I. Note that all of them have a similar performance in LSB resolution. But, in term of power consumption and area, the proposed design has significant improvement. Because a novel low power Schmitt-trigger based HDC can replace many DCV cells to obtain wider operating range. The reduction ratios are 87.9%, and 72.9% as compare with approach I, approach II, respectively.

The proposed DCO is evaluated in TSMC 180 nm and 1.8 V power supply. The power consumption of the proposed DCO, at 215 MHz frequency is 137 μW. The proposed DCO gains a high resolution of 1.37 ps and 3.58 ps delay step in the 2nd fine-tuning stage (two-input NOR DCV). These values are very close to the calculated resolution value in section 3 and shows the fidelity of analytical and simulation approach. Fig. 2 (b) shows operating frequency ranges of the novel DCO in the typical case (TT, 1.8 V, 25°C), the best case (FF, 1.9 V, −40°C), and the worst case (SS, 1.7 V, 125°C). The linearity already mentioned in (2) is emphasized by the simulation results showing a good linearity, which in turn is a key factor of PLL performance. Also the curves show that proposed DCO design is robust to PVT (Process, Voltage, and Temperature) variations. The controllable frequency range of proposed DCO is about 191 MHz ∼ 850 MHz in the typical corner case.

The jitter performance of the proposed DCO is evaluated at 500 MHz by Monte Carlo simulation using Gaussian distribution function taking into account 8% variation in supply voltage. Simulation results are shown in

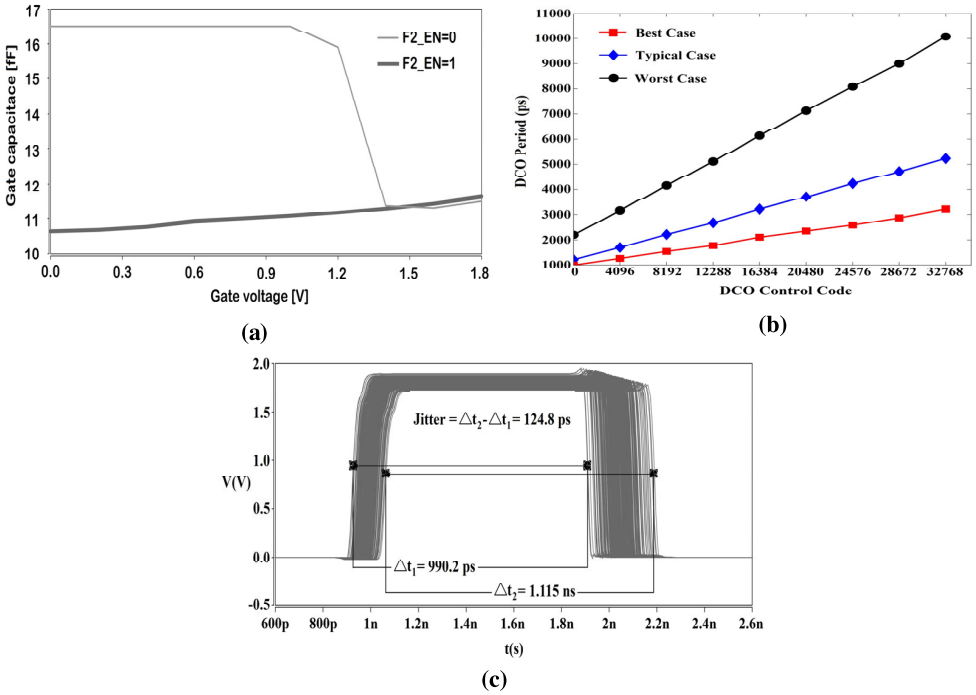

Fig. 2. a) Variation of two- input NOR gate's capacitance, b) Linearity of DCO, c) Time-period jitter of the proposed DCO (Monte Carlo analysis)

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Fig. 2 (c) by overlapping every cycle period. A 124.8 ps time-period Jitter is measured.

5 Conclusion

In this paper, an ultra low power and high-resolution DCO has been proposed. Proposed DCO has a segmental course–tuning stage and a fine-tuning stage with three sub stages which are implemented with novel Schmitt-trigger based HDC and different DCVs. Also our DCO has a proposed multistage path selector MUX which apply transmission gates in its structure and costs less area and lower power consumption compare to the conventional path selector MUXs which use tri-state buffers in their structure. Simulation of the proposed DCO using TSMC 180 nm model achieves a frequency of 191 MHz $\sim$ 850 MHz and power consumption of 137 μW at 215 MHz and 1.8 V power supply and 1.37 ps resolution.

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