

A 3D topology based-on partial overlapped clusters for NoC

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Abstract: Three-dimensional (3D) topology of Network-On-Chip (NoC) has become a promising way to solve the problem of IP core scale expansions. It offers greater device integration and also can provide higher-bandwidth, lower-latency and lower-consumption inter-layer communication with the help of through-silicon-vias (TSVs). However, the low yield of TSV and high overhead become a primary problems. In order to obtain better performance at relatively lower cost, this letter proposes a new 3D topology based-on Partial Overlapped Clusters (POC) for NoC, which reduces the number of routers and TSVs by sharing part of vertical links flexibly. We evaluate the proposed topology through performance analysis and simulations, the results demonstrate it can reduce the overhead distinctly and provide satisfactory performance.

Keywords: Network-on-Chip, 3D topology, through-silicon-via

Classification: Integrated circuits

References

- [1] M. Motoyoshi: Proc. IEEE **97** (2009) 43. DOI:10.1109/JPROC.2008.2007462
- [2] J. H. Wang, H. X. Gu and Y. T. Yang: IEICE Electron. Express **9** (2012) 1254. DOI:10.1587/elex.9.1254
- [3] B. S. Feero and P. P. Pande: IEEE Trans. Comput. **58** (2009) 32. DOI:10.1109/TC.2008.142
- [4] A. M. Rahmani and P. Likjeberg: Euromicro Int. Con. on PDP (2012) 507.
- [5] J. H. Lau: ECTC (2010) 1031. DOI:10.1109/ECTC.2010.5490828
- [6] L. Cheng, L. Zhang, Y. Han and X. Li: ASPDAC (2011) 357.
- [7] N. Viswannathan, K. Paramasivam and K. Somasundaram: IJPEDS **29** (2014) 346. DOI:10.1080/17445760.2013.866236
- [8] A. Kahng, B. Li, L. Peh and K. Samadi: IEEE Trans. VLSI Syst. **20** (2012) 191. DOI:10.1109/TVLSI.2010.2091686
- [9] W. Jang, O. He, J. Yang and D. Z. Pan: ICCAD (2011) 207. DOI:10.1109/ICCAD.2011.6105327

1 Introduction

With more and more IP cores integrated on a chip, two-dimensional topology become weaker for on-chip design due to the expanding of network size. 3D topology has been proposed as the most promising approach with the employment of TSV technology [1] to solve the problem of scale expansion. Topology determines the distribution and connection of the network nodes, which is a very significant aspect and should be taken into consideration. Unfortunately, TSV pads occupy crucial chip area and raise the complexity in wiring. In addition, the yield of 3D NoC declines sharply with the increasing manufacture density of TSV for the immature fabrication route. Therefore, it is essential to find an efficient method to reduce the number of TSV while providing satisfactory network performance.

Motivated by the cost efficiency and the yield of 3D chip, an efficient 3D topology based-on partial overlapped clusters (POC) for NoC is proposed in this letter, which achieves an optimal balanced point between performance and manufacturing cost with regard to network diameter, energy consumption and limited number of TSVs.

2 Related work

As the TSV has the characteristics of low yield [2], the design of 3D NoC topologies and the corresponding routing algorithm with limited number of TSVs are open problems. 3D mesh topology has the characteristics of lower latency of inter-layer communication, lower design complexity, regularity and symmetry layout. Thus, most existing three-dimensional topology of NoC adopt 3D mesh structure. However, due to the characteristic of low yield of TSV and all large radix of the routers is adopted, the manufacturing cost of 3D mesh increases dramatically with the number of IP cores. [3] proposed stacked mesh which adopts buses instead of TSVs in vertical direction. Cluster 3D mesh [2] can decrease the number of TSVs by sharing vertical TSV channel, and reduce the radix of router to 6 as well. However, both designs suffer from fierce competition in vertical direction, the performance degrades dramatically under a high network load. Several works have investigated the vertical interconnect based on the above topologies. An hybridization scheme for 3D NoC topology has been proposed in [4], which based on the stacked mesh and improved the architecture of bus. Vertical interconnect serialization technique [5] and the squeezing scheme [6] are also proposed to minimize the number of TSV, but they increase the design complexity and chip area due to adding a TSV arbiter module in router. [7] remove part of links and share vertical links to augment the yield of 3D topology and power consumption efficiency, but it's network performance become worse with the vertical links trimmed down to 75%.

3 Topology implementation

The more TSVs a topology adopted, the better performance it can achieved. However, the severe economic penalty caused by low yield of TSV should be reckoned with seriously. The POC topology we proposed applies a partial overlapped cluster scheme which optimize performance and economic benefit by flexibly sharing part of vertical links.

3.1 The POC topology

POC is a 3D topology that consists of several 2D layers. 2D layout of a single layer is presented in Fig. 1(a). There are two kinds of router, C-R (Cluster Router) and O-C-R (Overlapped Clusters Router), both of which adopt classical router architecture. Each C-R has 6 ports and each O-C-R has 7 ports. O-C-R is used to connect the IP cores into network. Considering the radix of the router, only two IP cores are connected to the O-C-R. C-R is used to connect four O-C-Rs in NorthEast, SouthEast, NorthWest, and SouthWest directions, and also the two adjacent C-Rs in the up and down layers. Each C-R along with four neighbor O-C-Rs, within a dashed box in Fig. 1(a), can be regarded as a cluster. The XYZ-coordinates is used after the rotation of 45 degrees in clockwise, as illustrated in Fig. 1(a). The address of each node is presented by three-dimensional coordinate (x, y, z) . The partial overlapped clusters is connected by the following rule: If there are N cores in a single 2D layer of POC, C-R(x, y, z) will be connected to $(x \pm 1, y, z)$ and $(x, y \pm 1, z)$, where $1 \leq x \leq \lceil \sqrt{N/2} \rceil + 1$, $1 \leq y \leq \lceil \sqrt{N/2} \rceil + 1$. For $2 \leq x \leq \lceil \sqrt{N/2} \rceil$, $2 \leq y \leq \lceil \sqrt{N/2} \rceil$, if $x < y$, the O-C-R(x, y, z) will be connected to $(x - 1, y, z)$, $(x + 2, y, z)$, $(x, y - 2, z)$ and $(x, y + 1, z)$, if $x > y$, it will be connected to $(x - 2, y, z)$, $(x + 1, y, z)$, $(x, y - 1, z)$ and $(x, y + 2, z)$.

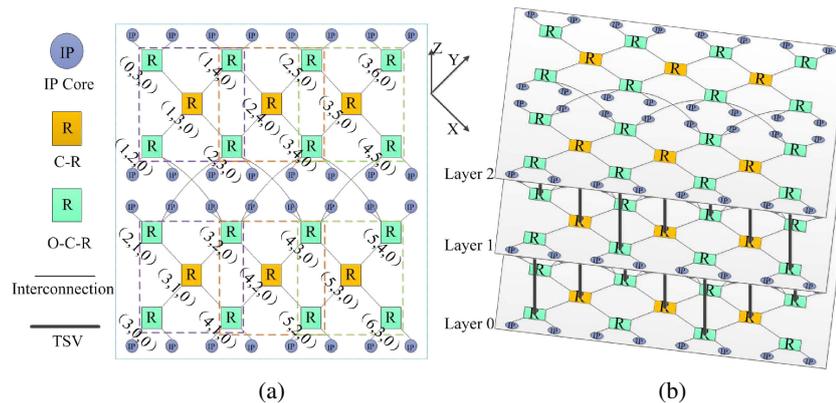


Fig. 1. Illustration of the 2D layout of POC topology (a) and 96 core POC topology (b)

When expanded to 3D topology, as described in Fig. 1(b), each 2D layer is stacked in vertical direction, and the inter-layer connection is implemented with TSVs. Each C-R connects its two neighbor C-R in the up and down layers. If $x + z$ is odd, the O-C-R(x, y, z) is connected to the O-C-R($x, y, z + 1$). Otherwise, the O-C-R(x, y, z) is connected to $(x, y, z - 1)$. Therefore, unlike 3D mesh which provides a dedicated vertical link, the POC topology shares vertical links between C-Rs and part of O-C-Rs. In this way, compared to 3D mesh with the same number of IP cores, the proposed topology can reduce the number of TSVs to 87.5% and consumes fewer interconnection links. In addition, for each edge H-V-R, there are three or four idle ports can be used for further expansion.

3.2 The routing algorithm

To ensure the communication efficiency of POC topology, we design an efficient routing algorithm. For intra-layer communication, the XY-routing and YX-routing are used to transfer packets. To avoid deadlock, we adopt five virtual channels to generate five virtual networks (VN_1 , VN_2 , VN_3 , VN_4 , and VN_5) to avoid circular dependency. In VN_1 , XY routing is allowed. In VN_2 , YX routing is allowed. In VN_3 and VN_4 , only YX and XY routing is allowed, respectively. The address of current and destination node is (x_c, y_c, z_c) and (x_d, y_d, z_d) , respectively. As we can see from Fig. 1(a), if a packet need to be delivered from (x_c, y_c, z) to (x_d, y_d, z) , there exist four situations.

Case one: ① $[(y_c = x_d) \text{ or } (x_c = y_d)] \& [(x_c + y_c) \bmod 2 \neq 0] \& [(y_c - y_d \geq 3) \text{ or } (y_d - y_c \geq 3) \text{ or } (x_c - x_d \geq 3) \text{ or } (x_d - x_c \geq 3)]$. ② $[(y_c = x_d) \text{ or } (x_c = y_d)] \& [(x_c + y_c) \bmod 2 = 0] \& [(y_c - y_d \geq 3) \text{ or } (y_d - y_c \geq 3) \text{ or } (x_c - x_d \geq 3) \text{ or } (x_d - x_c \geq 3) \text{ or } ((x_d = 2 \times x_c - y_c) \& (y_d = x_c))]$. ③ $[(y_c = x_d) \& (x_c = y_d)]$. If ① or ② or ③ is satisfied, packets are sent to the destination by combing XY with YX routing algorithm. If packets routed in XY-routing first then routed in YX-routing to reach the destination node will first be delivered to VN_1 and then VN_3 . Reversely, it will first be transmitted to VN_2 and then VN_4 .

Case two: If the source is $(\lceil \sqrt{N/2} \rceil - 1, \lceil \sqrt{N/2} \rceil + 2, z)$ or $(\lceil \sqrt{N/2} \rceil - 1, z)$, $(\lceil \sqrt{N/2} \rceil - 1, 0, z)$, and the destination is $(0, \lceil \sqrt{N/2} \rceil - 1, z)$ or $(\lceil \sqrt{N/2} \rceil + 2, \lceil \sqrt{N/2} \rceil - 1, z)$, YX, XY and YX turns are needed for packets to reach its destination. On this occasion, packets will be forwarded to VN_2 , VN_1 , and VN_3 .

Case three: If the source is $(0, \lceil \sqrt{N/2} \rceil - 1, z)$ or $(\lceil \sqrt{N/2} \rceil + 2, \lceil \sqrt{N/2} \rceil - 1, z)$, and the destination is $(\lceil \sqrt{N/2} \rceil - 1, \lceil \sqrt{N/2} \rceil + 2, z)$ or $(\lceil \sqrt{N/2} \rceil - 1, z)$, $(\lceil \sqrt{N/2} \rceil - 1, 0, z)$, packets are sent to its destination by XY, YX, and XY turns. In this situation, packets will be delivered to VN_1 , VN_3 , and VN_4 .

Case four: Only XY-routing or YX-routing is used to deliver packets to its destination for other nodes. If packets be sent to its destination only by XY-routing, it will be injected to VN_1 . Reversely, it will be injected to VN_2 .

In terms of inter-layer communication, we can combine ZXY with ZYX routing algorithm flexibly according to the position of the destination and source. Packets will be routed in Z-dimension before XY-routing or YX-routing if there exists the consistent vertical link connected to the destination layer. Otherwise, packets will be routed in Y-dimension or X-dimension to reach the neighbor C-R before it routed in Z-dimension. We define following rules to deal with all situations. In VN_5 , only XZ and YZ routing are allowed. ZY and ZX routing is allowed in VN_1 and VN_2 , respectively. Packets routed by ZXY-routing will be delivered to VN_2 and then VN_4 . Packets routed by ZYX-routing will be delivered to VN_1 and then VN_3 . Packets routed in the order of XZ, ZX, and XY will be injected to VN_5 , VN_2 , and VN_4 . Packets routed in the order of XZ, ZY, and YX will be injected to VN_5 , VN_1 , and VN_3 . Packets routed in the order of YZ, ZX, and XY will be injected to VN_5 , VN_2 , and VN_4 . Packets routed in the order of YZ, ZY, and YX will be injected to VN_5 , VN_1 , and VN_3 . There is no dependency in each virtual network and among these virtual networks. Hence, the proposed routing scheme is deadlock-free.

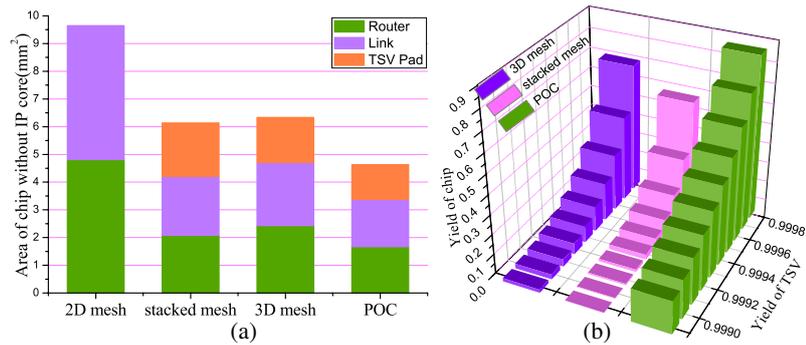


Fig. 2. The area (a), yield (b) of NoCs

4 Simulation results and performance analysis

In order to evaluate the performance of the POC 3D topology, we build an OPNET simulator to model 96-core NoC. To be fair, the 2D mesh, 3D mesh and stacked mesh are also simulated by OPNET with the same number of IP cores. The important simulation parameters configuration used for all the topologies are the same and which are listed as follows: the number of virtual channels in each input port is 5, the buffer depth is 5 flits, each packet size is 5 64-bits flits, and the operation frequency of router is 0.2 GHz. The costs of chip such as area, power, yield parameters are acquired from the Orion 2.0 [8] under the 65 nm technology parameter. The chip area includes router, link and TSV pad, as illustrated in Fig. 2(a). The area of TSV pad is acquired from the equation: $S_{pad} = P^2 \times N_{TSV}$ [9], where S_{pad} means the area of TSV pad, N_{TSV} implies the number of TSVs on each TSV bundle, P is obtained from TSV height variation. The result indicates that the area of POC has a significant advantage over the other NoCs with the same number of IP cores, which is decreased by 27.78% compared with 3D mesh. The primary reasons are that the overhead of TSV pads and routers have 43.75% and 37.04% reduction, respectively. Since the power consumed by 7×7 router is approximately 2 times more than that of 6×6 router and the number of routers are also reduced, the power of POC has been reduced by 46.41% of 3D mesh.

Fig. 2(b) shows the relationship between the yield of TSV and the yield of 3D chip. The amount of TSV will be a huge impact factor of 3D NoC until the yield of TSV is higher than 99.99%. The yield of TSV bundle is only determined by the amount of TSV it includes because the TSV height variations of point-to-point link and bus are equal. Hence, the yield of chip can be obtained from the equation: $Y_c = Y_b^{N_b \times (N_l - 1)}$, where Y_c means the yield of chip, $Y_b = Y_{TSV}^{N_{TSV}}$ suggests the yield of TSV bundle, Y_{TSV} denotes the yield of TSV, N_b express the number of TSV bundle in each layer and N_l means the number of layer [5]. The enhancement in 3D chip yield brought by eliminating the number of TSV is conspicuous.

The network throughput and end-to-end (ETE) delay performance of NoCs under uniform and hotspot traffic pattern are illustrated in Fig. 3, respectively. The ETE delay means the average time which packets consumed from the source node to the destination node. Throughput indicates the average number of packets that arrive at IP cores per clock cycle. For the uniform traffic, the POC 3D topology performs much better than 2D mesh and stacked mesh and its saturation point is

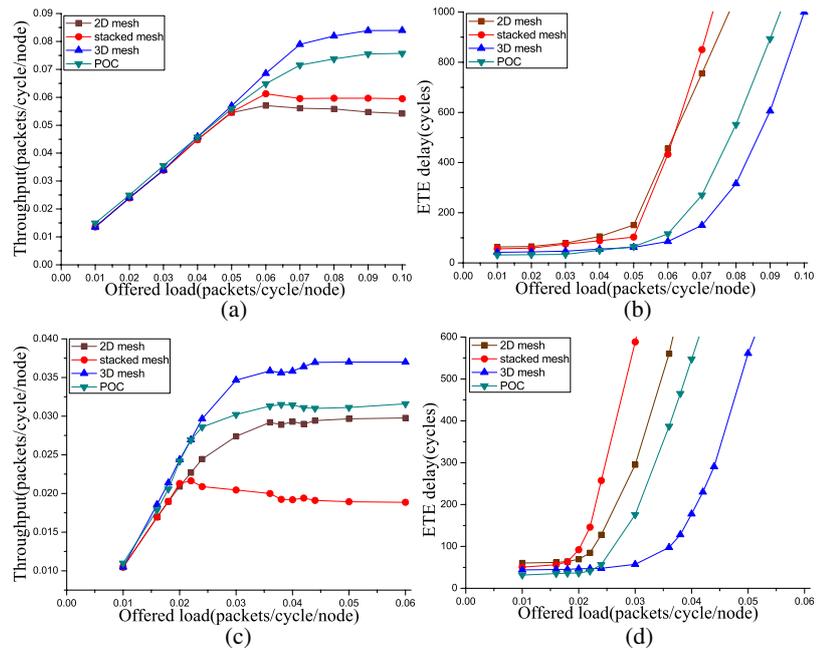


Fig. 3. Throughput and ETE delay under uniform (a), hotspot (b) traffic pattern.

approximately 90.72% of that of 3D mesh. As for the hotspot traffic, which is more closer to the real application, the saturation point of the POC 3D topology is about 82.69% of 3D mesh. These results reveal that the satisfactory performance is obtained.

5 Conclusion

A 3D topology based-on partial overlapped clusters is proposed in this paper. Unlike other 3D topologies, the POC topology can flexibly share part of vertical links by the staggered increasing of link in vertical direction and the structure of partial overlapped clusters, and a optimal balance between performance and manufacturing cost is also achieved at the same time. The simulation results reveal that the POC topology can reduce the overhead significantly and obtain satisfactory network performance.

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