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Tunable current-mode and voltage-mode quadrature oscillator using a DVCCTA

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Abstract: A novel tunable current-mode and voltage-mode quadrature oscillator design using a single differential voltage current conveyor transconductance amplifier (DVCCTA) and four all grounded passive elements is presented. The proposed circuit offers two explicit quadrature current outputs and two quadrature voltage outputs. The oscillation condition and oscillation frequency of the proposed oscillator are independently controllable. The use of only grounded passive components makes the proposed circuit ideal for integrated circuit implementation. HSPICE simulation results are given to verify the theoretical analysis.

Keywords: voltage-mode, current-mode, quadrature oscillator

Classification: Integrated circuits

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1 Introduction

Current-mode active building blocks have been receiving considerable attention owing to their larger dynamic range, greater linearity, wider bandwidth and low power consumption with respect to operational amplifier-based circuits [1]. Moreover, analogue signal processing in low supply voltages can be best accomplished in the current-mode and hence low voltage current-mode active building blocks operating in the current-mode and their applications are important in sinusoidal oscillators [2, 3, 4, 5, 6, 7]. In 2009, a new active building block for analogue signal processing, namely, differential voltage current conveyor transconductance amplifier (DVCCTA), was introduced [8]. DVCCTA device is obtained by cascading of the differential voltage current conveyor (DVCC) [6] with the operational transconductance amplifier (OTA) [7] in monolithic chip for compact implementation of analogue function circuits. As a result, DVCCTA has a transconductance stage at its back end and hence it provides the feature of electronic tuning to the circuit parameters, while also reducing the number of resistors by one. Recently, a voltage-mode DVCCTA-based quadrature sinusoidal oscillator is constructed in [9]. This circuit employs a single DVCCTA, two grounded capacitors and two grounded resistor and offers the advantages of (i) independent control of condition of oscillation (CO) and frequency of oscillation (FO), (ii) voltage-mode quadrature signals with 90° phase difference, and (iii) low active and passive sensitivities. In this paper, the authors also propose another electronically controllable DVCCTA-based quadrature sinusoidal oscillator. The proposed circuit has all of the advantages by Lahiri et al. [9] in addition to one more advantage of two explicit high-output impedance sinusoid currents with a 90° phase difference. Both current-mode and voltage-mode quadrature signals can be simultaneously obtained in the proposed circuit. Sinusoidal oscillators which produce both current-mode and voltage-mode quadrature signals are useful for their versatility. Since the proposed circuit consists of single DVCCTA and all grounded passive components thus it is more suitable for integrated circuit implementation.

2 Proposed current-mode and voltage-mode quadrature oscillator

DVCCTA is a versatile analogue active building block [8] and has received considerable attention as current-mode active element. The DVCCTA is based on DVCC [6] and consists of differential amplifier, current mirrors, and transconductance amplifier [7]. The symbolic representation of the DVCCTA is shown in Fig. 1(a). The terminal characteristics of the DVCCTA are give by $I_{Y1} = I_{Y2} = 0$, $V_X = V_{Y1} - V_{Y2}$, $I_{Z1+} = I_{Z2+} = I_X$, $I_{Z3-} = -I_X$, and $I_{O1} = I_{O2} = g_m V_{Z1+}$, where g_m is the transconductance gain from Z_1+ terminal to O_1 terminal of the DVCCTA [8]. The proposed current-mode and voltage-mode quadrature oscillator circuit is shown in Fig. 1(b) using a single DVCCTA, two grounded capacitors and two grounded resistors. The use of grounded capacitors and resistors is particularly attractive for inte-

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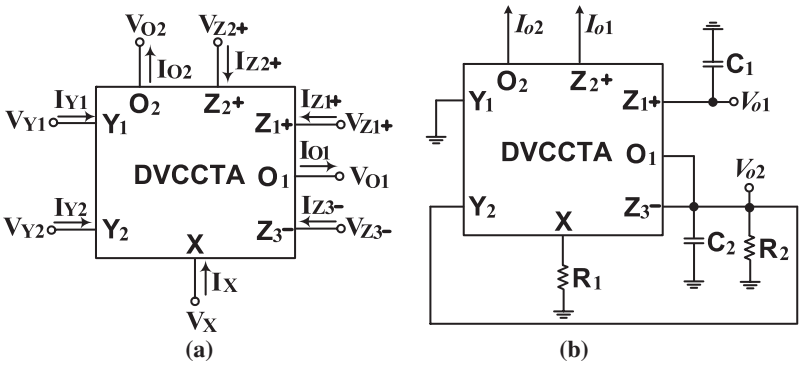

Fig. 1. (a) Schematic symbol of DVCCTA, (b) proposed DVCCTA-based quadrature oscillator.

grated circuit implementation. Routine analysis of the proposed oscillator circuit of Fig. 1(b) yields the following characteristic equation:

$$s^2 + \frac{s}{C_2}\left(\frac{1}{R_2} - \frac{1}{R_1}\right) + \frac{g_m}{C_1 C_2 R_1} = 0 \tag{1}$$

It is seen from (1) that the CO and the FO are given as

$$\text{CO:} \quad R_1 \leq R_2, \quad \text{FO:} \quad f_o = \frac{1}{2\pi}\sqrt{\frac{g_m}{C_1 C_2 R_1}} \tag{2}$$

As indicated by (2), the CO can be controlled independently of FO by changing R_2; the FO can be controlled by g_m and hence is current controllable by bias current I_B. From Fig. 1(b), under steady state, the relationships between output currents I_{o1} and I_{o2} are

$$I_{o2} = \frac{g_m}{\omega_o C_1} e^{-j90^\circ} I_{o1} \tag{3}$$

ensuring the currents I_{o2} and I_{o1} to be in quadrature. The relationships between output voltages V_{o1} and V_{o2} are

$$V_{o2} = \omega_o C_1 R_1 e^{-j90^\circ} V_{o1} \tag{4}$$

ensuring the voltages V_{o2} and V_{o1} to be in quadrature.

Clearly, the current-mode and voltage-mode quadrature signals can be simultaneously obtained from Fig. 1(b). Because the output impedances of the currents I_{o1} and I_{o2} in Fig. 1(b) are very high, the two output terminals, I_{o1} and I_{o2}, can be directly connected to the next stage.

3 Nonideality analysis and design considerations

By taking into account the nonidealities of the DVCCTA, the relationship of the terminal voltages and currents can be rewritten as $V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2}$, $I_{Z1+} = \alpha_1 I_X$, $I_{Z2+} = \alpha_2 I_X$, $I_{Z3-} = -\alpha_3 I_X$, $I_{O1} = \gamma_1 g_m V_{Z1+}$ and $I_{O2} = \gamma_2 g_m V_{Z1+}$, where α_1, α_2 and α_3 represent the current transfer gains from X terminal to Z_1+, Z_2+ and Z_3- terminals, respectively, and β_1 and β_2 represent the voltage transfer gains from Y_1 and Y_2 terminals to X terminal, respectively, and γ_1 and γ_2 represent the current transfer gains from Z_1+ terminal to O_1 and O_2 terminals, respectively. All of these parasitic volt-

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age/current gains differ from their ideal values of unity by voltage/current tracking errors. Taking into account the factors due to the nonidealities of the DVCCTA, the modified CO and the FO are given as

$$\text{CO:} \quad R_1 \leq \alpha_3\beta_2 R_2, \quad \text{FO:} \quad f_o = \frac{1}{2\pi}\sqrt{\frac{\alpha_1\beta_2\gamma_1 g_m}{C_1 C_2 R_1}} \tag{5}$$

The active and passive sensitivities of the quadrature oscillator parameters are shown as

$$S^{f_o}_{\alpha_1,\beta_2,\gamma_1} = S^{f_o}_{g_m} = -S^{f_o}_{C_1,C_2,R_1} = \frac{1}{2} \tag{6}$$

From (6), it is clearly observed that the circuit has low sensitivity performance in the sense that all values are equal to 0.5 in magnitude.

A study is next carried out on the effects of various parasitic of the DVCCTA used in the proposed circuit. A practical DVCCTA device can be modeled as ideal DVCCTA with finite parasitic resistances and capacitances. Fig. 2 shows the nonideal DVCCTA model including its parasitic elements. The non-zero parasitic input impedance at terminal X of the DVCCTA is represented by R_X. The parasitic resistance R_{Zi} $(i = 1, 2, 3)$ and parasitic capacitance C_{Zi} appear between the high-impedance Z_i terminals of the DVCCTA and grounded. The parasitic resistance R_{Oj} $(j = 1, 2)$ and parasitic capacitance C_{Oj} appear between the high-impedance O_j terminals of the DVCCTA and grounded. The X terminal of the DVCCTA in Fig. 1(b) is connected by external resistor R_1; accordingly, R_X is in series with R_1. Therefore, the effect of this parasitic resistance will be negligible because the value of R_X is much smaller than R_1. It is further noted that the proposed circuit employs external capacitors C_1 and C_2 parallel connecting at the terminals Z_1+ and Z_3-, respectively. As a result, the effects of the parasitic capacitances C_{Z1} and C_{Z3} can be absorbed, due to the fact that $C_1 \gg C_{Z1}$ and $C_2 \gg C_{Z3}, C_{O1}$. Hence, if the following conditions are satisfied:

$$R_2 \ll R_{Z3} \,/\!/\, R_{O1} \quad \text{and} \quad \frac{1}{sC_1} \ll R_{Z1} \tag{7}$$

then the influence of DVCCTA parasitic elements to the proposed oscillator of Fig. 1(b) can be ignored.

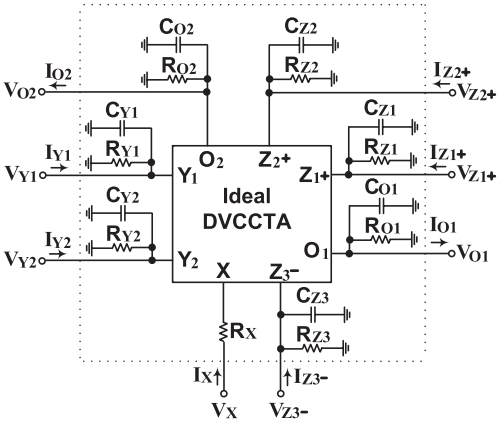

Fig. 2. Nonideal equivalent circuit model of DVCCTA.

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4 Simulation results

HSPICE simulations were performed using the CMOS realization of DVCCTA with TSMC 0.18 µm process MOSFET parameters. Fig. 3 represents the CMOS implementation of the DVCCTA as special case from the differential difference current conveyor transconductance amplifier by grounding the Y_3 terminal [10]. The aspect ratios (W/L) of the MOS transistors were taken as 8.75/0.35 for M1–M4; 17.5/0.18 for M5–M12; 8.75/0.18 for M13–M20; 10/0.5 for M21–M22; 25/0.8 for M23–M27; 8/0.8 for M28–M30. The supply voltages are $V_{DD} = -V_{SS} = 0.9\,\text{V}$, and the biasing voltage is $V_{BB} = -0.5\,\text{V}$. To obtain the sinusoidal output waveform with the oscillation frequency of $f_o \cong 3.183\,\text{MHz}$, the following component values have been chosen: $g_m \cong 200\,\mu\text{A/V}$ ($I_B = 96.5\,\mu\text{A}$), $R_1 = R_2 = 5\,\text{k}\Omega$ and $C_1 = C_2 = 10\,\text{pF}$, where $R_2 = 5.02\,\text{k}\Omega$ was designed to be larger than R_1 to ensure the oscillators would start. The steady state output waveforms for both the quadrature voltages and currents were shown in Figs. 4(a) and (b), respectively. The electronic tuning of the V_{o1} oscillation frequency with the bias current I_B for different capacitor values was shown in Fig. 5. These simulations results are close to the theoretical prediction and confirm the feasibility of the proposed configuration. The proposed sinusoidal oscillator has a simple topology and provides voltage-mode and current-mode operation with electronically tunable properties. The power dissipation is 2.283 mW.

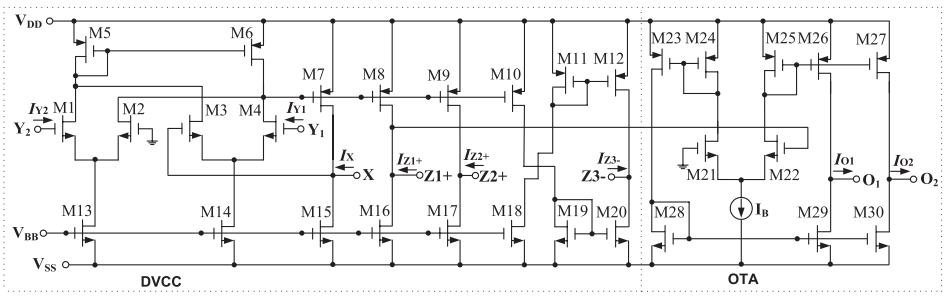
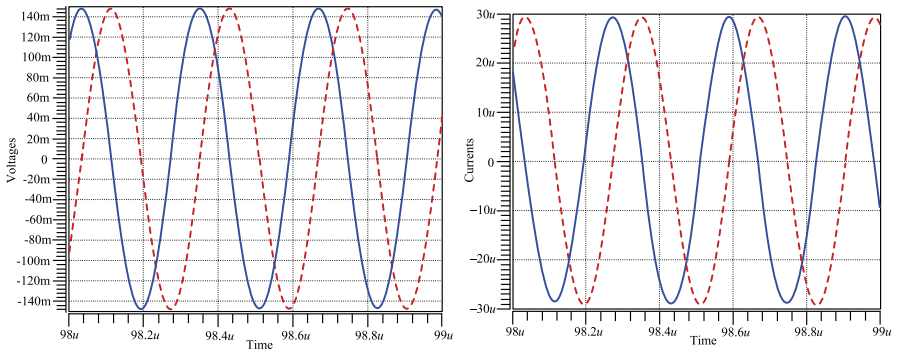


Fig. 3. CMOS implementation of DVCCTA.



(a) voltage waves of V_{o1} (blue) and V_{o2} (red) (b) current waves of I_{o1} (blue) and I_{o2} (red)

Fig. 4. Simulated quadrature outputs.

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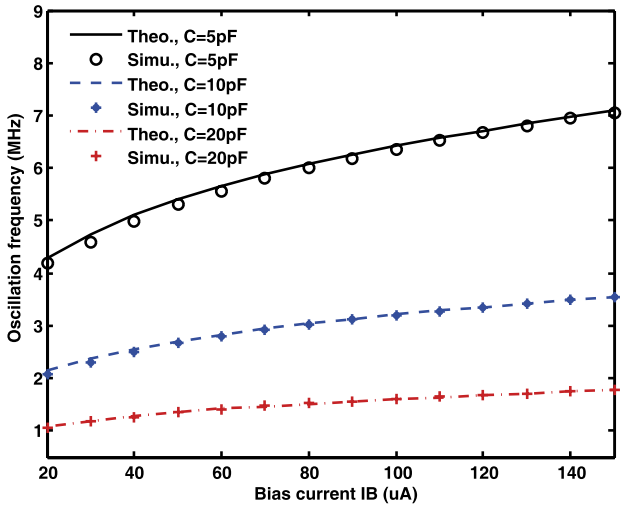

Fig. 5. Oscillation frequencies against bias current in the proposed circuit for various capacitances.

5 Conclusion

A new DVCCTA-based quadrature sinusoidal oscillator circuit is presented. The circuit employs single DVCCTA, two grounded resistors and two grounded capacitors. The current-mode and voltage-mode quadrature signals can be simultaneously obtained in the proposed circuit. The oscillation condition and oscillation frequency are independently controllable. The circuit provides two quadrature voltage signals with 90° phase difference. Besides the above stated advantages, the frequency of oscillation of the circuit is current controllable and moreover, the circuit provides two high-output impedance sinusoid currents with a 90° phase difference. The proposed circuit is an improvement over the previously reported voltage-mode DVCCTA-based oscillator [9]. HSPICE simulations with TSMC 0.18 µm process technology and ±0.9 V supply voltages confirm the theoretical predictions.

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