

A low supply voltage and wide-tuned CMOS Colpitts VCO

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Abstract: This paper presents a g_m -boosted differential Colpitts VCO with a switched capacitor tuning scheme which achieves low phase noise and a wide tuning range at a low supply voltage. In the proposed VCO, a voltage boosting circuit increases a turn-on resistance of the switching transistor for the capacitor array by generating higher gate bias voltage. As a result, the proposed VCO can achieve a wide frequency tuning range at a low supply voltage. The proposed VCO is implemented with 0.18- μm CMOS technology and oscillates from 3.60 to 4.14 GHz. Measurement results indicate a phase noise of -123.65 dBc/Hz at 1-MHz offset at 3.63 GHz, while dissipating 2.53 mA from the 0.7-V supply.

Keywords: Colpitts, differential, low supply, voltage controlled oscillator, frequency tuning range

Classification: Integrated circuits

References

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1 Introduction

Due to the requirements of low-cost and small chip area, CMOS technology has been scaled down to the level of deep sub-microns. As the feature size of the transistor has been reduced, a supply voltage has been also decreased to prevent velocity saturation and device breakdown from the high field. Many communication systems become fully integrated with this scaled CMOS technology. A voltage-controlled oscillator (VCO), which is a critical building block in wireless communication systems, also needs to be designed at a low supply voltage in the deep sub-micron CMOS process. However, the low

supply voltage results in a narrower frequency tuning range of the VCO by decreasing the tuning range of the control voltage of a MOS varactor. Several VCO topologies have been studied to obtain the low phase noise and the wide frequency tuning range at a low supply voltage [1, 2, 3, 4]. Among those designs, a switched capacitor array scheme has been widely adopted due to its low VCO gain and wide tuning range characteristics [4]. However, as the supply voltage is decreased, a turn-on resistance of the switching transistor in the switched capacitor array significantly is increased, and then degrades a quality-factor of an LC-tank. This paper analyzes the turn-on resistance effect of the switching transistor in the switched capacitor array. A newly proposed VCO, which consists of the g_m -boosted differential Colpitts VCO and the switched capacitor array with the voltage boosting circuit, is presented to achieve simultaneously the low phase noise and the wide tuning range.

2 Proposed VCO design

Fig. 1 shows the schematic of the proposed VCO, which consists of the g_m -boosted differential Colpitts structure and the 2-bit switched capacitor array with the voltage-boosting circuit. In the proposed VCO shown in Fig. 1, M_{bias} , M_{g_m} and M_{sw} are the current source, g_m -boosting and switching transistors, respectively [1]. Since the overall negative conductance of the g_m -boosted differential Colpitts VCO is increased, the start-up current power dissipation of the VCO can be reduced, compared to those of the conventional Colpitts VCO. In addition, the g_m -boosted differential Colpitts VCO shows good phase noise performance by keeping the switching transistor (M_{sw}) in the saturation region even at the large oscillation amplitude [1].

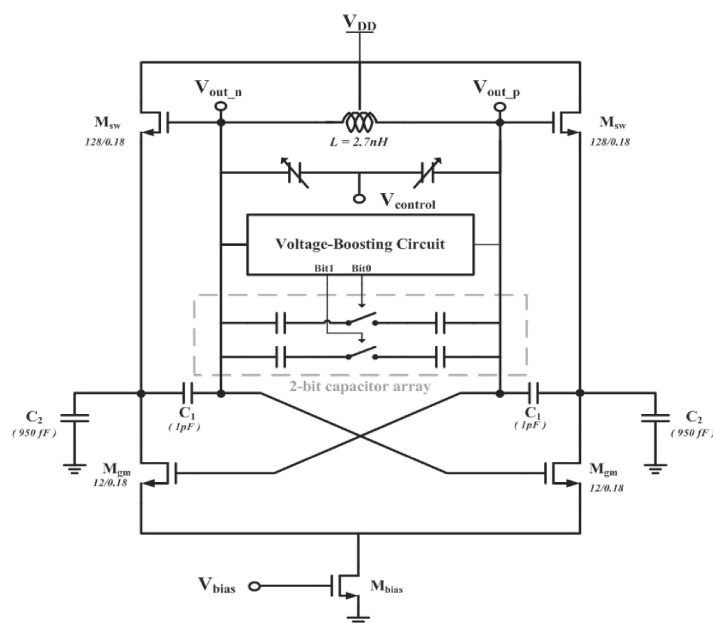


Fig. 1. Proposed g_m -boosted differential Colpitts VCO with voltage boosting circuit

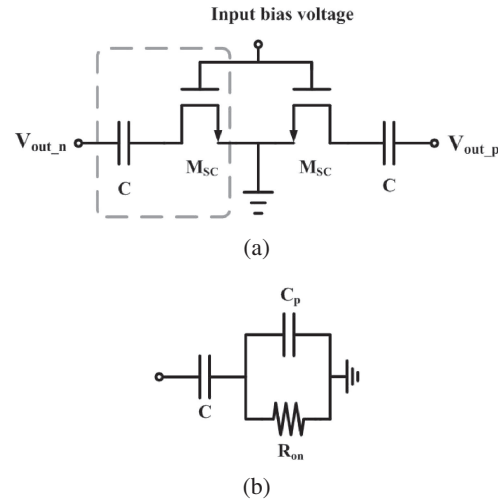


Fig. 2. (a) Switched capacitor and (b) its equivalent half circuit

Fig. 2 shows the switched capacitor array and its equivalent half circuit. In Fig. 2, C is a desired capacitance of the switched capacitor and C_p and R_{on} are the parasitic capacitance and turn-on resistance of the switching transistor (M_{sc}), respectively. The impedance of the equivalent half circuit shown in Fig. 2(b) is given by

$$Z_{real} = \frac{\omega^2 C^2 R_{on}}{\omega^4 C^2 C_p^2 R_{on}^2 + \omega^2 C^2} \quad (1)$$

$$Z_{imag} = -\frac{\omega^2 R_{on}^2 C_p (C_p + C) + 1}{\omega^3 C C_p^2 R_{on}^2 + \omega C} \quad (2)$$

where Z_{real} and Z_{imag} are the real and imaginary impedance of the switched capacitor, respectively. As can be seen from equation (1), the effective resistance is generated from switching transistor (M_{sc}) in the switched capacitor and it degrades the quality-factor of the LC-tank. From equation (2), when R_{on} is zero, Z_{imag} becomes the desired capacitance value, $1/\omega C$. However, when R_{on} is non-zero, the magnitude of Z_{imag} is decreased. Assuming that R_{on} is much larger than ωC , Z_{imag} is shown to be a series connection between capacitance C and C_p . As a result, the effective capacitance value of equation (2) is reduced and it leads to a narrower frequency tuning range of VCO, compared to that of the desired value. Furthermore, this effect becomes more significant when the oscillation frequency, ω , is higher, and an input bias voltage of the switching transistor is lower.

For improvement of the turn-on resistance, the proposed VCO adopts the voltage boosting circuit at the switched capacitor array. Fig. 3 shows a 2-bit switched capacitor array with a voltage boosting circuit [3]. The voltage-boosting circuit consists of two PMOS transistors (M_{B1} and M_{B2}) and two voltage charging capacitors (C_{B1} , C_{B2}). The source terminal of the PMOS transistors connects to the differential output of the VCO with capacitor array, and the gate terminal connects to the source node of the opposite PMOS transistor. The voltage charging capacitor is connected to the drain node of the PMOS transistor. In the voltage boosting circuit, the peak voltage

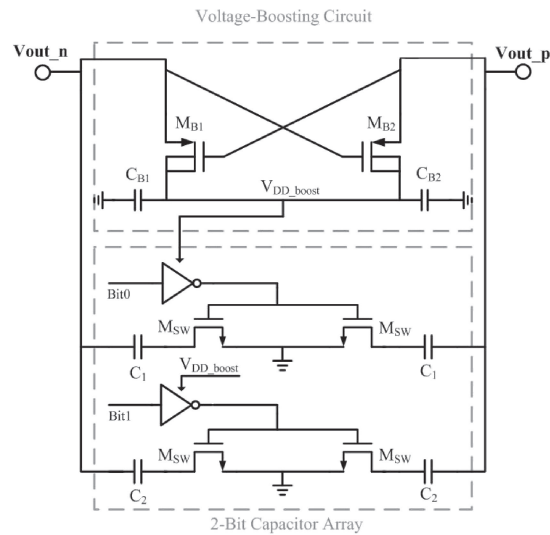


Fig. 3. Proposed 2-bit capacitor array with voltage boosting circuit

of the VCO output can be stored in the charging capacitors (C_{B1} and C_{B2}) through PMOS transistors. Ideally, the maximal peak voltage of the g_m -boosted differential Colpitts VCO can reach twice the level of the supply voltage V_{DD} . Eventually, the boosted voltage, $V_{DD,boost}$, is used by the gate bias voltage of the switching transistor (M_{SW}).

Since the boosted gate input voltage decreases the turn-on resistance of the switching transistor, the quality-factor of the LC-tank is improved and the effective capacitance of the switched capacitor array is less decreased. As a result, the proposed VCO with the voltage boosting circuit achieves better phase noise performance and a wider frequency tuning range, compared to those of the conventional VCO.

3 Simulation and measurement results

Fig. 4 shows the simulation result of the effective capacitance variation in the switched capacitor by the input bias voltage. From Fig. 4, as the input bias

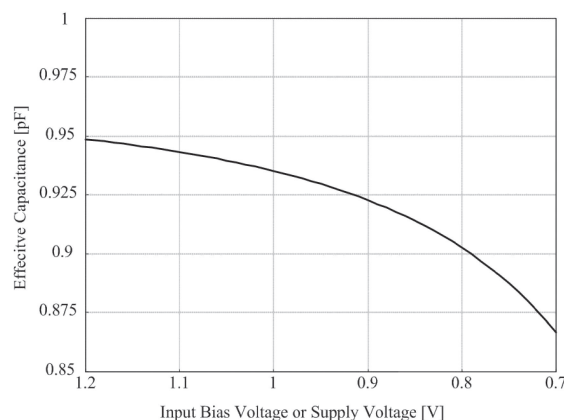


Fig. 4. Simulated effective capacitance variation by input bias voltage

voltage decreases, the effective capacitance of the switched capacitor is significantly reduced from the ideal value of 1 pF.

Fig. 5 shows the simulated effective capacitance variation of the switched capacitor for no switch (ideal capacitance), with a voltage-boosting circuit, and without a voltage boosting circuit, and at 0.7-V supply voltage. As can be seen in Fig. 5, the effective capacitance without a voltage boosting circuit is smaller than the ideal capacitance, and it decreases as the oscillation frequency is higher. On the other hand, the discrepancy between the effective capacitance with the voltage boosting circuit and ideal capacitance is much smaller than that of the case without voltage boosting.

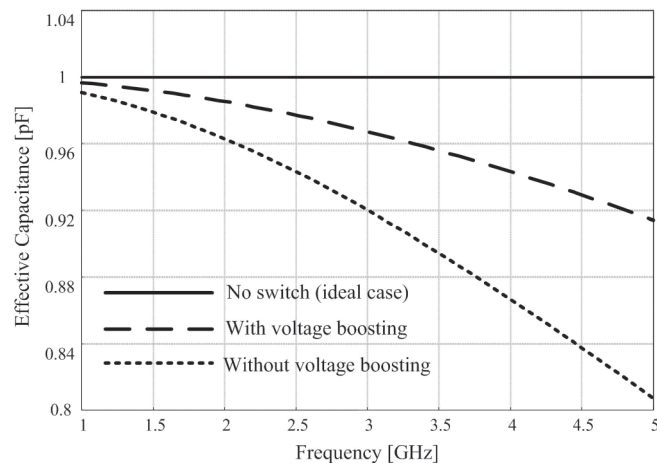


Fig. 5. Simulated effective capacitance versus oscillation frequency

The decrease in the effective capacitance of the switched capacitor leads to a narrower frequency tuning range of the VCO. From the simulation result, the VCO with a voltage boosting circuit oscillates from 3.60~4.14 GHz, while the VCO without a voltage boosting circuit oscillates from 3.76~4.20 GHz at 0.7-V supply. Even though the oscillation frequency is lower, the VCO with voltage boosting circuit achieves almost a 25% (100 MHz) wider frequency tuning range than that of the VCO without a voltage boosting circuit.

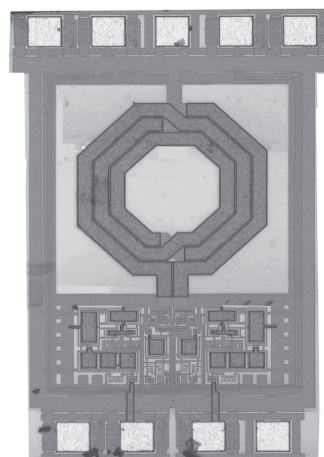


Fig. 6. Chip photograph of the proposed VCO

The proposed VCO has been fabricated by using 0.18- μm CMOS technology. The measured oscillation frequency of the VCO varies from 3.60 to 4.14 GHz over the control voltage of 0 to 0.7-V. Fig. 6 shows the fabricated chip photograph of the proposed VCO with a size of $800 \times 700 \mu\text{m}^2$. Fig. 7 is the measured phase noise of the proposed VCO. The measured phase noise shows -99.87 and -123.65 dBc/Hz at 100-kHz and 1-MHz offset frequency, respectively at 3.63 GHz, while dissipating a total current of 2.53 mA from a 0.7-V supply. These results match well with simulation.

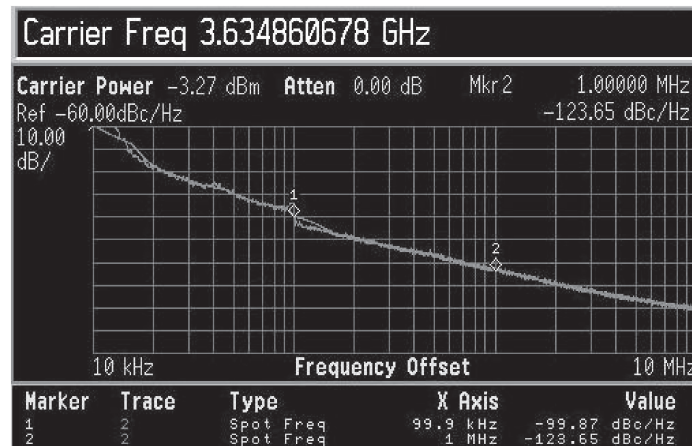


Fig. 7. Measured phase noise of the proposed VCO.

4 Conclusion

This work presents a newly proposed VCO with a wide tuning range and low phase noise at a low power supply. By adopting the g_m -boosted differential Colpitts topology, the proposed VCO can achieve small start-up current and good phase noise performance. In addition, the voltage boosting circuit for the switched capacitor array improves degradation of the frequency tuning range at a low supply voltage. The proposed g_m -boosted differential Colpitts VCO with voltage boosting circuit is implemented in 0.18- μm CMOS for 3.60~4.14 GHz operation. The measured phase noise shows -99.87 and -123.65 dBc/Hz at 100-kHz and 1-MHz offset frequency, respectively at 3.63 GHz. The proposed VCO dissipates a total current of 2.53 mA from a 0.7-V supply.

Acknowledgments

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