ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.9, No.23, 1807-1812

A true single-phase clocked flip-flop with leakage current compensation

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Abstract: A true single-phase clocked (TSPC) flip-flop, which compensates for the leakage current generated at dynamic nodes, is proposed to cover a wide operational frequency range in submicron CMOS processes. To implement the proposed TSPC flip-flop, three feedback circuits composed of a gated inverter (GI) are added to the conventional TSPC flip-flop. The GI is controlled by a clock and the internal signal of the conventional flip-flop, without an external control signal or a complementary clock signal. Furthermore, the strength ratio of the normal path to the feedback path does not need to be considered for the proposed TSPC flip-flop since the feedback circuit is only enabled when the dynamic node acquires a floating state. The proposed TSPC flip-flop is designed using a 1-poly 6-metal 65 nm CMOS process with a 1 V supply voltage. The simulation results show that the proposed TSPC flip-flop, which is optimized for normal operation at an operational frequency of 2 GHz, exhibits an error-free operation at low operational frequencies such as 1 MHz. The three added feedback circuits increase the power consumption by 8.8% as compared to that of the conventional TSPC flip-flop and occupy 12.28% of the proposed flip-flop.

Keywords: true single-phase clocked flip-flop, leakage current

Classification: Integrated circuits

References

[1] Y. Ji-Ren, I. Karlsson, and C. Svensson, "A true single phase clock dynamic CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 22, no. 5, pp. 899–901, Oct. 1987.

[2] Y.-T. Hwang and J.-F. Lin, "Low Voltage and Low Power Divide-By-2/3 Counter Design Using Pass Transistor Logic Circuit Technique," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 9, pp. 1738–1742, Sept. 2012.

[3] M. Hansson and A. Alvandpour, "A Leakage Compensation Technique for Dynamic Latches and Flip-Flops in Nano-Scale CMOS," *IEEE Int. SOC Conf.*, pp. 83–84, Sept. 2006.

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DOI: 10.1587/elex.9.1807
Received October 24, 2012
Accepted November 22, 2012
Published December 12, 2012

1. Introduction

A flip-flop is a critical circuit in all synchronous VLSI designs, including high-performance microprocessors. Flip-flops are required to cover a wide operational frequency range, which includes a standby mode for mobile applications. Among many flip-flop architectures, a true single-phase clocked (TSPC) flip-flop, which consists of a dynamic circuit, has been utilized for high speed-operation [1, 2]. A TSPC flip-flop has a small area and a low clock power. However, dynamic circuits such as a TSPC flip-flop are susceptible to noise and leakage, which causes a serious problem in the submicron CMOS process operating at a low supply voltage. Thus, the utilization of theses dynamic circuits in applications with high-speed operation is limited.

Fig. 1 shows the block and timing diagrams of a conventional TSPC flip-flop. This flip-flop is operated using only a one-phase clock signal, without a complementary clock signal. Thus, it has a simple architecture and fast operation. However, nodes A, B, and C in Fig. 1(a) are dynamic nodes with floating traps. That is, node A is in the floating state when the CLK signal is high and signal D is low. Further, nodes B and C would be in the floating state according to the state of the previous nodes, as shown in Fig. 1(b). In the high-frequency operation, the data stored in the dynamic nodes of a TSPC flip-flop can be maintained owing to the parasitic capacitor of metal lines and the junction capacitor of transistors. On the other hand, the charge loss stored in the dynamic nodes can be generated during the low-frequency operation. Thus, a TSPC flip-flop is required to compensate for the leakage current generated at the dynamic nodes to cover a wide operational frequency range in submicron CMOS processes.

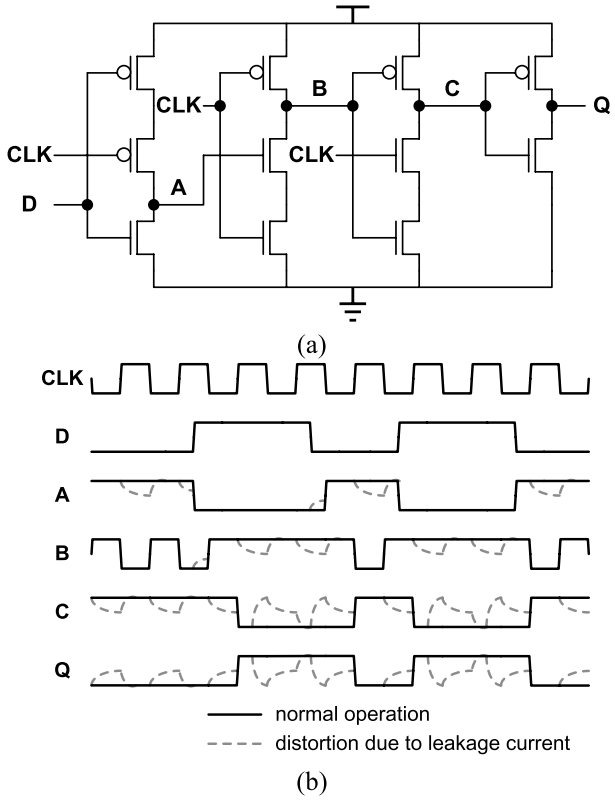


Fig. 1. Conventional TSPC flip-flop (a) circuit diagram (b) timing diagram

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DOI: 10.1587/elex.9.1807
Received October 24, 2012
Accepted November 22, 2012
Published December 12, 2012

The leakage compensation technique reported in the literature [3] was used for a dynamic flip-flop composed of transmission gates. A conditional static keeper added to the conventional transmission gate flip-flop enables low-frequency operation. However, the operation of this flip-flop is controlled by the external control signal according to the static and the dynamic modes. Furthermore, the strength ratio of the keeper circuit for the feedback path to the inverter for the normal path in this flip-flop affects the performances such as the operational frequency, setup time, hold time, and clock-to-output delay time. This disadvantage is attributed to the fact that the abovementioned circuits are enabled simultaneously. Thus, the minimum clock frequency required by this flip-flop is determined by the size ratio of the circuits of the two paths. This paper proposes a TSPC flip-flop that compensates for the leakage current to cover a wide operational frequency range in submicron CMOS processes. Three feedback circuits composed of a gated inverter (GI) are incorporated into the conventional TSPC flip-flop. The GI is controlled by a clock and the internal signal of the conventional flip-flop, without an external control signal and a complementary clock signal. Furthermore, the proposed TSPC flip-flop does not suffer from the abovementioned drawback of the strength ratio of the feedback circuit to the normal circuit. Section 2 describes the proposed TSPC flip-flop. The implementation and simulation results of the proposed TSPC flip-flop are discussed in section 3. Finally, section 4 presents the conclusion of this study.

2. Proposed true single-phase clocked flip-flop

Fig. 2 shows the circuit diagram of the proposed TSPC flip-flop, which compensates for the leakage current generated at the dynamic node. Three feedback circuits composed of a GI are added to the conventional TSPC flip-flop. Each GI has an equivalent architecture. Further, each GI is composed of two PMOS transistors and two NMOS transistors, and these four transistors are connected in series, as shown in Fig. 2. In the case of the first GI (*GI1*) circuit, shown in Fig. 2, the NMOS and PMOS transistors located in the center (*MCP0* and *MCN0*) are operated as an inverter. The upper PMOS and lower NMOS transistors (*MCP1* and *MCN1*) are used to control the activation of the inverter.

As shown in Fig. 1(b), node *A* becomes a dynamic node when the *CLK* signal is high and signal *D* is low. In this case, two transistors of the *GI1*

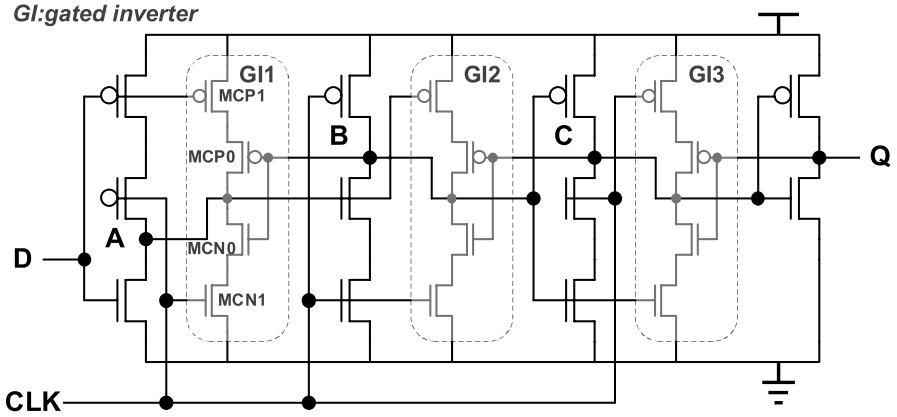


Fig. 2. Circuit diagram of proposed TSPC flip-flop

© IEICE 2012
DOI: 10.1587/elex.9.1807
Received October 24, 2012
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circuit (*MCP1* and *MCN1*), shown in Fig. 2, are enabled, and the output signal of the *GI1* circuit, which is inversed from signal *B*, is supplied to node *A*. Thus, node *A* becomes a static node owing to the *GI1* circuit. Consequentially, the *GI1* operates as a keeper circuit to compensate for the leakage current generated at the dynamic node *A*. Similarly, the leakage current generated at the remaining dynamic nodes, i.e. nodes *B* and *C*, is also compensated for by the *GI2* and the *GI3*, respectively.

Contrary to the leakage compensation technique reported in the literature [3], the proposed TSPC flip-flop does not suffer from the drawback generated by the strength ratio of the normal path to the feedback path, although the feedback path is enabled to compensate for the leakage current generated at the dynamic node. This is because each feedback circuit is enabled only when each dynamic node acquires a floating state. Thus, the transistor size of the circuits composed of *GI1*, *GI2*, and *GI3* for the feedback path is independent of that of the circuit for the normal path. Thus, the proposed TSPC does not require a design guide for the size ratio of the circuits of the two paths or the limitation of the operational frequency. In this study, the feedback circuits composed of *GI1*, *GI2*, and *GI3* use transistors with a minimum size to increase the operational frequency by reducing the parasitic capacitance and minimize the area added by the proposed scheme. Furthermore, the feedback circuit, GI, in the proposed TSPC flip-flop is controlled by a clock signal and an internal signal of the conventional flip-flop, without an external control signal and a complementary clock signal. Thus, an additional control for the operation of the TSPC is not needed according to the static and the dynamic modes.

3. Implementation and simulation results

To verify the proposed leakage current compensation scheme for the TSPC flip-flop, the conventional and proposed TSPC flip-flops were designed using a 1-poly 6-metal 65 nm CMOS process with a 1 V supply voltage. The area of the designed flip-flop was $11.25 \times 4.32\,\mu m^2$. The area added by the proposed scheme occupied 12.28% of the proposed flip-flop, as shown in Fig. 3.

The designed TSPC flip-flops were optimized for normal operation at an

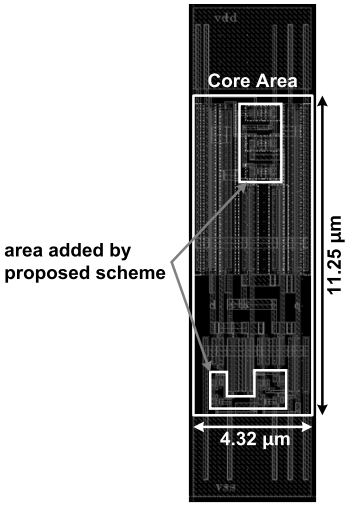


Fig. 3. Layout of proposed TSPC F-F

© IEICE 2012
DOI: 10.1587/elex.9.1807
Received October 24, 2012
Accepted November 22, 2012
Published December 12, 2012

operational frequency of 2 GHz to cover wide operational frequency ranges. Figs. 4(a) and (b) show the simulation results of the conventional and proposed TSPC flip-flops. The waveforms of each node of the two TSPC flip-flops are almost equal at the operation frequency of 2 GHz, as shown in Fig. 4(a). The dotted line and the solid line represent the waveforms of the conventional and proposed TSPC flip-flops, respectively. Thus, the performance of two TSPC flip-flops is similar. Fig. 4(b) shows the operation of the two flip-flops at an operational frequency of 1 MHz. In the case of the

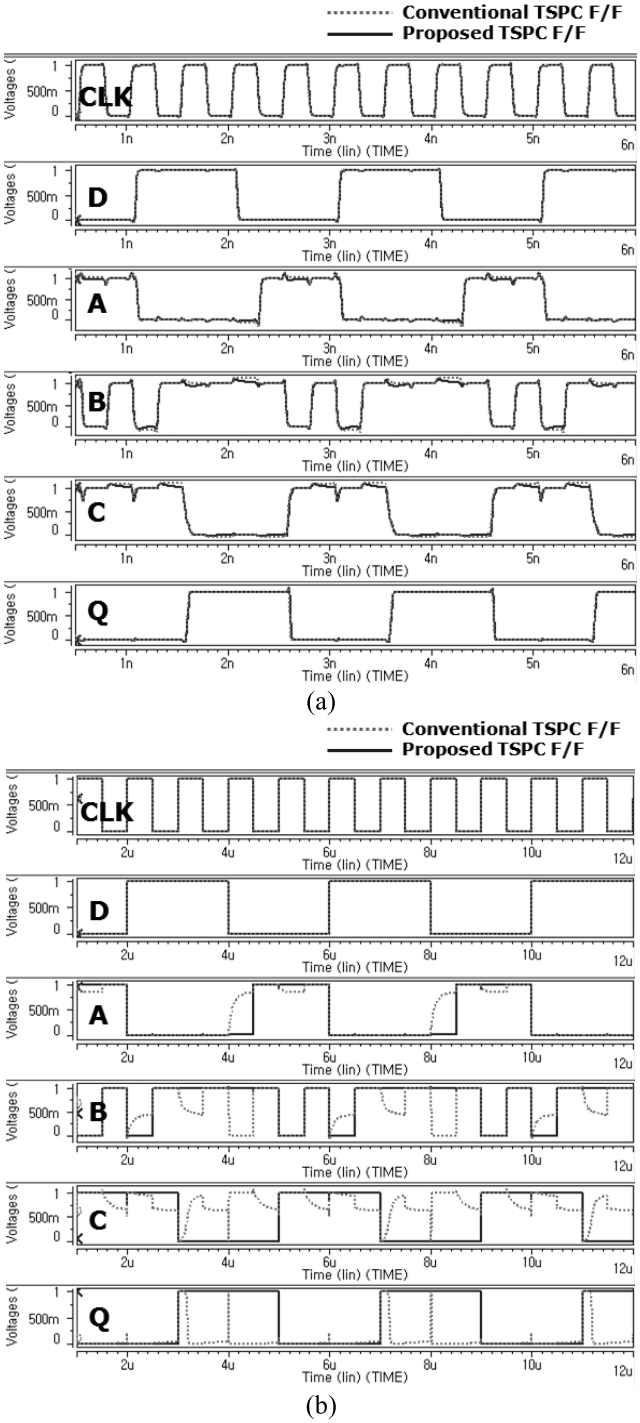


Fig. 4. Simulation results of conventional TSPC F-F and proposed TSPC F-F (a) operation at the frequency of 2 GH (b) operation at the frequency of 1 MH

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DOI: 10.1587/elex.9.1807
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conventional TSPC flip-flop, the leakage current generated at the dynamic nodes such as nodes *A*, *B*, and *C* causes the error function in the flip-flop operation. However, the proposed TSPC flip-flop exhibits an error-free operation at a low operational frequency of 1 MHz. This is because the floating state of the dynamic nodes is removed using the proposed feedback circuit composed of three GIs.

Table I is a comparison between the performance of the conventional and proposed TSPC flip-flops at the frequency of 2 GHz. The setup time, hold time, clock-to-output delay time (clock-to-Q delay time), and power consumption of the TSPC flip-flops are compared and analyzed. The setup time and delay time of clock to output of two flip-flops are similar each other. The hold time of the proposed flip-flop at the typical corner (TT) is increased by 9 ps as compared to those of the conventional TSPC flip-flop. The three added feedback circuits increase the power consumption by 8.8% as compared to that of the conventional TSPC flip-flop.

Table I . Performance comparison of TSPC F-F

Item	Conventional TSPC F-F			Proposed TSPC F-F		
	TT	FF	SS	TT	FF	SS
Setup time	-8ps	-7ps	-9ps	-5ps	-5ps	-6ps
Hold time	29ps	26ps	32ps	38ps	34ps	41ps
Clock to Q delay time	55.6ps	43.1ps	69.2ps	57.8ps	44.9ps	72.0ps
Power consumption	23.9uW	25.0uW	22.2uW	26.0uW	27.3uW	25.6uW

4. Conclusion

A TSPC flip-flop using three feedback circuits was proposed to compensate for the leakage current generated at the dynamic nodes in a submicron CMOS process. Each feedback circuit composed of a GI is controlled by a clock and an internal signal, without an external control signal or a complementary clock signal. The proposed TSPC flip-flop does not suffer from the drawback generated by the strength ratio of the normal path to the feedback path. The proposed TSPC flip-flop was designed using a 1-poly 6-metal 65 nm CMOS process with a 1 V supply voltage. The simulation results show that the proposed TSPC flip-flop, which is optimized for normal operation at an operational frequency of 2 GHz, exhibits an error-free operation at low operational frequencies such as 1 MHz. The setup time, hold time, and clock-to-output delay time of the proposed TSPC flip-flop is similar to those of the conventional TSPC flip-flop. The three added feedback circuits increase the power consumption by 8.8% as compared to the conventional TSPC flip-flop. The area added by the proposed scheme occupied 12.28% of the proposed flip-flop.

Acknowledgments

This paper was supported by Research Fund, Kumoh National Institute of Technology.

© IEICE 2012
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Accepted November 22, 2012
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