

SEU hardened layout design for SRAM cells based on SEU reversal

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Abstract: In this paper, the generation mechanism of single event upset reversal (SEUR) between 2 PMOS in SRAM cells is studied in depth based on 45 nm CMOS technology. We find that SEUR not only depends on the charge sharing but also follows the rule that the charge collection of passive device is larger and longer than that of active device. Based on SEUR generation mechanism, two novel layouts named Drain-Source-Drain (DSD) and Dummy are proposed to increase the rate of SEUR for reducing SEU vulnerability of SRAM cells. Compared with the traditional layout, DSD and Dummy layout reduce 4.26% and 31.56% SEU sensitive area under normal incident, respectively. For tilted incident, Dummy layout sharply increases SEUR rate while DSD layout is not better than the traditional layout on enhancing SEUR. Consequently, the proposed Dummy layout can improve SEU reliability without area penalty.

Keywords: SRAM cells, single event upset (SEU), charge sharing, single event upset reversal (SEUR), layout hardened design

Classification: Electron devices, circuits, and systems

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1 Introduction

The area rate of static random access memory (SRAM) in advanced integrated circuits (ICs) becomes larger and larger [1, 2]. However, the device size and the supply voltage scale with the technology progress, which decrease the critical charge and increase the rate of single event upset (SEU). Thus, the soft error in SRAM cells produced by advanced technologies becomes more and more seriously in radiation environments [3].

Moreover, the scaled space between the adjacent devices makes the charge sharing more serious. The serious charge sharing results in multi cells upset (MCU) and makes the existing hardened designs, such as Dual Interlocked Storage Cell (DICE), Triple Modular Redundancy (TMR) and C-element, become vulnerable to soft errors [4, 5, 6]. Although some researchers try to mitigate MCU, it is hard to restrain MCU without large area and time overhead [7].

On the other hand, the severe charge sharing between adjacent devices brings the new radiation characteristic for SRAM cells. The research of Ref. [8] and [9] shows that SRAM cell can reverse to initial state based on charge sharing after SEU happening. This new mechanism is called single event upset reversal (SEUR). Furthermore, Ref. [8] studied SEUR between 2 NMOS and Ref. [9] studied SEUR between 2 PMOS in a SRAM cell by using three-dimensional (3D) mixed-mode Technology Computer Aided Design (TCAD). Then, a novel layout is invented to mitigate SEU by utilizing generation mechanism of SEUR [10].

In this paper, we analyze SEUR mechanism between 2 PMOS in SRAM cells based on the 40 nm CMOS technology by using 3D mixed-mode TCAD once again. We find that the generation of SEUR not only bases on the charge sharing but also complies with the rule that the charge collection of passive device is larger and longer than that of active device. Then, we propose 2 new kinds of layout strategies based on SEUR between 2 PMOS to increase SEU reliability. In order to verify the validity, we compare SEU sensitive area of these 2 proposed layouts with that of traditional layout at normal incident. Then we get the threshold angle and threshold LET of SEUR at titled incident for these 3 layouts. The comparison results prove that one of the proposed layout strategies can decrease SEU sensitivity for SRAM cells.

2 Analysis of SEUR mechanism

SEUR happens in a SRAM cell due to the charge sharing between the active device (i.e. the device directly hit by particles) and the passive device (i.e. the adjacent device in the back of active device in logic). SEUR is similar to the quenching effect which can quench SET in the logic circuit [11]. The process of SEUR is described as follows: after the active device triggering the first upset, the passive device changes its state to OFF and then collects the deposited charge to trigger the second upset. The superposition of 2 upsets makes the SRAM cell reverse to its initial state.

We contrast a 3D TCAD model for 2 PMOS in a SRAM cell under 40 nm CMOS technology, and the remainder transistors of a SRAM cell are replaced by SPICE models, as shown in Fig. 1(a). The size of each transistor, the doping profiles of the 3D device models and the TCAD setups are the same to our previous works [12].

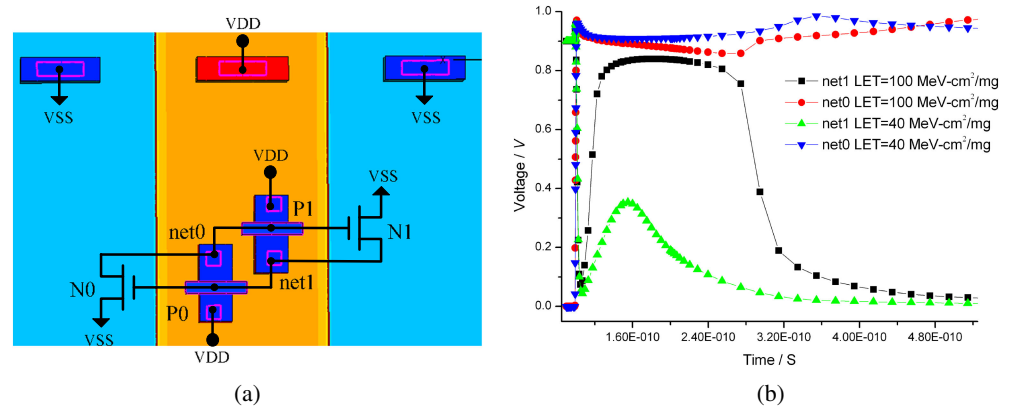


Fig. 1. (a) Schematic of a SRAM circuit with 2 PMOS in 3D TCAD model and 2 NMOS in SPICE model, and (b) voltage pluses of net0 and net1 at LET = 40 MeV·cm²/mg and LET = 100 MeV·cm²/mg.

The circuit is simulated in an initial state with net0 being LOW and net1 being HIGH, which results in P0 being OFF state and P1 being ON state. According to Ref. [9], striking the center of OFF PMOS drain is the easiest way to trigger SEUR. Thus, we simulate the particles striking the center of P0 drain with LET = 40 MeV·cm²/mg and LET = 100 MeV·cm²/mg, respectively. The simulation results are shown in Fig. 1(b), and it is clear that SEUR does not occur in all simulation results. When LET is 100 MeV·cm²/mg, both net0 and net1 become HIGH, and it makes SRAM cell enter into the metastable state. However, after the metastable state over, the SRAM cell still keeps upset state, which is inconsistent with the conclusion obtained by previous research.

To validate whether P1 collects enough deposited charge to trigger the upset, we refer the simulation method of the quenching effect in logic circuits. The 2 PMOS in 3D TCAD model are connected into an INV chain, as shown in Fig. 2(a). The input of INV chain is LOW, which keeps the state of net0, net1, P0 and P1 the

same with the ones in SRAM cell. Fig. 2(b) gives the simulation results that P0 collects deposited charge and triggers the first SET, and then P1 triggers the second SET after its state changing from ON to OFF. When LET is $40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, SET widths of net0 and out are 154 ps and 49 ps, respectively. And when LET is $100 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, SET widths of net0 and out are 214 ps and 18 ps, respectively. It indicates that the quenching effect happens between P0 and P1, and reduces SET width for the output of INV chains obviously. The charge sharing increases with LET values, and the increased charge sharing enhances the quenching effect. Thus, the quenching effect increases with LET value as shown in Fig. 2(b). These simulation results prove that the charge sharing between 2 PMOS is obvious, and P1 can collect enough deposited charge to trigger the upset. But in fact, SEUR does not happen between P0 and P1 under the same simulation conditions. There must be some details of generation mechanism of SEUR unclear, and they will be studied in depth in this paper.

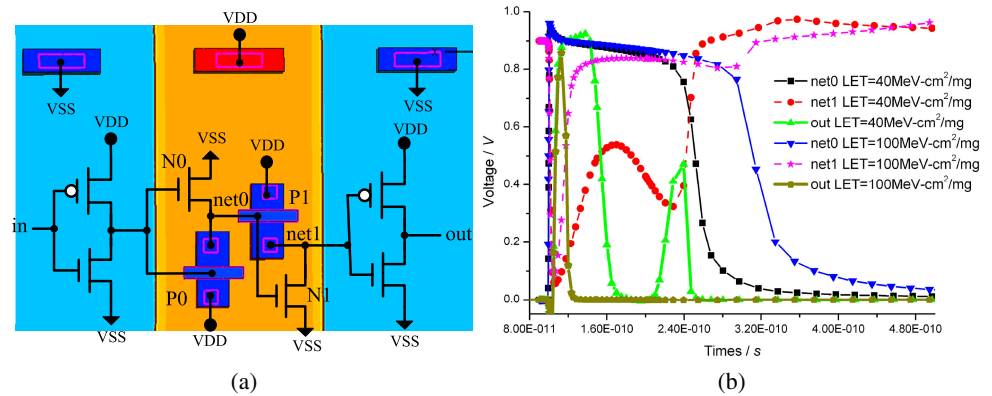


Fig. 2. (a) Schematic of a INV chains circuit with 2 PMOS in 3D TCAD model and other transistors in SPICE model, and (b) voltage pluses of net0, net1 and out at $\text{LET} = 40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ and $\text{LET} = 100 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

Since the delay of inverter in SRAM cells is very small, P1 changes from ON to OFF quickly after net0 changing from LOW to HIGH. Then, due to the drift and diffusion of charge and the parasitized bipolar amplification effect, P1 drain begins to collect charge. The state of net1 should change from LOW to HIGH if P1 collects enough charge, which is shown as the voltage pluses of net1 with LET of $100 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ in Fig. 1(b). Since the state switching of P1 is fast, P0 drain still collects charge at this time. Thus, after P1 turning into OFF state, P0 and P1 collect charge at the same time, and it makes the circuit enter into metastable state. When the metastable state is over, the circuit state is related to the competition between the charge collection of P0 and P1. For the particles striking the center of P0 drain at normal incidence, it is obvious that the charge collection of P0 is much more and longer than that of P1. Thus, the ability to maintain HIGH state of net0 is stronger than that of net1. Finally, net0 holds HIGH and net1 changes from HIGH to LOW, which makes the SRAM cell upset and SEUR not happen.

According to the discussions above, SEUR generation is mainly based on 2 factors: 1) the passive device collects enough deposited charge due to charge

sharing; 2) the charge collection of passive device is more and longer than that of active device, and the passive device wins the competition of drain voltage state. Although P1 collects enough charge to trigger SET in Fig. 2(b), SEUR does not happen. It indicates that striking the drain center of OFF PMOS, which is the most sensitive location, does not meet the second factor to trigger SEUR, while satisfying the first factor.

3 Implementation of hardened layout designs based on SEUR

Based on the new explored SEUR generation mechanism, we propose 2 layout strategies to decrease SEU rate for SRAM cells. Fig. 3(a) shows the traditional layout of a SRAM cell generated by Memory Compiler in 40 nm CMOS technology. Fig. 3(b) gives the first layout strategy, in which the 2 PMOS arrange in line and share the source. Since the layout structure is Drain-Source-Drain, the first layout strategy is called DSD layout for short. Fig. 3(c) gives the second layout strategy, in which a dummy PMOS is inserted and shares the active area with 2 original PMOS. The gate of dummy PMOS connects to the power supply (VDD), so the dummy PMOS can be closed all the time and can not affect the function of SRAM cells. The second layout strategy is called Dummy layout, as it inserts a dummy PMOS.

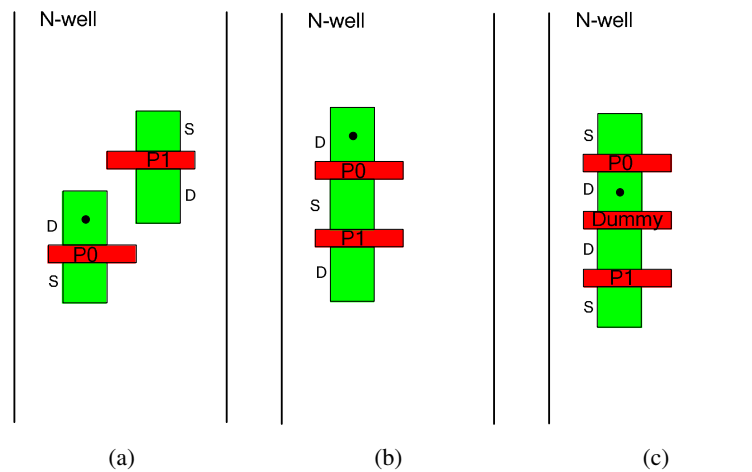


Fig. 3. (a) Traditional layout, (b) DSD layout in which 2 PMOS share the source, (c) Dummy layout in which a dummy PMOS is inserted and shares its active area with P0 and P1, respectively.

Compared with the traditional layout, DSD layout increases the distance between 2 drains, but cancels the shallow trench isolation (STI) between 2 drains. Since the canceled STI enhances the charge sharing between 2 PMOS, SEUR may happen easier. For Dummy layout, it not only cancels the STI but also reduces the distance between the 2 drains, which enhances the charge sharing further. Thus, SEUR rate of Dummy layout may be larger than that of DSD layout.

We get the whole SRAM cell height, width and area for all 3 kinds of layout based on commercial 40 nm process design rule, which are listed in Table I. Compared with the traditional layout, DSD layout decreases 24.36% SRAM cell

area while Dummy layout has the same SRAM cell area. Thus, DSD and Dummy layout strategies do not increase area for SRAM cells.

Table I. SRAM cell area information of the traditional, DSD and Dummy layout

Layout Type	SRAM Cell Height (μm)	SRAM cell Width (μm)	SRAM Cell Area (μm^2)
Tradition	0.58	1.34	0.78
DSD	0.58	1.10	0.59
Dummy	0.71	1.10	0.78

The inserted gate in Dummy cell keeps OFF all the time, so it does not produce dynamic power consumption. Since the source and drain of the inserted gate does not connect to VDD directly, the leakage current through the inserted gate is very small, which only increases a little power consumption. The traditional and Dummy SRAM cell are simulated in HSPICE tool based on 40 nm process, and the static power consumption of them is $7.85\text{e-}9\text{ W}$ and $8.25\text{e-}9\text{ W}$, respectively. We can see that the inserted gate only increases 5.10% power consumption. Thus Dummy layout does not bring serious power overhead.

4 SEU immunity validation

4.1 SEU sensitive area

SEU sensitive area is always used to estimate SEU sensitivity of SRAM cells. In this subsection, the SEU sensitive area is got at normal incident and $\text{LET} = 40\text{ MeV}\cdot\text{cm}^2/\text{mg}$ for all three layouts.

We also contrast the 3D TCAD models for DSD and Dummy, and connect them into the mixed-mode SRAM cell circuit as the one shown in Fig. 1(a). The initial

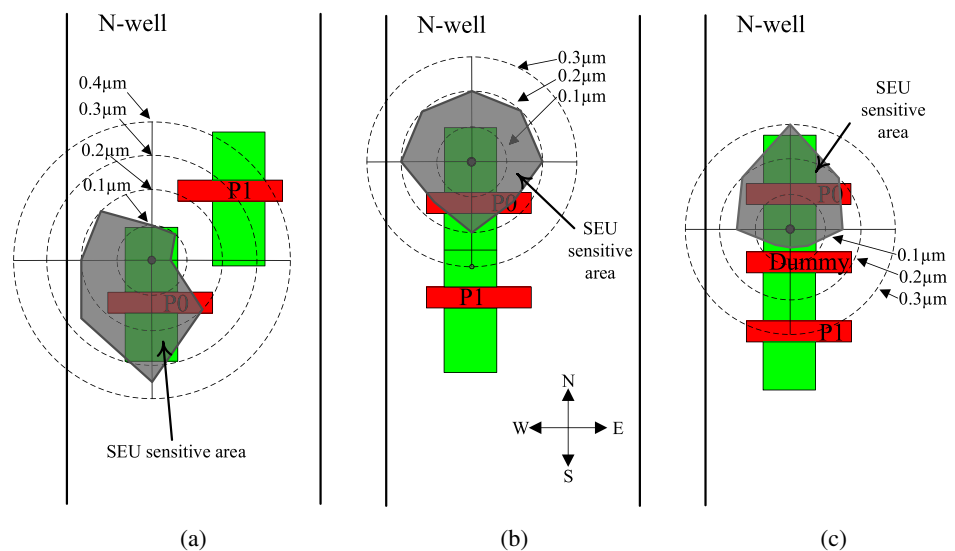


Fig. 4. SEU sensitive area of OFF PMOS in (a) traditional layout, (b) DSD layout and (c) Dummy layout while $\text{LET} = 40\text{ MeV}\cdot\text{cm}^2/\text{mg}$.

setup for each simulation is the same as before except that the gate of dummy PMOS in Dummy layout is connected to VDD all the time.

The drain center of device is regarded as the center point of SEU sensitive area, and then the hit location is extended to eight directions (i.e., east, southeast, south, southwest, west, northwest, north and northeast). The extended step of the hit location is $0.05\ \mu\text{m}$ and the last hit location induced SEU is treated as the boundary of SEU sensitive area in each direction. SEU sensitive area of device can be got after confirming the boundary in eight directions by simulation. Fig. 4 shows SEU sensitive areas for all three layouts. Via calculating the shadow area, we get SEU sensitive area values in Fig. 4, which are $1.03\text{E-}1\ \mu\text{m}^2$, $9.89\text{E-}2\ \mu\text{m}^2$ and $7.07\text{E-}2\ \mu\text{m}^2$ for the traditional, DSD and Dummy layout, respectively. Compared with the traditional layout, SEU sensitive area is reduced by 4.26% in DSD layout and 31.56% in Dummy layout.

It concludes that the proposed layouts can increase SEU immunity for SRAM cells. Although Dummy layout inserts a dummy PMOS into SRAM cell, it decreases SEU sensitive area sharply without area consuming. Thus, Dummy layout is an efficient way to improve SRAM cells radiation reliability.

4.2 Effect of incident angle

As discussed above, SEUR mainly depends on charge sharing between the active and passive devices. Since the incident angle affects the charge collection of device via changing the particle path, the effect of incident angle on SEUR is very important.

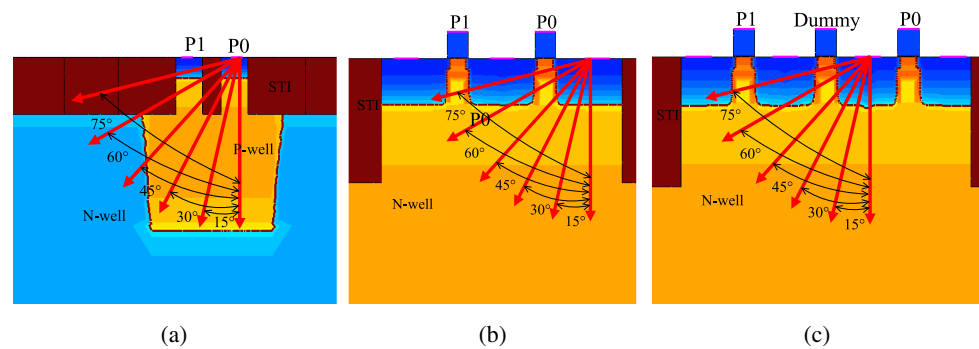


Fig. 5. Two-dimensional slice of 3D TCAD models containing 2 PMOS illustrating the angle of hit particles in (a) the traditional layout, (b) DSD layout, and (c) Dummy layout.

In the traditional layout, P1 is at the east of P0, so the incident angle leaned to east affects SEUR most. But in DSD and Dummy layout, P1 is at the south of P0, and the incident angle leaned to south direction affect SEUR most for them. Thus, in the following simulations, the incident particles are tilted to east in the traditional layout and tilted to south in DSD and Dummy layouts. The hit location is also the center of P0 drain in all simulations, and the extended step of the incident angle is 5° as shown in Fig. 5. Then we get the threshold angles of SEUR, which is the smallest incident angle inducing SEUR, when LET is $40\ \text{MeV}\cdot\text{cm}^2/\text{mg}$. The threshold angles of SEUR got in 3 layouts are listed in Table II.

Table II. Threshold angle of SEUR for three kinds of layout when LET is 40 MeV·cm²/mg

Layout Type	Threshold angles of SEUR
Tradition	30°
DSD	30°
Dummy	15°

The data listed in Table II shows that the threshold angle of SEUR is the smallest for Dummy layout, and it is the same for traditional and DSD layouts. Due to the span of incident angle is 90°, SEUR rate of Dummy layout is increased by 25% compared to traditional and DSD layouts under the tilted incident conditions. It proves that Dummy layout has a powerful capability to restrain SEU.

The unexpected data in Table II is that DSD layout does not decrease threshold angle of SEUR compared to the traditional layout under tilted incidence. The shared source in DSD layout not only enhances charge sharing between P0 and P1, but also increases the charge collection of P0 in tilted incident simulations. The increased charge collection of P0 restrains SEUR to happen. Thus, SEUR rate of DSD layout decreases and equals to traditional layout in tilted incident.

To study SEUR characterization under tilted incidence in depth, we refer the method of Ref. [9], and use the threshold LET of SEUR to evaluate SEU sensitivity of 3 kinds of layouts again. The threshold LET of SEUR means the smallest LET value to trigger SEUR. We choose 15°, 30°, 45° and 60° as the incident angle, and the incident direction is the same as mentioned above.

Table III. Threshold LET of SEUR under different incident angles and different layouts

Layout Type	Threshold LET of SEUR at 15° (MeV·cm ² /mg)	Threshold LET of SEUR at 30° (MeV·cm ² /mg)	Threshold LET of SEUR at 45° (MeV·cm ² /mg)	Threshold LET of SEUR at 60° (MeV·cm ² /mg)
Tradition	SEU	33	12	NONE
DSD	SEU	35	17	NONE
Dummy	23	3	NONE	NONE

Table III gives the threshold LET of SEUR for all three layouts. SEU in table means SEUR would not happen even LET is more than 100 MeV·cm²/mg, and NONE in table means upset would not happen under any LET values. When the incident angle is 15°, SEUR does not happen in the traditional and DSD layout. However, SEUR happens after LET increasing to 23 MeV·cm²/mg in Dummy layout. It is because the distance between the drains of P0 and P1 is the shortest in Dummy layout, which makes the tilted particle path close to P1 drain.

When the incident angles increase to 30° and 45°, SEUR happens easily in all three layouts. Moreover, the threshold LET of SEUR in Dummy layout is much smaller than that of the other 2 layouts at angle of 30°, and there is no SEU at angle of 45°.

As the incident angle going to increase, the threshold LET of SEU increases with the decreased charge collection of P0, and the threshold LET of SEUR decreases with the increased charge collection of P1. When the threshold LET of SEUR is no more than the threshold LET of SEU, SEU would not happen. That is the reason why SEU does not happen in all three layouts at angle of 60°.

In the whole tilted striking simulations, the occurrence rate of SEUR in Dummy layout is obviously larger than the traditional and DSD layout. Thus, Dummy layout can reduce SEU sensitivity for SRAM cells effectively. Although DSD layout reduces SEU sensitivity at normal incidence, it increases SEU sensitivity in tilted incident simulations.

5 Conclusion

We first study the generation mechanism of SEUR between 2 PMOS in SRAM cells in 40 nm CMOS technology by using 3D mixed-mode TCAD simulation. The simulation results show that SEUR will not happen when the particles hit the drain center of OFF PMOS. Through further simulating and analyzing, it is found that the generation of SEUR not only bases on the charge sharing but also complies with the rule that the charge collection of passive device is larger and longer than that of active device.

Then, two novel layout strategies named DSD and Dummy are proposed to increase rate of SEUR between 2 PMOS for reducing SEU vulnerability in SRAM cells. We get SEU sensitive area of PMOS in the traditional, DSD and Dummy layout, respectively. Comparing with the traditional layout, DSD layout reduces 8.33% SEU sensitive area, and Dummy layout reduces 16.67% SEU sensitive area. For the tilted incident, the occurrence rate of SEUR in Dummy layout is obviously larger than that of traditional and DSD layouts, while DSD layout is not better than the traditional layout on enhancing SEUR. In general, the proposed Dummy layout can increase SEU reliability for SRAM cells in both normal and tilted incident without area penalty.

Acknowledgments

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