

A hybrid threshold self-compensation rectifier for RF energy harvesting

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Abstract: This paper presents a novel highly efficient 5-stage RF rectifier in SMIC 65 nm standard CMOS process. To improve power conversion efficiency (PCE) and reduce the minimum input voltage, a hybrid threshold self-compensation approach is applied in this proposed RF rectifier, which combines the gate-bias threshold compensation with the body-effect compensation. The proposed circuit uses PMOSFET in all the stages except for the first stage to allow individual body-bias, which eliminates the need for triple-well technology. The presented RF rectifier exhibits a simulated maximum PCE of 30% at -16.7 dBm ($20.25 \mu\text{W}$) and produces 1.74 V across $0.5 \text{ M}\Omega$ load resistance. In the circumstances of $1 \text{ M}\Omega$ load resistance, it outputs 1.5 V DC voltage from a remarkably low input power level of -20.4 dBm ($9 \mu\text{W}$) RF input power with PCE of about 25%.

Keywords: energy harvester, RF rectifier, threshold compensation

Classification: Integrated circuits

References

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1 Introduction

Replacing internal power source by the extraction of energy from propagating radio waves, RF energy harvester shows promising applications on extending the lifetime and reducing the maintenance-cost of wireless sensor network nodes (WSNN). The

input voltage amplitude should be larger than the threshold voltage of the MOSFETs to make the rectifier work. However, the RF energy density is so small that the input voltage amplitude is far lower than the threshold voltage. Typically, the input voltage amplitude is no more than 300 mV although an impedance matching network is used to boost the voltage induced by the antenna. The threshold voltage compensation technology is proposed to improve the performance of the RF rectifier. Umeda et al. [1] and Li Bo et al. [2] compensate the threshold voltage by using auxiliary circuits to generate gate bias voltage. However, the efficiency decreases a lot due to the current consuming by the auxiliary circuits. Shameli et al. [3] has used low- V_{th} MOSFETs to improve the performance, which may greatly increase the cost. Papotto et al. [4] proposed a self-compensation technology by getting bias from the adjacent stage. However, to eliminate the body effect, all of the devices in [4] are NMOS in deep n-well, which cannot be implemented in standard CMOS process.

This paper proposed a novel hybrid threshold compensation approach, which combines the gate-bias-compensation with body-effect compensation. The proposed RF rectifier can be implemented in standard CMOS process to improve PCE and reduce the minimum input voltage.

2 The threshold voltage reduction caused by body effect

In standard CMOS process, the body of NMOS must be connected to ground. So in the Dickson's cascade boosting topology, with the increasing stage of RF rectifier, the voltage difference between the source and the substrate will increase, which causes the threshold voltage of NMOS higher [4]. However, in standard CMOS process, PMOS is fabricated in n-well and the voltage of body can be individually biased. The relationship between the threshold voltage of PMOS (V_{THP}) and the source-bulk voltage difference (V_{SB}) can be expressed as Eq. (1):

$$V_{THP} = V_{THP0} + \gamma(\sqrt{2|\Phi_F| + V_{SB}} - \sqrt{2\Phi_F}) \quad (1)$$

Where, V_{THP0} is the threshold voltage when V_{SB} is 0, γ is a constant determined by the process and Φ_F is the surface potential of the substrate. It is obvious that the threshold voltage would reduce when the source-body PN junction is forward biased ($V_{SB} > 0$). The leakage current should be considered because this PN junction is forward biased. In RF rectifier, the MOSFET works in strong inversion region. Thus to ensure device performance, the saturation current should be far greater than the leakage current of the PN junction. For the sake of simplicity, the forward-bias leakage current I_{leak} can be neglected, as long as it smaller than the sub-threshold current I_{sub} . The sub-threshold current can be depicted as Eq. (2) [5].

$$I_{sub} = \mu_p C_{ox} (\eta - 1) V_T^2 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (2)$$

Where, μ_p is the mobility of the hole, C_{ox} is unit area gate oxide capacitor, V_T is the thermal voltage. W and L are the width and length of the MOSFET channel, respectively. V_{TH} is the threshold voltage, η is sub-threshold inversion factor and V_{GS} is the voltage difference between the gate and the source. When V_{GS} is equal to V_{TH} , the sub-threshold current reaches to the maximum value.

$$I_{sub\ max} = \mu_P C_{ox} (\eta - 1) V_T^2 \frac{W}{L} \quad (3)$$

The leakage current is shown in Eq. (4) when V_{SB} is positive. I_{s0} is reverse saturation current, and A_{SB} is the contact area between the source and body.

$$I_{leak} = I_{s0} A_{SB} \left[\exp\left(\frac{V_{SB}}{V_T}\right) - 1 \right] \approx I_{s0} A_{SB} \exp\left(\frac{V_{SB}}{V_T}\right) \quad (4)$$

Defining $\alpha = I_{leak}/I_{submax}$, the maximum V_{SB} can be calculated from Eq. (3) and (4).

$$V_{SB} = V_T \ln \left(\alpha \cdot \frac{\mu_P C_{ox} (\eta - 1) V_T^2 W}{I_{s0} A_{SB} L} \right) \quad (5)$$

Based on the SMIC 65 nm CMOS process parameters, the critical value of V_{SB} (V_{SBth}) is about 0.58 V by setting $\alpha = 0.001$ and $W/L = 8\ \mu\text{m}/60\ \text{nm}$. In the proposed design example, if the forward bias between the source and body is smaller than 0.58 V, the forward leakage current can be neglected. Fig. 1 shows the threshold voltage of PMOS varies with the source-body bias in SMIC 65 nm CMOS process. In the circumstances of weak forward bias ($0 < V_{SB} < 0.58\ \text{V}$), the threshold voltage will decrease about 20 mV with V_{SB} increasing 100 mV, which is almost linear.

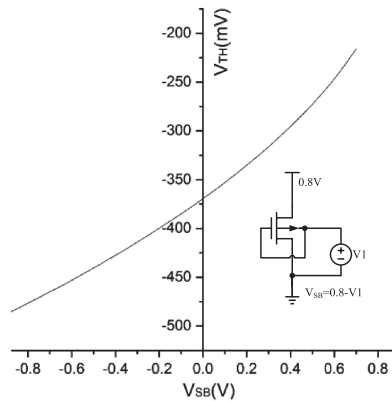


Fig. 1. PMOS threshold voltage versus V_{SB} in SMIC 65 nm CMOS process

3 The proposed hybrid threshold self-compensation rectifier

As mentioned in section 2, in standard CMOS process the body effect of the NMOSFET will degenerate the performance of RF rectifier. To eliminate body effect, the PMOSFETs of which the source and substrate are connected together can be used to replace the NMOSFETs in RF rectifiers. Fig. 2a shows a traditional 3-stage RF rectifier without threshold voltage compensation. By connecting the body to the source, the threshold of all the PMOSFETs keep the same value, which determined by the process. However, to lower the threshold voltage and improve the performance of the rectifier, threshold compensation should be used.

Threshold self-compensation technology [4] provides an effective way as there is no auxiliary circuits and power consumption are needed. To compensate the

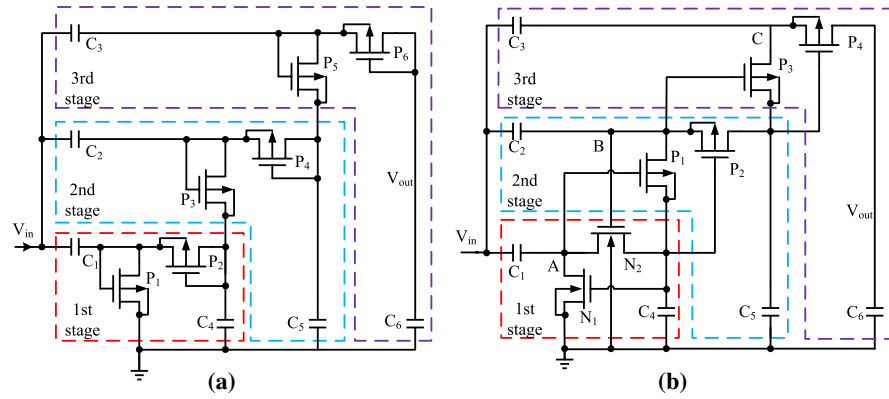


Fig. 2. (a) 3-stage RF rectifier without threshold compensation (b) 3-stage RF rectifier with threshold gate-bias-compensation

threshold voltage, the gate of the PMOS should be connected to a lower potential than that of the source. So in the Dickson's cascade boosting topology, the gate of PMOS should be biased by the former stage. On the contrary, the gate of NMOS in this structure should be biased by the latter stage. Fig. 2b shows a 3-stage RF rectifier with threshold gate-bias-compensation. In the structure without threshold compensation as shown in Fig. 2a, if the output load is not considered, the idea output can be expressed as Eq. (6).

$$V_{out} = N \left(2V_{in} \frac{C_s}{C_s + C_p} - 2|V_{THP}| \right) \quad (6)$$

N is the number of stages of the RF rectifier, V_{in} is the amplitude of input signal and V_{THP} is the threshold voltage of PMOSFET. C_p is the total parasitic capacitance in node A (the same with node B or C) and C_s is the sampling capacitance of C_1 (the same with C_2 or C_3) which is much larger than C_p . So Eq. (6) can be simplified as Eq. (7).

$$V_{out} \approx 2N(V_{in} - |V_{THP}|) \quad (7)$$

Eq. (7) shows that the threshold voltage has a large influence on the output voltage of the RF rectifier, and the voltage difference between the adjacent two stages is about $2(V_{in} - |V_{THP}|)$. It can be considered that the equivalent threshold voltage has a decrease of $2(V_{in} - |V_{THP}|)$ by the gate-bias-compensation, comparing with the rectifier without threshold compensation shown in Fig. 2a. So the compensation voltage V_{comp} in Fig. 2b can be defined as $2(V_{in} - |V_{THP}|)$, which is almost equal to the voltage between the gate and drain V_{GD} . The ideal compensation voltage can be shown as Eq. (8).

$$V_{comp} = V_{GD} \approx 2(V_{in} - |V_{THP}|) \quad (8)$$

In fact, since some non-ideal factors such as reverse leakage current, the actual compensation voltage will be smaller than the ideal value V_{comp} . The compensation voltage V_{comp} applied on the gate of MOSFET, the MOSFET can go into strong inversion with a smaller input voltage. In other words, it is equivalent to that the threshold voltage is reduced. According to Eq. (7), the threshold voltage V_{TH} decreasing means higher output voltage and conversion efficiency. As mentioned above, by connecting the body and the source together, the threshold voltage of all

the PMOSFETs can be the same. The weak forward bias between source and body can further decrease the threshold voltage of PMOS according to Eq. (2), which has been introduced previously.

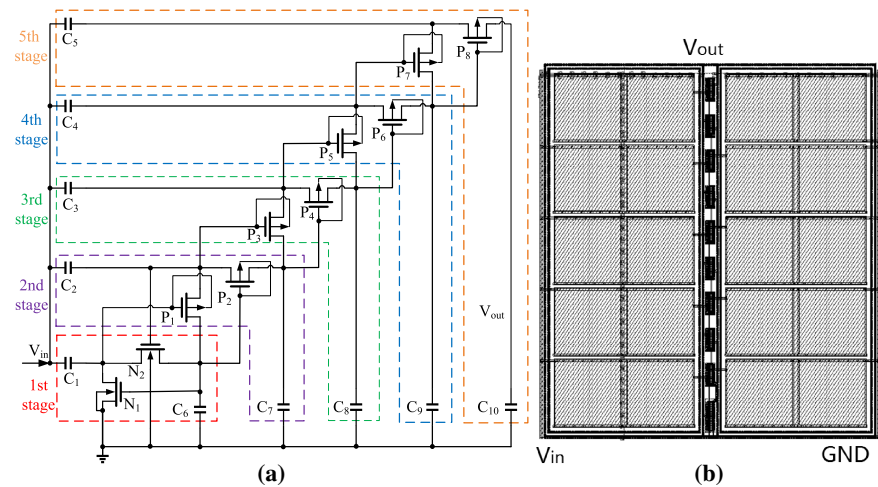


Fig. 3. (a) 5-stage hybrid threshold self-compensation RF rectifier
(b) Layout of the proposed rectifier based on SMIC 65 nm standard CMOS process

Fig. 3a shows the proposed 5-stage hybrid threshold self-compensation RF rectifier. The first stage consists of two NMOS (N_1 , N_2) and two sampling capacitors (C_1 , C_6). And the next four stage are constituted with 8 PMOS ($P_1 \sim P_8$) and 8 capacitors ($C_2 \sim C_4$ and $C_7 \sim C_{10}$). To further reduce the threshold of these PMOSFETs, we connect the body to the gate rather than the source as shown in Fig. 3a. The source voltage of NMOSFETs in the first stage is low and the body effect of the first stage can be neglected. The aspect ratio of all the MOSFETs in Fig. 3a is $8 \mu\text{m}/60 \text{ nm}$, and the capacitance of all the sampling capacitors is 1.5 pF . To ensure the rectifier work properly, the voltage between source and body should be lower than the critical value V_{SBth} , which can be expressed in Eq. (9).

$$V_{SB} = V_{SG} = V_{SD} + V_{DG} = V_{SD} + V_{comp} < V_{SBth} \quad (9)$$

In the proposed RF rectifier, by using both the gate-bias-compensation technology and body-effect compensation of PMOS, the threshold voltage can be reduced to the maximum extent. According the Eq. (9), we can choose the value of the compensation voltage V_{comp} properly to improve the performance of the RF rectifier. Based on SMIC 65 nm standard CMOS process, the layout of the proposed 5-stage hybrid threshold self-compensation RF rectifier is shown in Fig. 3b. The total layout area is about $0.16 \times 0.14 \text{ mm}^2$.

4 Simulation results

Based on the spice models of SMIC 65 nm CMOS process, simulations of the proposed 5-stage hybrid threshold self-compensation RF rectifier are made. The antenna can be regarded as a sinusoidal voltage source with 50Ω internal resistance. Fig. 4 shows the transient simulation results of the proposed rectifier with $0.5 \text{ M}\Omega$ load resistance and the RF input power is -16.9 dBm . It can be seen that

the voltage difference between every two stages is almost the same about 0.38 V, which is the gate-bias compensation voltage value. The simulation result shows that the maximum V_{SD} is about 0.11 V in saturation region, and then the maximum V_{SB} of 0.49 V can be calculated by the Eq. (9). As mentioned in section 2, the absolute value of the threshold voltage of PMOSFET is reduced from 370 mV to 275 mV by weak forward bias of the source-body PN junction, and the threshold voltage decreases by about 25.7%.

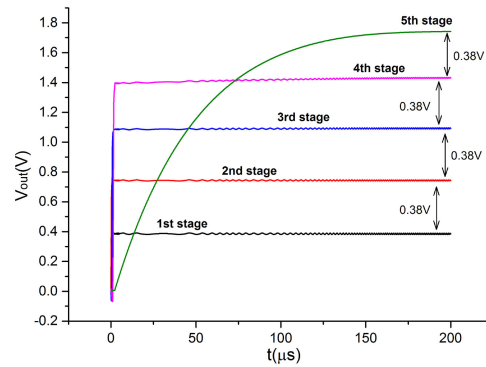


Fig. 4. Transient simulation results of the proposed RF rectifier ($C_{load} = 0.1$ nF, $R_{load} = 0.5$ M Ω , $f = 915$ MHz, RF input power = -16.7 dBm)

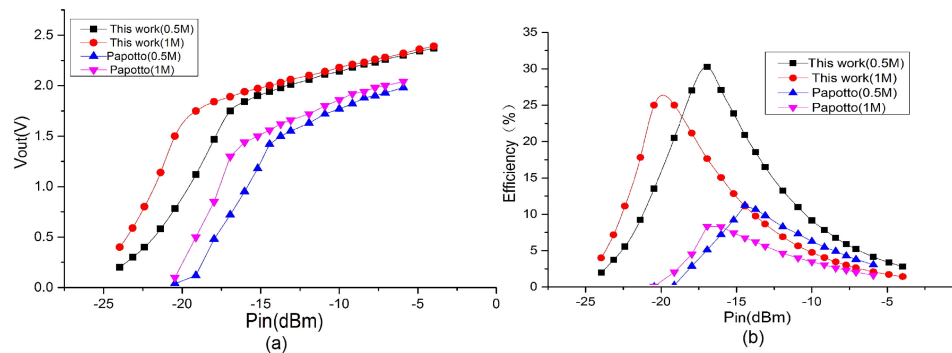


Fig. 5. (a) Output dc voltage versus available RF input power for different load resistance values (b) PCE versus available RF input power for different load resistance values ($C_{load} = 0.1$ nF, $f = 915$ MHz)

The output dc voltage versus available RF input power for different load resistance values are shown in Fig. 5a. When loaded by 0.5 M Ω load resistance, the proposed rectifier can deliver the output dc voltage of 1.5 V with an available input RF power of -17.9 dBm (16.3 μ W). In the circumstances of 1 M Ω load resistance, the output dc voltage can reach the same value at -20.45 dBm (9 μ W) RF input power. The rectifier PCE is reported in Fig. 5b as a function of the available input RF power for different load resistances. Under general conditions (1.5 V dc output), the proposed rectifier attains the maximum PCE of 25% (-20.45 dBm RF input) on 1 M Ω load and 30% (-16.9 dBm) on 0.5 M Ω load respectively. Comparing with the classic RF rectifier in reference [4], the proposed one with hybrid compensation exhibits better output performance, lower RF input power and

higher power conversion efficiency. The summary of the proposed rectifier and comparison with the previous works are given in Table I.

Table I. Rectifier's performances summary and comparison with prior Art

Reference	Process	Frequency	Load	PCE	Output	Area
[1]	0.25 μm	950 MHz	400 nA	1.2%@-14 dBm	1.2 V	0.64 mm ²
[2]	0.18 μm^{L}	920 MHz	2 μA	5.2%@-14.1 dBm	1.0 V	1 mm ²
[3]	0.13 μm	900/1900 MHz	1 M Ω	9.1%@-19.3 dBm	1.15 V	0.8 mm ²
[4]	90 nm ^D	915 MHz	1 M Ω	11%@-18.8 dBm	1.2 V	0.19 mm ²
[6]	0.18 μm	953 MHz	320 nA	32%@-30 dBm	1.0 V	0.03 mm ²
This work	65 nm	915 MHz	1 M Ω	25%@-20.45 dBm	1.5 V	0.022 mm ²
			0.5 M Ω	30%@-16.9 dBm	1.74 V	

0.18 μm^{L} : Low- V_{TH} Transistor used. 90 nm^D: Deep n-well process used.

5 Conclusion

This paper proposes a novel 5-stage hybrid threshold self-compensation RF rectifier based on SMIC 65 nm CMOS process. We combine the body-effect compensation and the gate-bias-compensation strategy together to reduce the threshold voltage of the rectifying device to the maximum extent. By this way, the equivalent threshold voltage of PMOSFET could decrease from -370 mV to 105 mV, which can make the PMOSFETs work in strong inversion region at very low input RF power. Simulation results show that the proposed RF rectifier outputs 1.5 V DC voltage (25% PCE) with 1 M Ω load when the input power is -20.45 dBm. And with 0.5 M load, the output is 1.74 V (30% PCE) when the input power is -16.7 dBm. The proposed RF rectifier can be widely used in WSN to replace battery for providing energy.

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