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140 GHz CMOS amplifier with group delay variation of 10.2 ps and 0.1 dB bandwidth of 12 GHz

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Abstract: A 140 GHz CMOS wideband amplifier is proposed with the low group delay variation required to achieve a high-speed D-band wireless receiver. The amplifier is fabricated by the standard 1P12M 65 nm CMOS process. From measurement, the gain is 10 dB with a group delay variation of 10.2 ps. The 0.1 dB bandwidth, used as the figure of merit of the gain flatness, is 12 GHz, whereas the generally used 3 dB bandwidth is 27.6 GHz. The power consumption is 57.1 mW with a supply voltage of 1.2 V.

Keywords: millimeter wave, CMOS, wideband, amplifier, group delay

Classification: Microwave and millimeter wave devices, circuits, and systems

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1 Introduction

Recently, CMOS circuits operating in the millimeter-wave band have been realized owing to the improvement of high-frequency performance by miniaturizing the gate length of MOSFETs. Several CMOS millimeter- and short-millimeter-wave wireless transceivers have been reported [1, 2], in which a front-end low-noise small-signal amplifier is an important component. The amplifier is used to amplify the weak signal received from an antenna, and requires a high gain and high operating frequency to amplify the received small signal before downconversion. In addition, wideband operation is required to achieve high-speed communication, because the modulated signal has a wide frequency band owing to the high bit rate. The performance of the amplifier affects the sensitivity and data rates of a receiver.

Generally, both amplitude information and phase information are used in wireless communication. Since the envelope of a communicating signal is formed with the amplitude variation, demodulation fails when the envelope of the signal collapses. As a result, the group delay as well as the gain of the amplifier has to be constant in a target frequency band. The flatness of the gain and group delay is important in high-speed communication. Note that the D band, 110 to 170 GHz, has the potential to be used for wideband communication, in which high-speed wireless communication can be achieved. As a result, the amplifier for the D band is required to cover the frequency band. In the microwave ultrawide band (UWB), a technique using a group delay equalizer has been proposed to keep the group delay constant in the target frequency band as shown in Fig. 1 (a) [3]. However, this technique increases the power consumption and decreases the communication speed owing to the equalizer, which adjusts the group delay using passive devices having considerable insertion loss. In particular, it is difficult for D-band amplifiers to obtain sufficient gain because NMOSFETs have only a small maximum available gain (MAG) in the D band. The insertion loss caused by an equalizer degrades the gain of the D-band amplifier and the receiver cannot obtain sufficient sensitivity. On the other hand, when an amplifier

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with a constant group delay is achieved, no degradation of gain due to the equalizer occurs and the receiver can obtain sufficient sensitivity as shown in Fig. 1 (b).

In this letter, we propose a wideband amplifier with a flat gain and low group-delay variation for high-speed wireless communication. The target specification of the amplifier is 3 dB bandwidth of 25 GHz and group-delay variation within 16 ps, complying with modulated signal for 12.5 Gbps amplitude-shift keying (ASK). In section 2, the design method of the amplifier is described. Measurement results for the fabricated amplifier are reported in section 3. Finally, the letter is concluded in section 4.

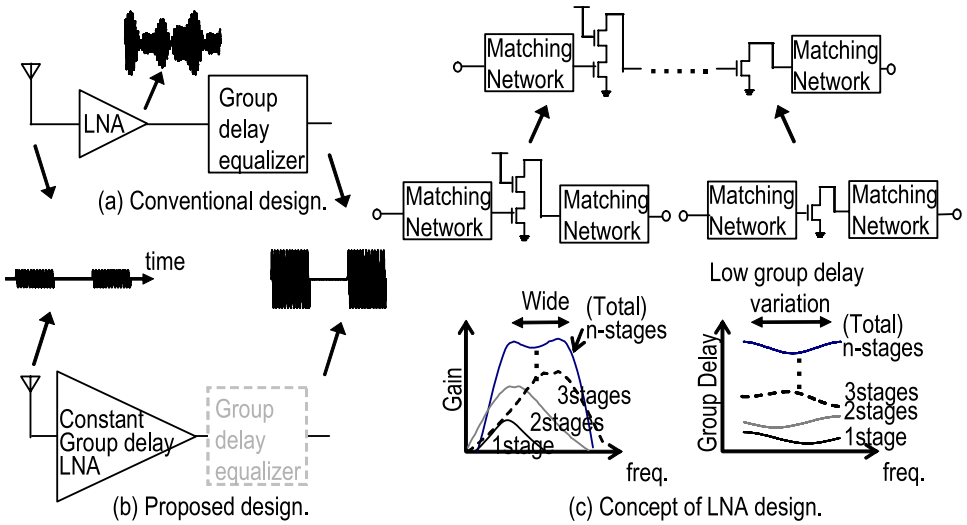

Fig. 1. LNA applied as for high-speed transceiver.

2 Design principle for a short-millimeter-wave wideband amplifier

Figure 1 (c) shows the design concept of the proposed amplifier. Cascade stages are used to achieve a high gain with wideband operation. When all the interstage matching circuits are designed at the same frequency, the amplifier gives the highest peak gain but no wideband characteristics can be achieved. As a result, the matching frequencies in the interstage matching circuits should be allocated with distribution in the target frequency band so that wideband characteristics may be achieved. Here, the frequency response of matching circuits is dependent on source and load impedances. However, gate impedance, which is the load of an input matching circuit of the MOSFET, is determined only after the load impedance of the drain is determined. Similarly, drain impedance, which is the source of an output matching circuit of the MOSFET, is also determined only after the impedance connected to the gate is determined. Therefore, it is difficult to design all the matching circuits simultaneously in a wideband cascade amplifier. To overcome this issue, we firstly allocate the matching frequency in each stage with the proper distribution and design single-stage amplifiers separately with source and load

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of reference impedance Z_0. After designing all the single-stage amplifiers, we combine them and make a wideband amplifier.

Similarly, to minimize the variation of group delay of the amplifier, each stage is designed so that the group delay may be constant after the signal goes through all the stages. Generally, the group delay has a peak response as the gain has. In a single-stage amplifier with a single gain peak, the peak frequency of the group delay is close to the peak frequency of the gain. By utilizing this feature, the constant group delay of the whole amplifier can be realized by combining single-stage amplifiers with different group delay peak as the gain is made constant. On the other hand, since group-delay variation becomes steep when the gain variation is steep, a constant group delay is difficult to realize by combining single-stage amplifiers with high gain. Namely, the tradeoff between peak gain and group delay flatness exists in the single-stage amplifier, and group delay can be adjusted by changing the peak gain. As a result, when the multistage amplifier is synthesized, the gain is not only made constant, but group delay is also made constant by optimizing the gain.

Specific design steps are as follow. Firstly, assuming that input and output impedances are a reference impedance Z_0 ($=50\,\Omega$), single-stage amplifiers with the T-shape matching networks are designed to optimize gains at a specific frequency. In this design step, input and output matching networks in each single-stage amplifier are determined and the gate and source impedances of each MOSFET are also determined. These single-stage amplifiers can be directly connected. In the interstage matching network, the drain impedance in the previous stage will change to the gate impedance in the next stage going through Z_0 at the connecting point of two matching circuits. This cascade connection with two-stage T-shape matching circuits gives two insertion losses from two matching circuits between adjacent MOSFETs, which will decrease the total gain of the amplifier. To minimize the loss, these two-stage T-shape matching networks, between adjacent MOSFETs with fixed drain and gate impedances, are redesigned without going through Z_0 using single-stage T-shape matching network. Here, the frequency characteristics in the terminal impedances of the original two-stage T-shape matching network are approximated by those of the redesigned single-stage T-shape matching network. By keeping the terminal impedances of the matching networks, total gain and group delay of the amplifier are also maintained.

Figure 2 (a) shows a schematic of the proposed wideband amplifier, which comprises MOSFETs, MIM capacitors and TLs. A cascode amplifier is used in the first stage, and five-stage common-source amplifiers are used in the other stages. Since the power consumption and layout size increase with increasing number of stages, the gain per stage has to be increased to reduce the number of stages. Generally, a common-source amplifier obtains a higher gain in the D band than a cascode amplifier. On the other hand, a common-source amplifier is less stable than the cascode amplifier since the common-source amplifier has a smaller reverse isolation. In our design, the cascode amplifier is used in the first stage to suppress the unpredictable stability issue

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due to multistage amplifiers, and common-source amplifiers are used in the second to sixth stages to increase total gain.

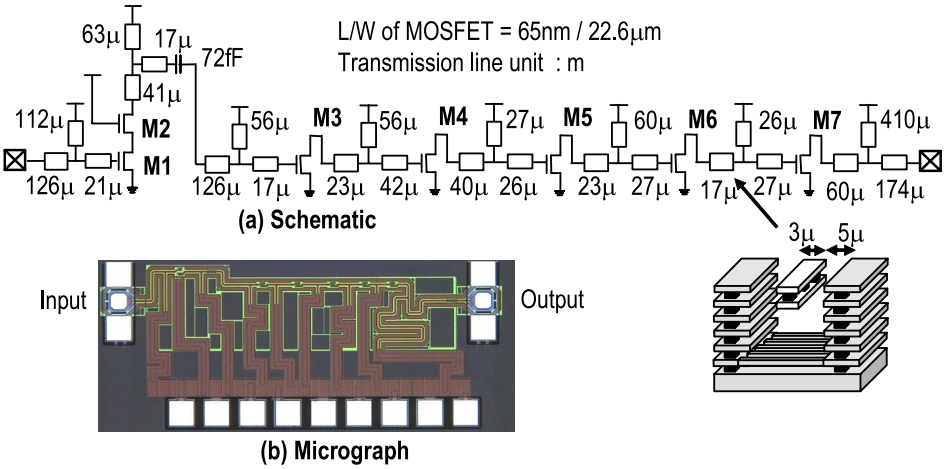


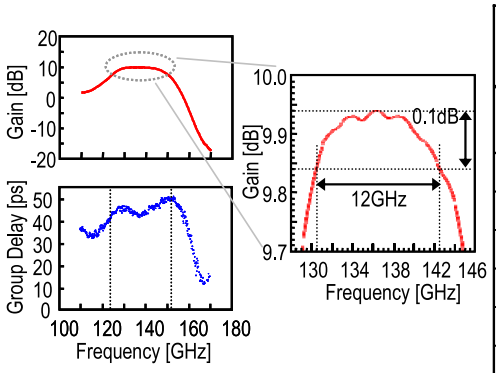
Fig. 2. Schematic and micrograph of the amplifier.

3 Measurement results

We fabricated the D-band wideband amplifier with standard 1P12M 65 nm CMOS technology. Figure 2 (b) shows a micrograph of the amplifier. The core size is $400\times800\,\mu\text{m}^2$. Measurement results for the amplifier are shown in Fig. 3. Figure 3 (a) shows the measurement results of gain and group delay. The peak gain is 10 dB at 137.3 GHz, and the 3 dB bandwidth is 27.6 GHz. The power consumption is 57.1 mW with a supply voltage of 1.2 V. Figure 3 (b) shows the gain close to the peak-gain frequency in detail, showing that the 0.1 dB bandwidth is 12 GHz.

Group delay is calculated from the S-parameters of the amplifier using Eq. (1).

$$GroupDelay = \frac{\Delta Phase(S_{21})}{2\pi \cdot \Delta freq}. \tag{1}$$



Freq. [GHz]	0.1dB -BW [GHz]	3dB-BW [GHz]	Peak Gain [dB]	GD [ps] @3dB-BW	P_{DC} [mW]	Technology [nm]	Ref.
136.1	12	27.6	9.9	46.2 ±13.1	57.1	65	This work
150	1.1	27.0	8.2	N/A	25.5	65	[4]
140	0	10	8	N/A	63	65	[5]
144	1.9	10	9	N/A	75.6	65	[1]
95	2.8	19	10	N/A	35.0	65	[6]
63	2.3	14	17	N/A	36	90	[7]
60	1.0	8.5	12.2	120.7 ±26.3	29.1	130	[8]

(c) Comparisons

Fig. 3. Measurement results and comparisons.

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The group delay in the 3 dB bandwidth is 40.3 to 50.5 ps, thus, the group delay variation is 10.2 ps. Finally, performance comparisons are shown in Fig. 3 (c). A 0.1 dB bandwidth is used as the figure of merit of the gain flatness. Other reported D-band amplifiers have a 0.1 dB bandwidth of less than 3 GHz. On the other hand, the proposed amplifier has a 0.1 dB bandwidth of 12 GHz, which is the largest value ever reported. Moreover, the proposed amplifier achieved a group-delay variation of 10.2 ps, although the group delay was not discussed for previously reported D-band amplifiers. According to our results, the proposed amplifier has sufficiently high gain and good group-delay characteristics for use as a front-end amplifier in a high-speed D-band receiver.

4 Conclusion

In this letter, a 140 GHz CMOS amplifier with a 0.1 dB bandwidth of 12 GHz and a 3 dB bandwidth of 27.6 GHz was realized with a low group-delay variation. The proposed amplifier was fabricated by a standard 1P12M 65 nm CMOS process, and had a peak gain of 10 dB with a group-delay variation of 10.2 ps. The power consumption was 57.1 mW with a supply voltage of 1.2 V. As a result, the performances required to realize a low-power front-end amplifier for a D-band wireless receiver were obtained.

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