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Pico Watt sub-threshold CMOS voltage reference circuit

A. Sahafi[a)], **J. Sobhi, and Z.D. Koozekanani**

Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran

a) *a.sahafi@tabrizu.ac.ir*

Abstract: This paper presents a simple Pico Watt reference circuit with the output voltage of 263.1 mV using sub-threshold operation of MOSFETs at supply voltage of 0.7 V. Proposed circuit consumes merely 400 pW of power at room temperature and it is designed using standard TSMC 0.18 μm technology. Reference voltage is provided by subtracting the 0°C threshold voltage of MOSFETs. The simulation results show voltage variation of 0.32 mV/V for supply voltage from 0.7 V to 2.5 V and about 0.4 mV of temperature variation in the range of −40°C to 120°C. The active area of the proposed circuit is 500 μm^2. Our device would be suitable for use in passive RFIDs, WSN applications and all other power-aware SOCs.

Keywords: voltage reference, Pico Watt, sub-threshold, WSN, RFID

Classification: Integrated circuits

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1 Introduction

Voltage reference circuits play a key role in analog and mixed signal systems. They are important components of analog to digital and digital to analog converters also they are applied in numerous analog circuits used in portable devices, RFID tags and implantable medical devices such as operational amplifiers, filters, and sensors [1]. These devices should operate in ultra-low power condition, e.g. some micro Watts or less because they will probably be placed under conditions where they have to get the necessary energy from poor energy sources such as micro-batteries and environmental energy sources [2].

The most common solution for on-chip voltage reference is the Bandgap Voltage Reference (BGR), which can be implemented in standard CMOS technology using vertical BJTs [3, 4, 5] with nearly temperature-independent reference. However, they need resistors with a high resistance of several hundred mega-Ohms with large occupied chip area to achieve low-current, sub-threshold operation that make it unsuitable to use in low cost and low power applications. Therefore, modified voltage reference circuits for low-cost, low-power applications have been reported. However, these circuits have various problems such as large power dissipation [6, 7] and sensitive output voltage to supply voltage and temperature variation [8].

In this paper, a reformed full CMOS voltage reference configuration, based on temperature compensation technique derived from the sub-threshold region of operation, is described. Within the circuit, two n-channel MOSFETs with different 0°C threshold voltages are presented and the reference voltage value is obtained by subtracting threshold voltages.

This paper is organized as follows: In section 2 the proposed scheme is described, in section 3 simulation results are shown and in section 4 a comparison with low-power and low-voltage competitors is presented and concluded.

2 Proposed circuit

Figure 1 illustrates the architecture of proposed voltage reference circuit that consists of two parts: start up circuit and reference voltage generator. The zero Watt startup circuit (M_{S1}, M_{S2}, C_{NMOS}) has been implemented to decrease the steady state time of circuit to some milliseconds. The reference

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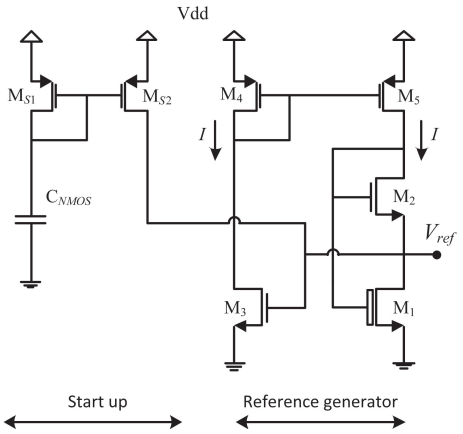

Fig. 1. Proposed voltage reference circuit

voltage generator (M_1–M_5) is a self-biased current source with embedded load (M_1: high voltage NMOS, M_2: normal NMOS) which has no resistor and works with all MOSFETs in the sub-threshold region. By using zero Watt start-up circuit and eliminating unnecessary current branches compared to [8], total power dissipation is reduced dramatically.

The drain current of a MOSFET in sub-threshold region is an exponential function of the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}), and given by [6], [8], and [9]:

$$\begin{aligned} I_D &= K\mu V_T^2 \exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right] \\ K &= (W/L)C_{ox}, \quad V_T = \frac{k_B T}{q} \end{aligned} \tag{1}$$

where W/L is the transistor aspect ratio, C_{ox} is the gate oxide capacitance per unit area, μ is the electron mobility, V_T is the thermal voltage (k_B is the Boltzmann constant, q the elementary charge and T the absolute temperature), V_{th} is the MOSFET threshold voltage and η is the sub-threshold slope factor.

For $V_{DS} > 0.1\,\mathrm{V}$, drain current is independent of V_{DS} and gate-source voltage (V_{GS}) is obtained by using Eq. (1):

$$V_{GS} = V_{th} + \eta V_T \ln\left(\frac{I_D}{K\mu V_T^2}\right) \tag{2}$$

Threshold voltage of the MOSFET is reduced linearly by temperature [10]:

$$V_{th} = V_{0th} + (k_{1t} + k_{2t}V_{BS})(T/T_0 - 1) \tag{3}$$

where V_{0th} is the threshold voltage at 0°C ($T_0 = 273.15\,\mathrm{K}$), V_{BS} is the body-to-source voltage of the transistor, k_{1t} and k_{2t} are negative temperature coefficients.

Output voltage of the reference circuit is obtained by subtracting gate-source voltage of M_1 and M_2:

$$V_{ref} = V_{GS3} = V_{GS1} - V_{GS2} \tag{4}$$

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By utilizing Eq. (2)–(4):

$$V_{ref} = (V_{0th1} - V_{0th2}) + (k_{1t1} - k_{1t2} - k_{2t2}(-V_{ref}))(T/T_0 - 1) + \Delta V \quad (5)$$

where

$$\Delta V = (\eta_1 - \eta_2)V_T \ln\left(\frac{I}{\mu V_T^2}\right) + V_T \ln\left(\frac{K_2^{\eta_2}}{K_1^{\eta_1}}\right) \quad (6)$$

Current of I is equal to drain current of M_3:

$$I = I_{D3} = K_3 \mu V_T^2 \exp\left(\frac{V_{ref} - V_{th3}}{\eta_3 V_T}\right) \quad (7)$$

By combination of Eq. (6) and Eq. (7):

$$\begin{aligned} \Delta V &= (\eta_1 - \eta_2)V_T \ln\left(K_3 \exp\left(\frac{V_{ref} - V_{th3}}{\eta_3 V_T}\right)\right) + V_T \ln\left(\frac{K_2^{\eta_2}}{K_1^{\eta_1}}\right) \\ \Delta V &= \frac{\eta_1 - \eta_2}{\eta_3}(V_{ref} - V_{th3}) \; + \; V_T \ln\left(\frac{K_2^{\eta_2} K_3^{\eta_1 - \eta_2}}{K_1^{\eta_1}}\right) \end{aligned} \quad (8)$$

Using Eq. (4)–(8), output voltage of reference circuit can be rewritten by:

$$V_{GS1} - V_{GS2} = V_{ref} = A \times T + B \quad (9)$$

where A and B are temperature independent constants:

$$\begin{aligned} A &= \frac{k_{1t1} - k_{1t2} + k_{2t2}V_{ref}}{T_0} - \frac{\eta_1 - \eta_2}{\eta_3} \times \frac{k_{1t3}}{T_0} + \frac{k_B}{q} \ln\left(\frac{K_2^{\eta_2} K_3^{\eta_1 - \eta_2}}{K_1^{\eta_1}}\right) \\ B &= (V_{0th1} - V_{0th2} - k_{1t1} + k_{1t2} - k_{2t2}V_{ref}) + \\ &\quad + \tfrac{\eta_1 - \eta_2}{\eta_3}(V_{ref} - V_{0th3} + k_{1t3}) \end{aligned} \quad (10)$$

To get temperature independent reference voltage, temperature coefficient must be zero (i.e. $A = 0$):

$$\ln\left(\frac{K_2^{\eta_2} K_3^{\eta_1 - \eta_2}}{K_1^{\eta_1}}\right) = \frac{q}{k_B T_0}\left(-k_{1t1} + k_{1t2} - k_{2t2}V_{ref} + \frac{\eta_1 - \eta_2}{\eta_3} \times k_{1t3}\right) \quad (11)$$

so:

$$\begin{aligned} V_{ref} = B &= (V_{0th1} - V_{0th2} - k_{1t1} + k_{1t2} - k_{2t2}V_{ref}) + \\ &\quad + \tfrac{\eta_1 - \eta_2}{\eta_3}(V_{ref} - V_{0th3} + k_{1t3}) \\ V_{ref} &= \frac{V_{0th1} - V_{0th2} + k_{1t2} - k_{1t1} + \frac{\eta_1 - \eta_2}{\eta_3}(k_{1t3} - V_{0th3})}{1 + k_{2t2} - \frac{\eta_1 - \eta_2}{\eta_3}} \end{aligned} \quad (12)$$

Eq. (11) is satisfied by adjustment of transistors aspect ratios ($K_1 - K_3$); consequently temperature-independent reference voltage would be achieved identical to Eq. (12).

Because of using self-biasing circuit with large length transistors (M_1–M_5), output voltage is almost independent of voltage of power supply. Two stack transistors to M_2, M_3 can be added to decrease line sensitivity in the cost of increasing minimum acceptable voltage for power supply (Vdd).

3 Simulation results

The proposed circuit has been designed in 0.18 μm 1P6M TSMC CMOS tech-

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nology and simulated by Cadence Spectre software. Table I shows the size of transistors used in the reference voltage circuit. Because the reference voltage is obtained by subtracting threshold voltages, M_1 has been chosen a high voltage (3 V) NMOS transistor with about 200 mV higher threshold voltage than normal NMOS transistor (2 V) to get a reference voltage ($\sim V_{0th1} - V_{0th2}$) more than 200 mV. Figures 2 (a) and (b) show reference voltage as a function of temperature and Vdd respectively, that indicate an accurate reference voltage with 0.4 mV (9.5 ppm/°C) variation related to temperature in the range of −40°C to 120°C and line sensitivity of 0.32 mV/V (1200 ppm/V).

Table I. Size of transistors

Transistor	M_1	M_2	M_3	M_4, M_5
W/L :(μm/μm)	1/10	3/10	0.5/20	1/20

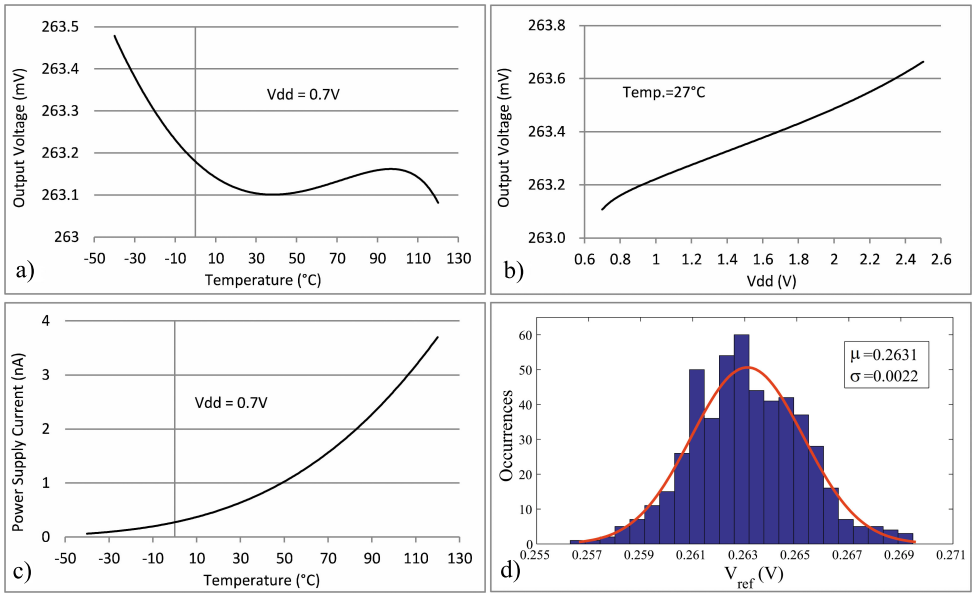

Fig. 2. a) Output voltage of reference circuit versus temperature, b) Output voltage of reference circuit versus Vdd, c) Power supply current versus temperature, d) Distribution of output voltage, as obtained from Monte Carlo simulation of 500 runs

Figure 2 (c) shows drawn current from power supply. Power consumption of circuit in room temperature is 400 pW (560 pA × 0.7 V).

To study the dependence of the output voltage on process variations, we performed Monte Carlo simulations of 500 runs. Figure 2 (d) shows the distribution of V_{ref} at room temperature. The average of V_{ref} is 263.1 mV with standard deviation of 2.2 mV. The coefficient of variation (σ/μ) is 0.84%. Figures 3 illustrates layout of the proposed reference voltage circuit with the active area of 500 μm^2 (21 μm × 24 μm).

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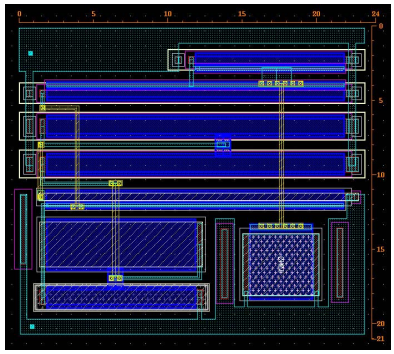

Fig. 3. Layout of the proposed voltage reference circuit

4 Conclusion

In this paper a high accuracy ultra-low power voltage reference circuit using sub-threshold operating MOSFETs was proposed and simulated. Table II shows the comparison between the designed circuit and some recent works. The circuit is featured with a small area of 500 μm^2 and low power consumption of merely 400 pW at room temperature. The performance of the proposed voltage reference circuit is highly precise with temperature inaccuracy of 0.4 mV in the range of -40°C to 120°C and line sensitivity of 0.32 mV/V in the range of 0.7 V to 2.5 V. Moreover, having a simple structure and using the same transistors in the current mirror (M_4, M_5), better coefficient of variation (σ/μ) toward process variation compared with [8] was obtained.

Table II. Comparison of reported voltage reference circuits with proposed one

	[5]	[6]	[7]	[8]	**[This Work]**
Vdd range (V)	0.9∼1.8	1.4∼3	∼3.6	0.45∼2	**0.7∼2.5**
Power Cons. @ room temp.	6 μW	300 nW	648 μW	2.6 nW	**400 pW**
$\overline{V_{ref}}$	0.55 V	745 mV	1.23 V	263.5 mV	**263.1 mV**
Temp. range (°C)	0∼100	-20∼80	-40∼120	0∼125	**-40∼120**
Inaccuracy vs. temp. (ppm/°C)	23	7	11.8	142	**9.5**
Line sens. (ppm/V)	2400	20	——	4400	**1200**
Coefficient of variation (σ/μ)	——	0.87%	——	3.9%	**0.84%**
Die area (μm^2)	20000	55000	100000	43000	**500**
Process	0.18 μm	0.35 μm	0.5 μm	0.18 μm	**0.18μm**

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