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Ultra-low voltage high-speed Schmitt trigger circuit in SOI MOSFET technology

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Abstract: This paper proposes a novel ultra-low voltage and high speed Schmitt trigger circuit designed in silicon-on-insulator (SOI) technology. The proposed circuit is designed using dynamic threshold MOS (DTMOS) technique and multi-threshold voltage CMOS (MTCMOS) technique to reduce power consumption and accomplish high speed operation. The experiment shows the proposed Schmitt trigger circuit consumes 4.68 μW at 0.7 V power supply voltage and the circuit demonstrates the maximum switching speed of 170 psec.

Keywords: SOI, Schmitt trigger, DTMOS, MTCMOS

Classification: Integrated circuits

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1 Introduction

Recently the emphasis on current VLSI design has shifted to high speed and low power due to proliferation of portable electronic systems. In the high speed and low power systems, Schmitt trigger circuit is widely used to reshape the signals under noisy conditions. Better noise margin and noise stable operation are offered by the hysteresis of the Schmitt trigger circuit. However, as power supply level scales down with technology, threshold voltage are to be scaled down to reduce electric field in VLSI systems, which in turn increases leakage current. Therefore, conventional Schmitt trigger circuits can not be operated in the ultra-low voltage less than 1 V which means a new technology and a design technique for the Schmitt trigger circuit needs to be developed to satisfy all the requirements.

SOI MOSFET has become more attractive than conventional MOSFET in designing VLSI circuits as a low power and high performance solution with features such as high current driving capability, low supply voltage, high current gain, and so on [1].

The disadvantage of the SOI MOSFET is its instability due to floating body and self-heating effect. In order to reduce this disadvantage, several techniques for the body-contact have been developed. Among them, dynamic threshold MOSFET (DTMOS) results in higher current driving capability than that of conventional CMOS. It gives higher operating speed at very low voltage below 0.7 V with little history effect. The typical DTMOS is made by connecting MOSFET gate to its floating body or MOSFET drain to its floating body [2].

Multi-threshold CMOS (MTCMOS) technology is a popular power gating approach that provides low leakage and high performance operation using low V_{th} transistors for logic cells and high V_{th} transistors for power switches [3].

This paper proposes a novel Schmitt trigger circuit using both the DTMOS technique and the MTCMOS technique implemented in the SOI technology to satisfy ultra-low voltage and high speed operation.

2 Circuit Description

The proposed Schmitt trigger circuit reduces unwanted state changing in electronic circuits with noisy inputs and operates at ultra-low voltage (0.7 V) for very low power consumption. Different switching voltage or switching time of the Schmitt trigger circuit causes the hysteresis which offers better noise margin and stable operation. The switching voltages of rising transition and falling transition can be determined by the ratio of each MOSFET [4].

Figure 1 (a) shows the proposed Schmitt trigger circuit, where DTMOS technique is used to reduce the operational voltage and threshold voltage. Also, MTCMOS technique with virtual V_{DD} node and virtual Ground node is used to make different switching threshold voltage (V_{stv}) in DC voltage transfer characteristics (VTC). Equation (1) presents the basic equation to

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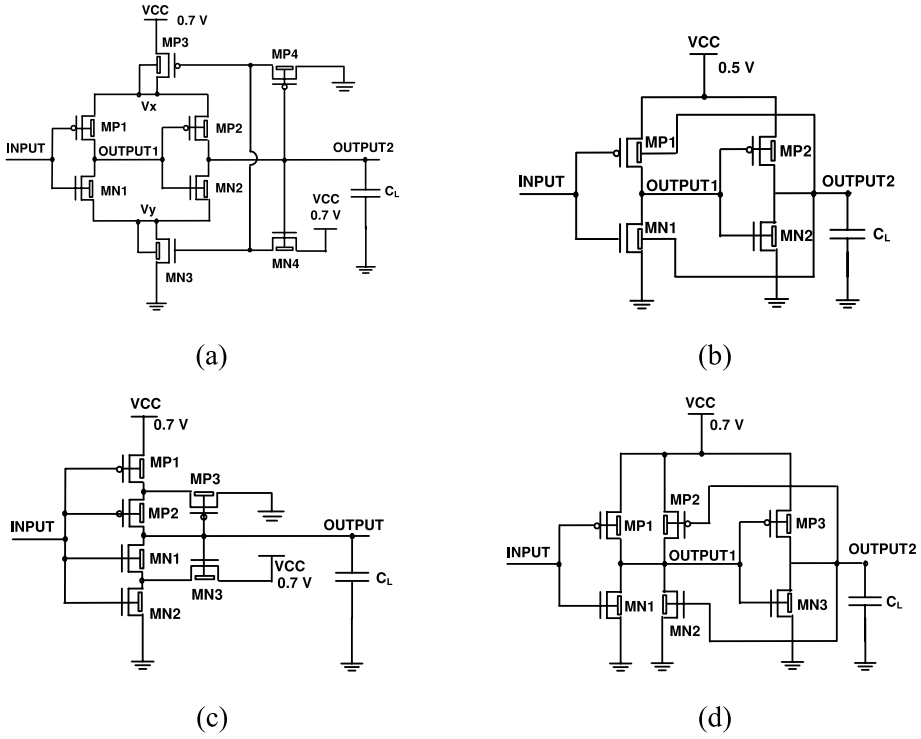

Fig. 1. Schmitt trigger circuits: (a) Circuit A **(proposed circuit)**, (b) Circuit B, (c) Circuit C, (d) Circuit D.

determine the inverter switching threshold voltage in saturation region [4].

$$I_D = \frac{\beta_n}{2}(V_{stv} - V_{tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{stv} - |V_{tp}|)^2 \tag{1}$$

where I_D is the drain current, V_{stv} is the switching threshold voltage, V_{DD} is input voltage, and β_p and β_n are transconductance parameters of N-MOSFET and P-MOSFET, respectively.

The key point of the proposed method is to apply the virtual V_{DD} (V_x) and virtual Ground (V_y) to Eq. (1) in each rising transition and falling transition of the output to make different V_{stv} in the transitions. The operation of the circuits is as follows.

The first case is for low-to-high transition of INPUT signal. When INPUT is logic LOW initially, MP1 is on-state, MN2 is on-state, MP4 is on-state, and finally MP3 is on-state. This determines V_x voltage which depends on the value of effective resistor of MP3, while V_y node is floating. As INPUT signal changes to logic HIGH, the high-to-low transition of OUTPUT1 is determined by the voltage of the V_y node to be set by MN4, the voltage of V_x to be set initially, and switching point of MP1/MN1 structure. The switching threshold voltage (V_{stv_hl}) can be determined from Eq. (1), and it is given by

$$I_D = \frac{\beta_n}{2}(V_{stv\_hl} - V_{y\_hl} - V_{tn})^2 = \frac{\beta_p}{2}(V_{x\_hl} - V_{stv\_hl} - |V_{tp}|)^2 \tag{2}$$

$$V_{stv\_hl} = \frac{1}{1+\sqrt{\frac{\beta_n}{\beta_p}}}(V_{x\_hl} - |V_{tp}|) + \frac{\sqrt{\frac{\beta_n}{\beta_p}}}{1+\sqrt{\frac{\beta_n}{\beta_p}}}(V_{y\_hl} + V_{tn}) \tag{3}$$

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where V_{x_hl} and V_{y_hl} are the virtual V_{DD}/Ground voltages, respectively, in case of the high-to-low transition of OUTPUT1.

The second case is for high-to-low transition of INPUT signal. The same equations can be used to determine the switching threshold voltage (V_{stv_lh}) in case of the low-to-high transition of OUTPUT1, and it is given by

$$V_{stv\_lh} = \frac{1}{1+\sqrt{\frac{\beta_n}{\beta_p}}}(V_{x\_lh} - |V_{tp}|) + \frac{\sqrt{\frac{\beta_n}{\beta_p}}}{1+\sqrt{\frac{\beta_n}{\beta_p}}}(V_{y\_lh} + V_{tn}) \tag{4}$$

where V_{x_lh} and V_{y_lh} are the virtual V_{DD}/Ground voltages, respectively, in case of the low-to-high transition of OUTPUT1.

Therefore, assuming that β_n is equal to β_p, the hysteresis width (V_{width}) is calculated as follows.

$$V_{width} = V_{stv\_hl} - V_{stv\_lh} = \frac{1}{2}\left[(V_{x\_hl} - V_{x\_lh}) + (V_{y\_hl} - V_{y\_lh})\right] \tag{5}$$

Equation (5) states that V_{width} depends on the difference between the virtual V_{DD}/Ground voltages of V_{stv_lh} and V_{stv_hl} cases. Assuming that each MOSFET is a resistor, V_x and V_y are given by

$$V_x = \frac{R_{MP3}}{R_{MP1} + R_{MP3}},\ V_y = \frac{R_{MN3}}{R_{MN1} + R_{MN3}} \tag{6}$$

Each resistance is determined by the size of each MOSFET and the operation region of each MOSFET, especially, the operation regions of MP3 and MN3 which are determined by MP4 and MN4, respectively. Therefore, V_{x_lh} and V_{x_hl} as well as V_{y_lh} and V_{y_hl} have different values depending on the sizes and the operation regions. The typical voltage difference is 0.25 V.

In the proposed circuit, all the MOSFETs are implemented using DT-MOS technique to connect gate node to floating body except MP3 MOSFET and MN3 MOSFET. It reduces threshold voltage in on-state and increases threshold voltage in off-state, which increases the speed of the circuit and decrease the leakage current of the circuit. The connection of drain node to floating body of MP3 MOSFET and MN3 MOSFET is required because they need high threshold voltage to reduce leakage current and the MOS capacitance. If the MOS capacitance is large, the OUTPUT2 does not provide rail-to-rail full swing. Experimentally, connecting drain to body gives smaller capacitance value than the case of connecting gate to body.

If high supply voltage is used in the circuit, MP4 and MN4 are not necessary. However, the Schmitt trigger should be operated in saturation region at very low voltage, which means the voltage variation of virtual V_{DD} and virtual Ground should be controlled carefully. Also, MP3 and MN3 should be used as resistor to set the voltage of the virtual nodes. The role of MP4 and MN4 is to operate MP3 and MN3 in linear region by making the gate voltage of the MP3 and MN3 lower than V_{DD}.

3 Conventional Schmitt Trigger Circuits in SOI MOSFET

Figure 1 (b), (c), and (d) show the well-known conventional Schmitt trigger circuits. In order to compare these circuits with the proposed circuit, all the

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circuits are converted into the circuits implemented in DTMOS.

Figure 1 (b) is the circuit proposed in [5] implemented in a standard CMOS process. If the circuit is implemented in SOI technology, its power is extremely small due to small size and the small number of MOSFET parasitic capacitors, however the propagation delay is longer because the input voltage of MP1 and MP2 are opposite to the voltages of the floating body of the MOSFETs. Whenever the input(gate) and body voltages change at the same time, the speed of SOI MOSFET is fastest because threshold voltage is lowered with the increase of gate bias as a result of floating body effect. The V_{stv} of the circuit depends on the change of the threshold voltages of MP1 and MN1, therefore the controllability of $Vstv$ is not good due to the small threshold voltage variation. The circuit shown in Fig. 1 (c) is presented in [6]. The V_{stv} of the circuit is set by ratioed operations of NMOS and PMOS transistors. It suffers from long transition time, large power dissipation by MN2 and MP3, and racing phenomena after starting transition [4, 7]. Finally, the circuit of Fig. 1 (d) makes use of voltage keeper structure to generate different V_{stv} [8]. It provides high speed switching by feedback structure, but dissipates a lot of power due to the short circuit and leakage current.

4 Experimental Results

The proposed circuit has been designed using Hspice in a 0.15 μm BSIM-SOI3.2 technology. This experiment uses an ideal saw waveform as the input signal whose voltage is 0.7 V with 20 fF for the load capacitor C_L.

Figure 2 (a) shows the DC VTC of the proposed circuit close to the ideal DC VTC of Schmitt trigger circuit. It shows that High-to-Low switching threshold voltage (V_H) is 0.42 V and Low-to-High switching threshold voltage (V_L) is 0.28 V. The input waveform and output1 waveform shown in Fig. 2 (b) present high switching speed and low delay.

Table I shows the power and performance data of each Schmitt trigger in SOI technology shown in Fig. 1 for comparison with the proposed design in this paper. In the experiment, V_H (0.42 V) and V_L (0.28 V) of each circuit is the same, and only difference is that the supply voltage of the Circuit B is 0.5 V in order to set the V_H and V_L to the same value. In terms of power dissipation, the circuit B is lowest as expected in the previous section. Except the circuit B, the proposed circuit A dissipates the lowest power, and circuit D has the highest power dissipation. In propagation delay, the proposed circuit A has the lowest time, while as circuit B has the highest time. Circuit B and circuit C cannot follow the input transition time below 1 nsec. Circuit A operates well over 0.4 nsec input transition time and circuit D works around at 0.2 nsec input transition time. Finally, circuit A to circuit C have almost ideal switching speed in DC VTC, however circuit D has low switching speed.

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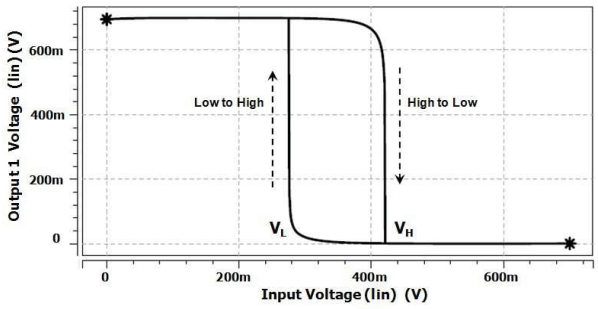
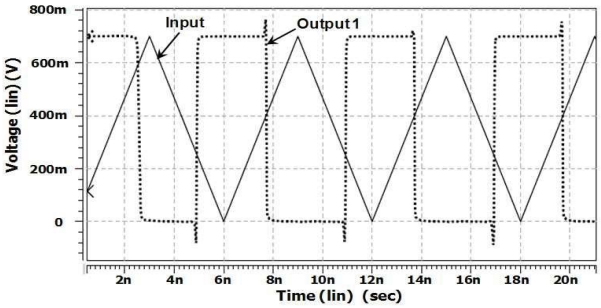


(a)



(b)

Fig. 2. Simulation results of the proposed circuit (Circuit A) (a) DC voltage transfer characteristics, (b) INPUT waveform and OUTPUT1 waveform.

Table I. Power and performance comparison.

	Circuit A **Proposed**	Circuit B [5]	Circuit C [6]	Circuit D [8]
Power Dissipation	$4.68\,\mu W$	$1.66\,\mu W$	$5.14\,\mu W$	$7.39\,\mu W$
Propagation Delay	$170\,psec$	$770\,psec$	$750\,psec$	$340\,psec$
Minimum transition time of Input waveform	$0.40\,nsec$	$1.00\,nsec$	$1.00\,nsec$	$0.20\,nsec$

5 Conclusion

A new ultra-low voltage and high speed Schmitt trigger circuit in SOI MOSFET technology is presented and simulated. Three conventional Schmitt trigger circuits are converted to SOI MOSFET circuits, and simulated to compare with the proposed circuit. The experimental results of the simulation show the proposed Schmitt trigger is the best structure in terms of power and performance. This means the proposed circuit has extreme value in low power and high speed application.

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