

A low-power wideband multi-frequency synthesizer for mobile TV tuner ICs

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Abstract: A low-power wideband frequency synthesizer that generates multiple LO frequencies for mobile TV tuner ICs is presented. The synthesizer utilizes a single on-chip LC VCO and an odd-order frequency division technique to achieve both low power and small silicon area. The integrated LC VCO has a tuning range of 2.3 to 3.85 GHz. With a division ratio of 2, 4, 6, 12, 16, 24, and 32, the LO generation block supports FM, VHF III, UHF, Europe-L, and USA-L bands. The measured LO phase noise for the L-band is under -79 dBc/Hz at an offset of 10 kHz. The synthesizer implemented in $0.18\text{-}\mu\text{m}$ CMOS technology occupies an area of about 1.2 mm^2 and dissipates up to 33.5 mW from a 1.8-V supply.

Keywords: frequency synthesizer, LC VCO, IC, frequency division

Classification: Integrated circuits

References

- [1] P. Antoine, P. Bauser, H. Beaulaton, M. Buchholz, D. Carey, T. Cassagnes, T. K. Chan, S. Colomines, F. Hurley, D. T. Jobling, N. Kearney, A. C. Murphy, J. Rock, D. Salle, and C.-T. Tu, “A direct-conversion receiver for DVB-H,” *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2536–2546, Dec. 2005.
- [2] M. Marutani, H. Anbutsu, M. Kondo, N. Shirai, H. Yamazaki, and Y. Watanabe, “An 18 mW 90 to 770 MHz synthesizer with agile auto-tuning for digital TV-tuners,” *IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, pp. 681–682, Feb. 2006.
- [3] Y. Kim, J. Kim, V. N. Parkhomenko, D. Baek, J. Lee, E. Sung, I. Nam, and B. Park, “A multi-band multi-mode CMOS direct-conversion DVB-H tuner,” *IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, pp. 608–609, Feb. 2006.
- [4] N. Itoh, “A study of capacitor-coupled varactor VCO to investigate flicker noise up-conversion mechanism,” *IEEE Int. Workshop RF Integration Technol.*, Singapore, pp. 157–160, Nov. 2005.
- [5] R. Magoon and A. Molnar, “RF local oscillator path for GSM direct conversion transceiver with true 50% duty cycle divide by three and active

- third harmonic cancellation,” *IEEE Radio Freq. Integrated Circuits Symp.*, pp. 23–26, June 2002.
- [6] Y. Yang, F. Lee, and S. Lu, “A single-VCO fractional-N frequency synthesizer for digital TV tuners,” *IEEE/MTT-S Int. Microw. Symp.*, pp. 1545–1548, June 2007.
- [7] B. Razavi, “Multi-decade carrier generation for cognitive radios,” in *Proc. Symp. VLSI Circuits*, pp. 120–121, 2009.

1 Introduction

To support various mobile TV standards (e.g., digital video broadcasting-handheld (DVB-H), terrestrial digital multimedia broadcasting (T-DMB), and integrated services digital broadcasting-terrestrial (ISDB-T)) with low cost and low power consumption, a low-power mobile TV tuner IC is essential for battery-powered handheld devices. In order to support these standards simultaneously, multiple LC-tank VCOs (LC VCOs) and complex LO frequency generation techniques are usually required for multiple frequency generation [1, 2, 3]. Since these conventional synthesizer architectures may increase the chip size and power consumption, these are not suitable for use in hand-held mobile TV tuner ICs that demand low power as well as compact silicon area.

In this letter, we present a new low-power, compact, wideband CMOS frequency synthesizer that can simultaneously generate multi-band LO frequencies supporting FM (88 to 108 MHz), VHF III (170 to 240 MHz), UHF (470 to 862 MHz), Europe-L (1452 to 1492 MHz), and USA-L (1670 to 1675 MHz) bands. To achieve both low power and small area, the proposed synthesizer utilizes a single LC VCO and adopts an odd order frequency division technique using differential CMOS divided-by-3 (DIV3) circuits.

2 Circuit design

A block diagram of the proposed frequency synthesizer is shown in Fig. 1 (a). It consists of the following circuit blocks: a fractional-N PLL frequency synthesizer with an on-chip LC VCO and an off-chip loop filter; a VCO buffer; and an LO generation block consisting of a MUX, five divide-by-2 (DIV2) dividers, and a divide-by-3 (DIV3) divider. Frequency division is controlled using control switches (S1~S8) and the DIV3 divider is turned on (by S2) to enable odd-order frequency division for a division ratio of 6, 12, and 24. The entire circuit, except the off-chip second order loop filter, is fully integrated on a chip using 0.18- μ m CMOS technology.

Fig. 1 (b) shows the integrated single LC VCO circuit, consisting of a cross-coupled CMOS Gm-cell, an on-chip inductor L , a varactor, and a 6-bit binary-weighted switched capacitor array (SCA). The LC VCO has a tuning range of 2.3 to 3.85 GHz, which is controlled by the 6-bit SCA and AMOS varactor. To achieve a high Q-factor of over 20, a single-turn inductor with a width of 30 μ m is used. An adaptive frequency calibration technique is used

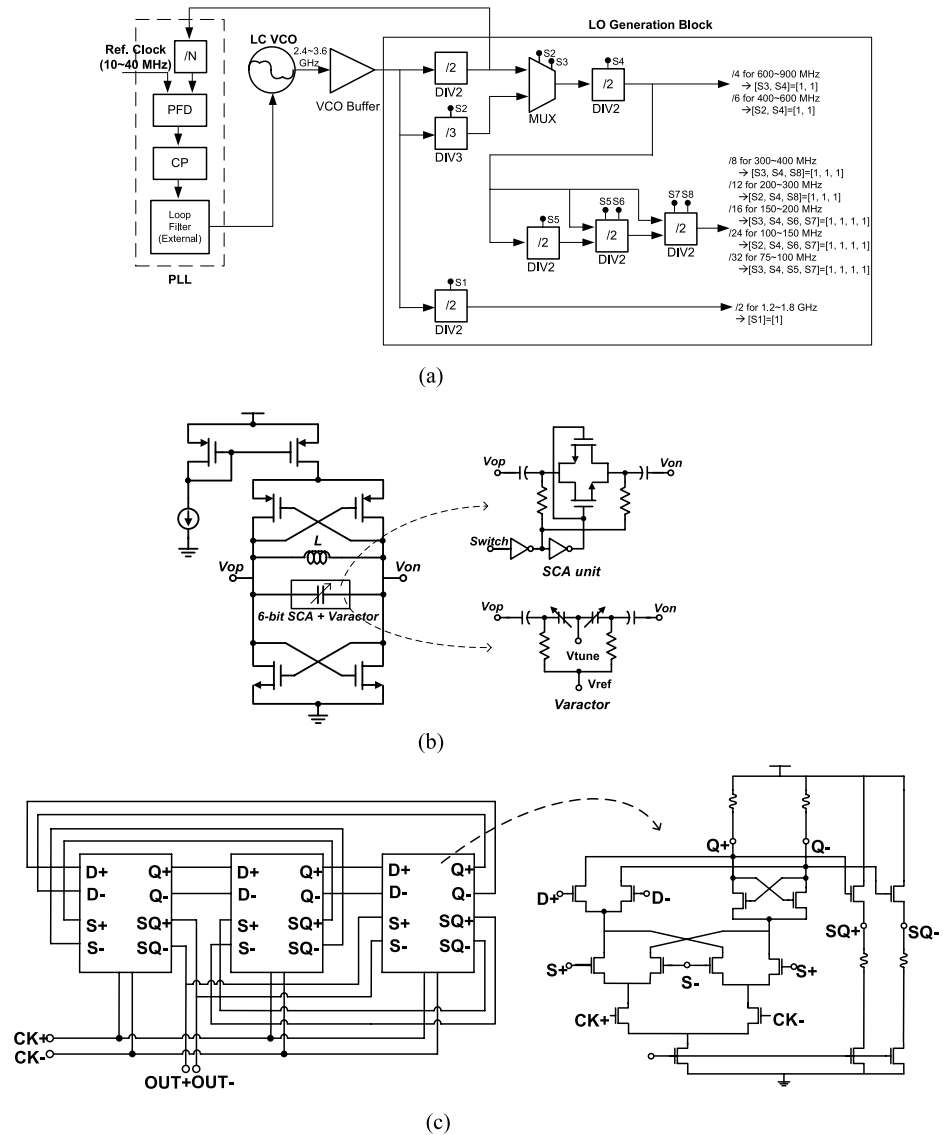


Fig. 1. (a) Proposed frequency synthesizer architecture, (b) Simplified LC VCO, and (c) Divide-by-3 (DIV3) architecture and unit circuit

for coarse tuning, which is controlled by the 6-bit binary-weighted SCA with NMOS switches. The accumulation MOS (AMOS) varactor is used for fine tuning. The use of both MIM capacitors and the varactor makes the circuit less sensitive to the AM-FM phase noise generated by the oscillator core and the supply noise [4].

The output of the LC VCO is buffered through a VCO buffer and then divided with a division ratio of 2, 4, 6, 12, 16, 24, and 32 for each band. To generate a wide LO frequency range from 75 MHz to 1.8 GHz with low power and silicon area, a simple odd-order frequency division technique is used for a division ratio of 6, 12, and 24. Five differential DIV2 circuits and a differential DIV3 circuit are cascaded together according to the control signals of S1~S8, as shown in Fig. 1 (a). By virtue of the characteristics of the DIV2 and DIV3 circuits generating a 50% duty cycle clock, quadrature-phase LO clocks are easily generated without using a complex phase trimming

circuit. The DIV2 circuit is realized using conventional differential CML-type D flip-flops. As compared to single-ended DIV3 circuits implemented in BJTs [5], the differential CMOS DIV3 architecture shown in Fig. 1 (c) generates a 50% duty cycle clock with much less power and area but with higher signal integrity.

3 Experimental results

The proposed frequency synthesizer is implemented using 1-poly 6-metal 0.18- μm CMOS technology and packaged for measurement in a micro etched leadless package (μELP). A microphotograph of the chip with a die area of about 1.2mm^2 is shown in Fig. 2(a). Fig. 2(b) shows the measured frequency tuning characteristics of the LC VCO. The tuning range of the VCO is from 2.3 to 3.85 GHz (50.4%). The VCO gain ranges from 21 to 86 MHz/V. Fig. 2 (c) shows the measured phase noise characteristics of the frequency synthesizer for each frequency. The measured LO phase noise for the L-band is under -79dBc/Hz and -95dBc/Hz at offset frequencies of 10 kHz and

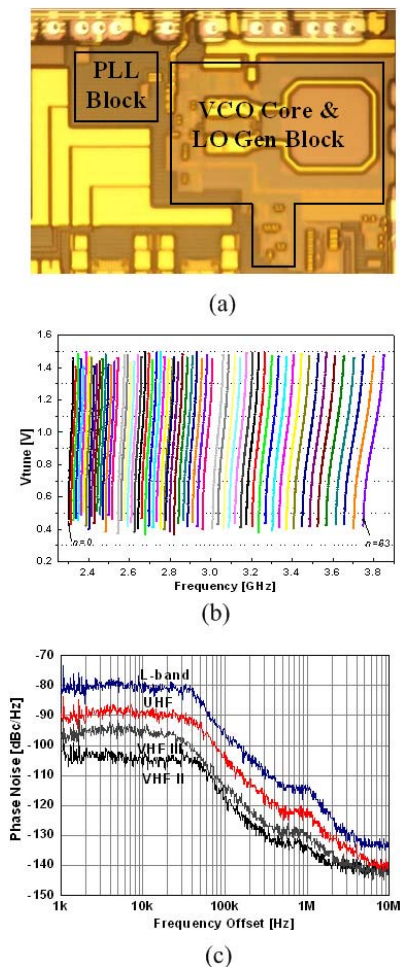


Fig. 2. (a) Chip microphotograph, (b) Measured overall VCO tuning range for Vtune v.s. oscillation frequency, and (c) Measured phase noise of different frequencies (VHF II, VHF III, UHF, and L-band)

100 kHz, respectively. The proposed synthesizer dissipates up to 33.5 mW from a 1.8-V supply, which is only 1/5 of that dissipated by the conventional single-VCO synthesizers used in digital TV tuners [6]. The detailed performance results are summarized and compared with other recently published synthesizers [1, 2, 6, 7] in Table I. [1] uses three VCOs and consumes 47 mW to cover a frequency range from 430 to 1000 MHz. [2] uses two VCOs and consumes around 20 mW with a largest die area of about 1.9 mm² to cover a frequency range from 90 to 770 MHz. [7] introduced a new carrier generation technique using a bimodal quadrature oscillator and three divider changes to produce carrier frequencies in the range of 1 to 10 GHz. However, it is not appropriate to directly compare [7] with this work, since [7] does not use a PLL. Also, the power dissipation of [7] is about 31 mW without a PLL. Therefore, this work is superior to other references in terms of its small power and area overhead as well as the largest frequency range.

Table I. Performance Summary and Comparison

	[1]	[2]	[6]	[7]	This work
Supply voltage	2.775V (UHF band)	1.2V	2.2V	N/A	1.8V
DC current	17mA (UHF band)	15.3~16.9mA	70	N/A	16~18.6mA
Power dissipation	47mW	18~20mW	154mW	31mW(except PLL)	28.8~33.5mW
Chip area	N/A	1.9mm ² (w/LPF)	1.5 mm ²	0.29mm ²	1.2 mm ²
Freq range	430-1000MHz	90-770MHz	90-862MHz	1-10GHz	75-900MHz, 1.2-1.8GHz
Technology	0.35um SiGe	0.11um CMOS	0.18um CMOS	90nm CMOS	0.18um CMOS
Phase noise (dBc/Hz) / Integrated phase noise (10 Hz ~ 4 MHz)					L-band: -79 @10 KHz, -116 @1.25 MHz, 1.5° rms // UHF: -90 @10 kHz, -124 @ 1.25 MHz, 0.6° rms // VHF III: -95 @10 kHz, -134 @ 1.25 MHz, 0.2° rms // VHF II: -107 @10 kHz, -136 @ 1.25 MHz, 0.1° rms

4 Conclusion

To support multiple LO frequencies for use in multi band mobile TV tuner ICs, a low-power small-area frequency synthesizer implemented in 0.18-μm CMOS technology is presented in this letter. By using a single on-chip LC VCO with a tuning range of up to 3.85 GHz and an odd-order frequency division technique, the LO generation block can be used to achieve division ratios of 2, 4, 6, 8, 12, 24, and 32 with small area and low power consumption.

The LO frequency ranges from 75 MHz to 1.8 GHz, which covers DVB-H, T-DMB, and ISDB-T simultaneously. With a die area of about 1.2 mm², the synthesizer dissipates around 33.5 mW, which is suitable for use in compact mobile TV tuner ICs for multiband and multimode devices.