ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.12, 1–9

Hamming network circuits based on CMOS/memristor hybrid design

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Abstract: Memristor, as an innovative technology, has been proposed in the application of neural networks since its physical implementation was reported by HP lab. In this paper, we proposed a Hamming network circuits based on CMOS/memristor hybrid design which is compact in device size and circuit structure. Through HSPICE simulation, pattern recognition and classification functions of hamming network circuits are demonstrated using a 16×16 nanocrossbar memory.

Keywords: hamming network, memristor, nanocrossbar, neural networks

Classification: Electron devices, circuits, and systems

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DOI: 10.1587/elex.10.20130404
Received May 28, 2013
Accepted June 04, 2013
Publicized June 12, 2013
Copyedited June 25, 2013

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1 Introduction

After the hot wave of research in 1990s, hardware neural network has entered into an stage of slow and incremental progressing [1]. One main challenge for implementing large scale neural networks using traditional VLSI technology is that the hardware resource needed is massive and the interconnection is complex, which may even overshadowed the profits it achieved. However, in recent years, this domain has again attracted people's attention for reasons of many aspects [2], the most important one of which is that technology innovations bring new opportunities to the hardware implementation of neural networks.

Memristor is such an innovative technology, which represents the latest achievement of nanoelectronics. Since its physical implementation was reported by HP lab using two-terminal titanium dioxide nanoscale device [3], memristor has been proposed in the application of neural networks [4]. Its high density potential conforms to the requirement of constructing large scale neural networks. Its memory property has been demonstrated to be similar to that of bio-synapse [5]. Meanwhile, memristor array organized in a nanocrossbar structure [6] provides abundant connectivity and benign scalability for implementing neural networks with highly interconnected nanowires. Besides, it is worth noting that fabrication process of the CMOS/memristor hybrid design has already been demonstrated experimentally [7]. All these merits make memristor an ideal candidate for implementing neural networks circuit.

In this paper, a CMOS/memristor hybrid circuit design is proposed for implementing Hamming network, a typical neural network model [8]. Here, by referring to the term memristor, we mean a variety of threshold type memristive devices which show a threshold voltage behavior [5]. Our design utilizes a nanocrossbar memory as the core component, based on the observation that nanocrossbar is a relatively mature fabrication process of integrating memristor devices, and many researches have been proposed considering its circuit design issue [9, 10]. Through HSPICE simulation, pattern recognition and pattern classification function of Hamming network are demonstrated using a 16×16 nanocrossbar memory.

DOI: 10.1587/elex.10.20130404
Received May 28, 2013
Accepted June 04, 2013
Publicized June 12, 2013
Copyedited June 25, 2013

2 Hamming network circuits structure

Hamming network is a maximum likelihood classifier which selects from a group of exemplar patterns the closest one to an input pattern [8]. All the exemplar patterns and the input pattern are represented in the form of one-dimensional binary vector. When an input pattern $P = (p_1, p_2, \ldots, p_N)$ is presented to the network, the Hamming network firstly calculates matching scores between the input pattern and each exemplar pattern $W_i = (w_{i1}, w_{i2}, \ldots, w_{iN})$ $(1 \leq i \leq M)$, which is defined as follow:

$$\begin{aligned} MS_i &= N - HD(P, W_i) \\ &= N - \sum_{j=1}^{N} |P_j - W_{ij}| \end{aligned} \tag{1}$$

where $HD(P, W_i)$ is the Hamming distance between input pattern P and exemplar pattern W_i, P_j is the j-th element of input pattern $P(1 \leq j \leq N)$, W_{ij} is the j-th element of exemplar pattern W_i. After that, a WTA (winner-take-all) operation is performed to the matching score, where only the winner (the maximum matching score) will be indicated by a high level output, given by (2):

$$U_i = \begin{cases} 1, i = i^* \\ 0, i \neq i^* \end{cases} \tag{2}$$

where $MS_{i^*} \geq MS_i, \forall i$.

In the remaining part of this section, we will introduce structure and function of the circuits designed to implement the above-mentioned Hamming network model.

2.1 Feedforward layer circuit

Here, we describe the design of the feedforward layer circuit which performs the function of computing matching scores as defined in (1).

Feedforward layer circuit is composed of a nanocrossbar and its corresponding peripheral CMOS circuits. The gray area shown in Fig. 1 indicates the nanocrossbar structure. The blocks at the top and right of the nanocrossbar are programming circuits which are used to write and erase a nanocrossbar memory. The programming method has been proposed in our previous research [10], and will not be discussed later.

In the nanocrossbar, each column is used to store one exemplar pattern. Each memristor is programmed to either R_{ON} state or R_{OFF} state. However, the bit representation is different from traditional memristor memory. Here, we use a pair of memristors which are complementary in logic state to represent one bit. The definition of logic value depends on designer. In this paper, we use the resistance combination (R_{ON}, R_{OFF}) to represent logic 1, and (R_{OFF}, R_{ON}) for logic 0. Take a 3-bit exemplar pattern $(1, 1, 0)$ for instance, six memristors (three pairs) within a column are needed. Their resistance state in turn is R_{ON}, R_{OFF}, R_{ON}, R_{OFF}, R_{OFF}, R_{ON}.

For input pattern, logic value is represented by voltage signals input to the nanocrossbar from the left side, as shown in Fig. 1. Similar to the representation of exemplar pattern, a complementary voltage signal is generated

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Received May 28, 2013
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Copyedited June 25, 2013

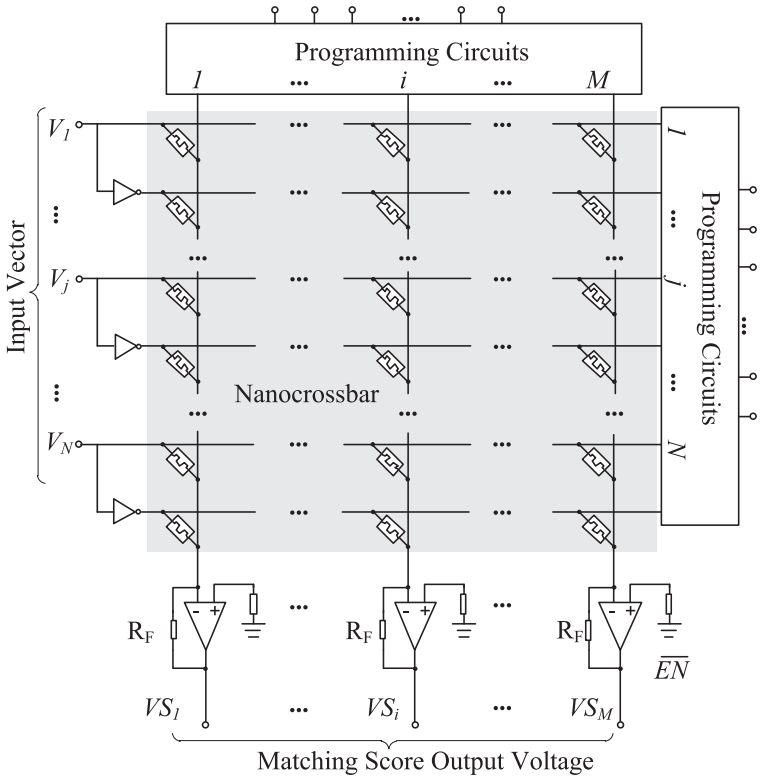

Fig. 1. Circuit structure of feedforward layer which is composed of a nanocrossbar (gray area) and peripheral CMOS circuits.

to form a logic combination with the original input bit. According to the previous definition of logic value, voltage combination (V_H, V_L) is defined as logic 1, and (V_L, V_H) as logic 0. V_H is a small voltage bias which is able to induce a detectable current through a memristor, and V_L is set to 0 V.

When an input pattern is presented to the nanocrossbar, operational amplifier (OPA) circuits working at reverse feedback state connect each vertical nanowire to virtue ground and collect current flowing through each column, as shown in Fig. 1. Amplitude of the input signals is set to be smaller than threshold voltage of the memristor so that their states remain unchanged. For the j-th input bit, if it matches the j-th bit of the i-th exemplar pattern (no matter if it is logic "1" or "0"), the current through the memristor pair is given by:

$$I_{ij} = V_H/R_{ON} + V_L/R_{OFF} = I_{ON} \tag{3}$$

where $I_{ON} = V_H/R_{ON}$. If the j-th input bit mismatches the j-th bit of the i-th exemplar pattern, the current through the memristor pair is given by:

$$I_{ij} = V_L/R_{ON} + V_H/R_{OFF} = I_{OFF} \tag{4}$$

where $I_{OFF} = V_H/R_{OFF}$. For the i-th column of memristors, the output voltage of the OPA circuit can be calculated by:

$$\begin{aligned} VS_i &= -R_F \cdot \sum_{j=1}^{N} I_{ij} \\ &= -R_F \cdot (MS_i \cdot I_{ON} + (N - MS_i) \cdot I_{OFF}) \end{aligned} \tag{5}$$

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Copyedited June 25, 2013

where R_F is the feedback resistor of the OPA circuit. Usually I_{ON} is hundreds to thousands times of I_{OFF}, thus I_{OFF} can be omitted, leading to an approximate proportional expression of matching score:

$$VS_i = -R_F \cdot I_{ON} \cdot MS_i \tag{6}$$

2.2 WTA circuit

WTA (winner-take-all) layer circuit is shown in Fig. 2. Output voltage signals from feedforward layer are firstly converted to current signals using voltage-current converter circuit. Then the current signals are input into a current-mode WTA circuit which picks out the maximum current input by giving an output voltage Vo_i $(1 \leq i \leq M)$ obviously higher than the other outputs. Thus, winner-take-all function as indicated by (2) is accomplished.

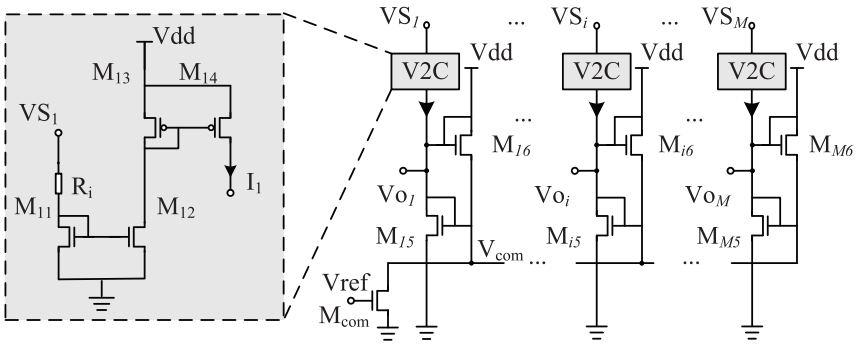

Fig. 2. WTA Circuits. The inset shows the voltage-current converter circuit. [11, 12].

This current-mode WTA circuit was proposed by C. Mead et al. [11], and modified to voltage-mode version by A. Fish et al. [12]. Here we adopt this circuit as the WTA layer of our Hamming network design. In this way, the network identifies the most approximate exemplar pattern(s) to the input pattern.

3 Simulation and analysis

To support our design, in this section, a SPICE simulation on the designed Hamming network circuits using a 16×16 nanocrossbar is introduced. The memristor model used for simulation is based on the SPICE model of [13]. The parameters are set to: $V_p = 1.2\,\text{V}$, $V_n = 0.6\,\text{V}$, $A_p = 5$, $A_n = 30$, $x_p = 0.7$, $x_n = 0.8$, $\alpha_p = 4$, $\alpha_n = 24$, $a_1 = 2.3 \times 10^{-4}$, $a_2 = 3.8 \times 10^{-4}$, $b = 0.04$, according to [13]. The OPA circuit is implemented using an ideal behavioral model, and the feedback resistor R_F is set to $33\,\text{k}\Omega$. V_H is a pulse of $-0.5\,\text{V}$ in amplitude and 1 us in width. Resistance of memristors are initialized to their corresponding states before simulation begins, and remains unchanged during simulation. According to the SPICE model, the memristor's state variable is set to either 0.01 or 0.999, corresponding to a high resistive state R_{OFF} of about $6.58\,\text{M}\Omega$ and a low resistive state R_{ON} of

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Copyedited June 25, 2013

Table I. Exemplar patterns used in simulation.

Column No.	Pattern bits	Column No.	Pattern bits
1	1 0 0 0 0 0 0 0	9	0 1 1 1 1 1 1 1
2	1 1 0 0 0 0 0 0	10	0 0 1 1 1 1 1 1
3	1 1 1 0 0 0 0 0	11	0 0 0 1 1 1 1 1
4	1 1 1 1 0 0 0 0	12	0 0 0 0 1 1 1 1
5	1 1 1 1 1 0 0 0	13	0 0 0 0 0 1 1 1
6	1 1 1 1 1 1 0 0	14	0 0 0 0 0 0 1 1
7	1 1 1 1 1 1 1 0	15	0 0 0 0 0 0 0 1
8	1 1 1 1 1 1 1 1	16	0 0 0 0 0 0 0 0

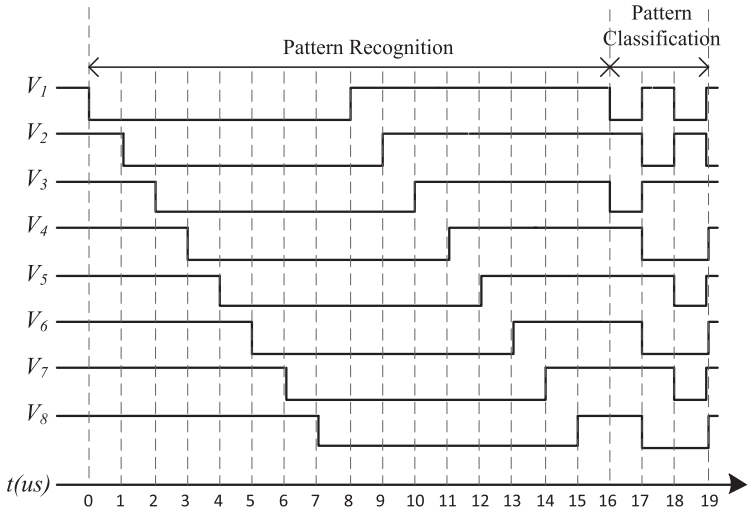

Fig. 3. Input voltage waveform.

about 65.85 kΩ, respectively. The exemplar patterns stored in each column are shown in Table I.

Input patterns which exactly matches one of the exemplar patterns are presented to the Hamming network circuits in turn, as shown in Fig. 3. Output waveform of column 1, column 2 and column 16 are selected to be shown in Fig. 4. It can be seen that the columns output a high level voltage at their corresponding input cycle and much lower voltages when other patterns are presented. Voltage output distribution of the circuits when exemplar pattern No. 6 and No. 10 are chosen as input are shown in Fig. 5. The x-coordinate of the graph indicates the column number, while the y-coordinate shows the output voltage at the corresponding terminal. It can be seen that both input patterns have been recognized correctly by a maximum voltage output. The second closest exemplar patterns to the input pattern with a Hamming distance of 1 output a much lower voltage. Output of the other cases resemble these two examples in amplitude while differ in distribution.

Pattern classification function is examined by presenting random chosen input pattern. Here, three different random input patterns, $(1,0,0,1,1,1,1,1)$, $(1,0,1,0,0,0,0,0)$, $(0,1,0,1,0,1,0,1)$, are input to the circuits, respectively, as shown in Fig. 3. The results of the simulation show that all the

DOI: 10.1587/elex.10.20130404
Received May 28, 2013
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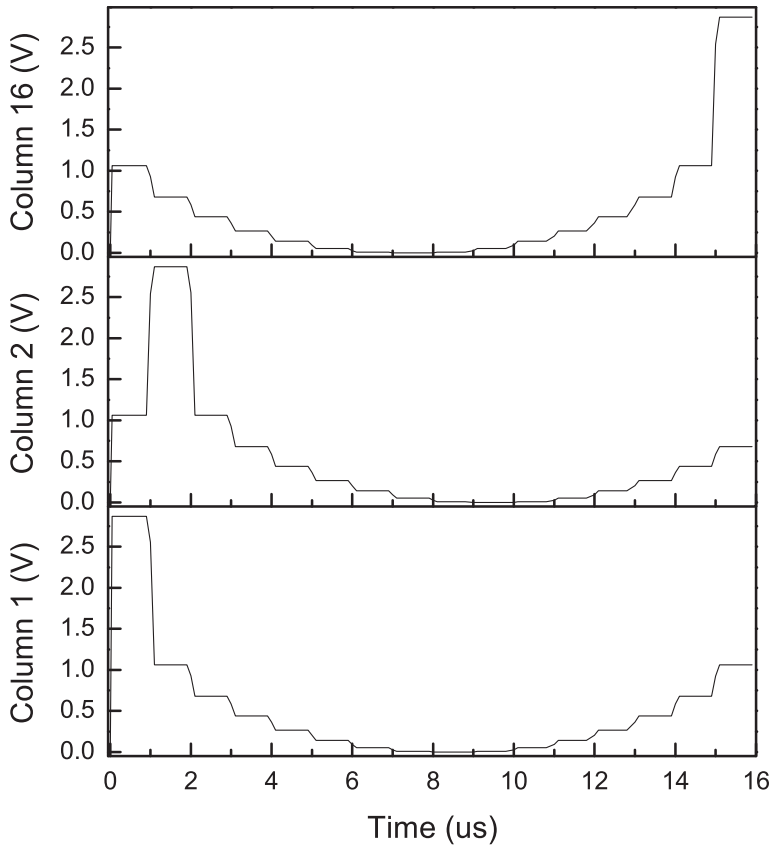

Fig. 4. Output voltage of column 1, 2 and 16 when exemplar patterns are presented in turn.

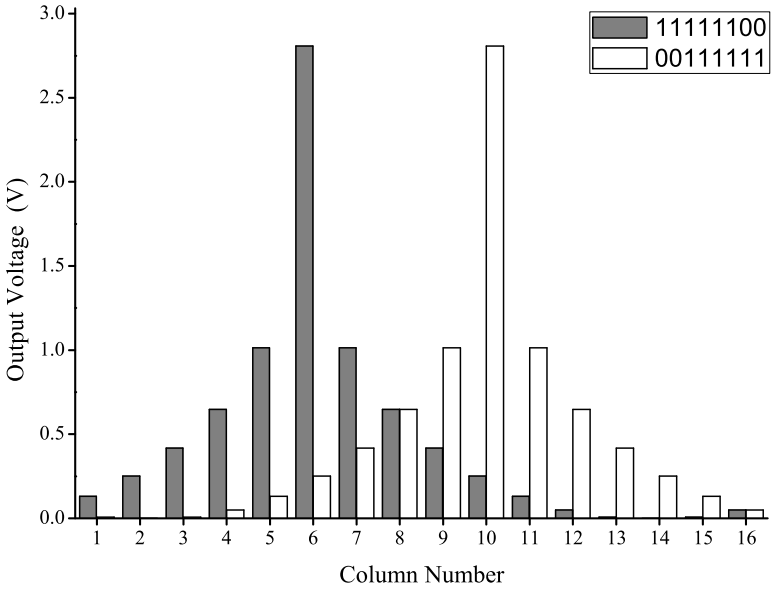

Fig. 5. Voltage output of each column when pattern "11111100" (gray) and "00000011" (white) are presented to the circuit, respectively.

patterns have been classified to the correct exemplar pattern which is the closest to them, as shown in Fig. 6. For input pattern $(1, 0, 0, 1, 1, 1, 1, 1)$, exemplar pattern No. 11 $(0, 0, 0, 1, 1, 1, 1, 1)$ has the smallest Hamming distance

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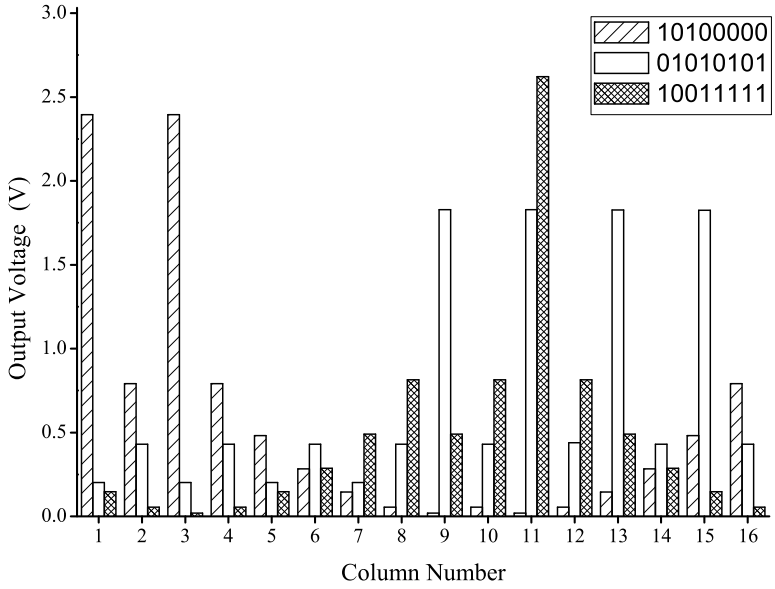

Fig. 6. Voltage output of each column when pattern "10100000", "01010101" and "10011111" are presented to the circuit, respectively.

($HD = 1$) to it. Thus, it is distinguished from other exemplar patterns. For input pattern $(1, 0, 1, 0, 0, 0, 0, 0)$, exemplar pattern No. 1 and No. 3 have the same smallest Hamming distance ($HD = 1$), and they both are distinguished from the other patterns. For input pattern $(0, 1, 0, 1, 0, 1, 0, 1)$, exemplar pattern No. 9, No. 11, No. 13 and No. 15 all have the smallest Hamming distance ($HD = 3$), and they are all distinguished from the other patterns.

4 Discussion and conclusion

Here, we would like to discuss some related aspects that are not fully covered in this paper. First of all, circuit overhead issue may be questioned that too much area are needed to implement the peripheral analog circuit, and that density benefit of memristor may lost. Let us make a conservative assumption that about 100 transistors are need to implement the peripheral OPA circuit and the WTA circuit for each column of memristors. For patterns that are 64-bit long, the average hardware cost for implementing one bit is two memristors plus no more than two transistors, far less than traditional CMOS method [14, 15] where at least one SRAM unit consisted of six transistors is used to store one bit.

Secondly, the circuit shows benign tolerance to memristors' conductance variety which will probably happen due to unmature fabrication process as well as unprecise programming process. Lacking sufficient experimental data, it is reasonable to assume that the conductance of both OFF and ON state obey a Gaussian distribution or a uniform distribution. It is distinct from (5) that positive errors and negative errors of I_{ON} through different memristors will counteract when they are summed up, weakening the effect of parameter distribution.

In summary, we have proposed an approach for implementing Hamming

DOI: 10.1587/elex.10.20130404
Received May 28, 2013
Accepted June 04, 2013
Publicized June 12, 2013
Copyedited June 25, 2013

network based on CMOS/memristor hybrid circuit design. A complementary memristor pair is used to store one bit of an exemplar pattern. Through HSPICE simulation, pattern recognition and classification functions of Hamming network are demonstrated on a 16×16 nanocrossbar memory.

Acknowledgments

The authors would like to thank Dr. M.T. Deng of Lund University for his useful comments and suggestions. This work was supported by NSFC project of China (Grant No.61003082 and Grant No.60921062).

DOI: 10.1587/elex.10.20130404
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