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ReRAM technology; challenges and prospects

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Abstract: We review recent progresses in Resistive Random Access Memory (ReRAM) technologies together with difficult challenges and prospects. ReRAM is one of the most promising emerging nonvolatile memories, in which both electronic and electrochemical effects play important roles in the nonvolatile functionalities. First, a brief historical overview of the research is provided. The technological overview is reported with the epoch-making achievements. Second, the current understanding in terms of the operation mechanism is shown followed by the technical assessment, especially the advantages of ReRAM. Finally, we summarize the challenges facing the ReRAM technology and the prospects.

Keywords: nonvolatile memories, resistance switching, functional oxides, electrochemical devices, redox reaction

Classification: Electron devices, circuits, and systems

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1 Introduction

Functional oxides, which show various novel electronic phenomena, such as resistance switching, have been intensively investigated as emerging research materials in the field of nano-electronics [1, 2]. One of the most promising applications is Resistive Random Access Memory (ReRAM), consisting of the functional-oxide layer sandwiched by metal electrodes, namely Metal/Oxide/Metal (MOM) structure (Fig. 1). Why is ReRAM the up-and-coming candidate in emerging nonvolatile memories? The biggest advantage of ReRAM technology is its good compatibility with CMOS technologies. Much of our knowledge about current semiconductor technologies is applicable to the development of ReRAM. As will be discussed below, the scaling merit will work in terms of the low-power consumption of the ReRAM operation. These two advantages will bring a strong cost competitiveness to ReRAM. In this contribution, the brief historical overview and the epoch-making achievements in ReRAM technologies are reported in section 2. In section 3, the current understanding of the operation mechanism is given followed by the technological assessment. Finally, the paper is concluded in section 4, by showing the difficult challenges and the prospect facing the

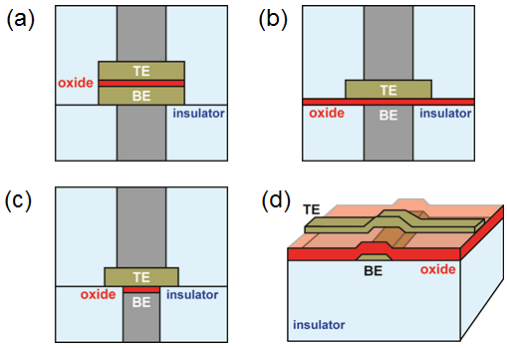

Fig. 1. Various ReRAM devices. (a) Typical MOM simple stacking structure. (b) The memory cell on the metallic via as a bottom electrode. (c) The oxidized via material for the resistance switching oxide layer. (d) The cross-bar structure.

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practical application of the ReRAM technology.

2 Historical overview and epoch-making achievements

2.1 Technical glossaries

Two operation modes and the technical terminology for ReRAM are shown in Fig. 2. Figs. 2 show unipolar and bipolar operations of HfO_x-based ReRAM with the bottom electrode of TiN and the top electrode consisting of Pt and Ti, respectively. By changing the combination of the oxide and the electrode, it is possible to change the stable operation mode of the ReRAM device. In the case of Fig. 2 (a), the high resistance state (HRS) of the device changes to a low resistance state (LRS) at around 3.3 V. This process is called Set. The LRS changes to the HRS by a voltage sweep in the same direction. A sudden current drop is observed at around 0.5 V. This process is called Reset. The ReRAM device starts to show a nonvolatile resistance change when the Reset and Set processes are alternated. Note that, in general, the as-grown sample shows the HRS state. The first Set requires the higher voltage than that of the Set process. This process is called Forming and is considered to be the soft breakdown of the MOM structure. Since the Forming voltage decreases with a decrease in the thickness of the oxide layer, the Forming process will not be the additional operation in the practical memory application. In the bipolar operation, the Set and Reset processes are achieved by applying the voltage in opposite directions, as shown in Fig. 2 (b).

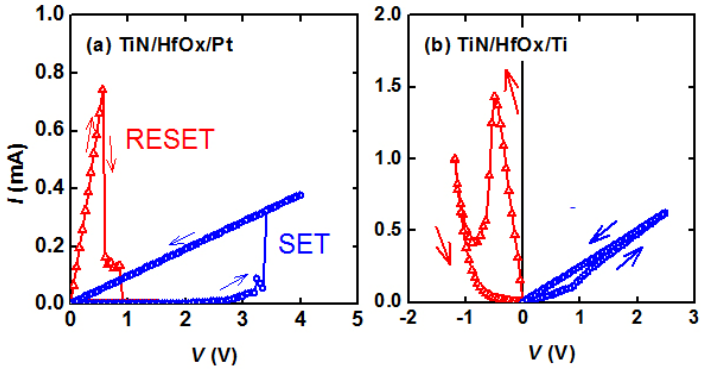

Fig. 2. I-V characteristics of two operation modes of ReRAM. (a) Unipolar and (b) bipolar modes. The arrows show the current sweep direction. Set and Reset processes are shown by blue and red lines, respectively.

2.2 Resistance switching

Resistance switching is an essential physical effect in the ReRAM operation. The resistance switching effect has been studied for more than 40 years. Large negative resistance was reported in the current-voltage (I-V) characteristics of five MOM structures: SiO_x, Al_2O_3, Ta_2O_5, ZrO_2, and TiO_2 [3]. The

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resistance switching effect is classified according to the I-V curve. One is the memory type and the other is threshold type, as shown in Figs. 3 (a) and (b), respectively [4]. In Fig. 3 (a), the I-V curve of HRS (the blue line) intersects with that of LRS (the red line) at zero voltage. The memory-type resistance switching is utilized in ReRAM. The possible mechanism was reported in the study of NiO, where the switching was believed to be due to the formation and rupture of a nickel metallic filament in a NiO thin film sandwiched between two electrodes [5]. This is the first report on the so-called "filament model" (see section 3). The resistance switching in oxide materials was reviewed in 1970 [6].

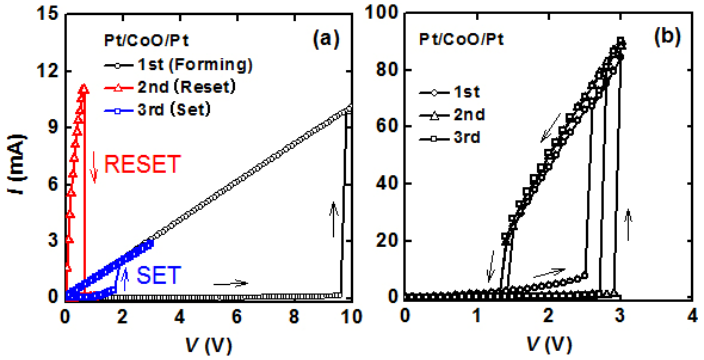

Fig. 3. Resistance switching (a) memory-type and (b) threshold type, observed in the Pt/CoO/Pt MOM structure. Set and Reset processes in the memory-type are shown by blue and red lines, respectively [4].

2.3 Materials issue

In the past, due to analogies from ferroelectric memory, many groups frequently used Pt as the electrode in a ReRAM device. The Pt electrode can be easily fabricated by the sputtering deposition method. On the other hand, it has the following disadvantages: high cost and difficulties in the etching process. To enhance the etching ratio and to avoid residual products, for example, a high substrate temperature is required even in the reactive etching process. More seriously, these issues decrease the process margin, degrading the scalability. However, the present understanding is that a Pt electrode is not necessary, could be even detrimental, for the stable ReRAM operation. Various combinations of metal electrodes and oxides that have shown nonvolatile resistance switching are summarized in Ref. 2. The standard metallic materials in the current semiconductor technology, such as TiN and Ta, are now widely used.

The resistance switching phenomena have been observed in various types of oxide materials, such as oxides with the perovskite crystal structure. In this contribution, however, we will focus on the switching observed in binary metal oxides. Although an excellent resistance switching has been reported

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in these binary metal oxides, efforts to boost the practical development are now focused on the usage of so-called high-k oxides, such as HfO_x. These high-k oxide materials are relatively robust in fabrication processes, while the properties of oxide materials, such as the resistivity, are changed by the oxygen concentration. The precise control of the metal/oxide interface is also an issue for the development. Any unintentional oxygen diffusion from the oxide memory element to the metal electrode and the passivation (insulating) layer should be avoided. Recently, technical improvements to control the oxygen distribution have been reported. For example, an engineered barrier with AlO_x at the metal/oxide interface improved the read disturb immunity [7]. That is, the robustness of the non-volatile operation was improved. In contrast to the diffusion barrier, diffusion control by the oxygen gettering effect of the inserted Ti layer against HfO_x was used to control the forming voltage.

2.4 Epoch-making achievements

The pioneering study, a reversible and non-volatile resistance change, was reported in the beginning of the 21st century. The practical application toward the nonvolatile memory was first reported in 2002 [8, 9]. Zhuang *et al.* fabricated a 64-bit perovskite-oxide-based ReRAM memory array, using a 0.5-μm CMOS process [10]. In 2004, the fabrication of binary transition-metal-oxide based ReRAM was reported by a group from the Samsung Advanced Institute of Technology. They demonstrated the ReRAM operation below 3 V and 2 mA, 10^6 Set/Reset operations, and 10^{12} reading cycles [11]. Sub-mA low-current ReRAM operation was reported in the CuO_x-based MOM structure. The CuO_x layer was fabricated by the thermal oxidation of the 0.18-μm Cu via structure [12]. NiO and CoO were then being intensively studied as oxide materials for ReRAM [13, 14, 15, 16]. TaO_x-based ReRAM with endurance over 10^9 cycles and the retention exceeding 10 years at 85°C was demonstrated in 2008 [17]. The 8 kbit 1 Transistor/1 Resistor (1T1R) memory array with a good operating window was fabricated using the standard 0.18 μm CMOS process. The good scaling behavior of ReRAM was demonstrated in an HfO_x-based memory with a memory element size of 30 nm in 2009 [18]. The devices in a 1-kbit array exhibited a high device yield ($\sim$ 100%) and robust cycling endurance ($> 10^6$) with the pulse width of 40 ns. In 2010, switching speed down to 300 ps was achieved in HfO_x-based ReRAM together with the robust endurance (10^{10} cycles) [19].

In terms of the scaling, the 9 nm Half-Pitch Functional Resistive Memory Cell with $< 1\,\mu$A Programming Current was reported in WO_x resistive memory cell [20]. Sudden decrease of the operation current was observed in TiO_x/AlO_x memory structure by using sub 10 nm scale electrodes [21]. Very recently, HfO_x-based ReRAM cell with the area of less than $10 \times 10\,nm^2$ has been demonstrated, with switching times on the order of ns and below, operating voltages well below 3 V, $> 5 \times 10^7$ endurance and no degradation of the on/off ratio after 30 hrs/200 degree C and extrapolated retention of $>$ 100 degree C/10 yrs [22]. 64 Mbits ReRAM prototype which was made using a 50-nm process technology and the memory array operation has been

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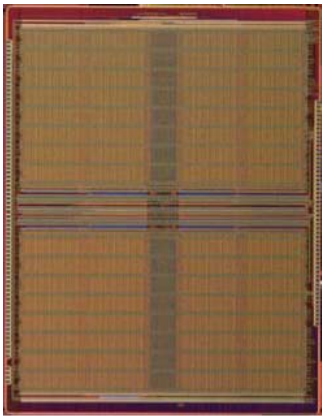

Fig. 4. 64 Mbits ReRAM array [23].

reported in Jan. 2012 [23].

3 Operation mechanism and technical assessment

A number of studies have been conducted to elucidate the origin of the resistance switching of ReRAM. The proposed mechanisms can be classified into two models: the filament model and the interface model. As mentioned in section 2, the filament model was first proposed in 1964 [5]. More physical observations by conductive atomic force microscopy (cAFM) evidenced the formation and rupture of conducting channels was provided with a high spatial resolution. By applying the external voltage to the cAFM tip as the top electrode, the nonvolatile resistance switching operations of Forming, Reset, and Set were triggered, the conducting spots appeared in the Forming and Set processes [24]. It is considered that the "electric faucet" turns ON and OFF at the high-resistance interface to regulate the current flow in the filament conduction path between two electrodes (Fig. 5). In the same report, a high-resolution transmission electron microscopy (HR-TEM) image of the NiO layer showed the fabrication of nano-scale nickel filament across two electrodes through the grain boundaries of the insulating NiO material.

On the other hand, regarding to the interface model, the contribution of the electrochemical reaction at the metal/oxide interface was implied by the fact that the resistance switching took place on the anodic side of the conductive filaments in NiO [25]. The redox (reduction and oxidation) reaction was firstly evidenced optically in the Fe-O based ReRAM [26]. Raman microspectroscopy on the lateral device and 4-electrode transport measurements revealed that the resistance switching was explained as a redox reaction between Fe_3O_4 and Fe_2O_3 at the interface near the anode. The redox reaction at the electrode interface in a $Pt/TaO_x/Pt$ memory cell was also confirmed by hard X-ray photoemission spectroscopy [17]. The spectra showed the correspondence of the reduced TaO_x component to the change in the resistance state. For example, in the Reset operation, by applying a positive voltage to the anode electrode, O^{2-} ions migrated and the ions led to the formation of $Ta_2O_{5-\delta}$ from $TaO_{2-\beta}$. Increasing the $Ta_2O_{5-\delta}$ component enlarged the

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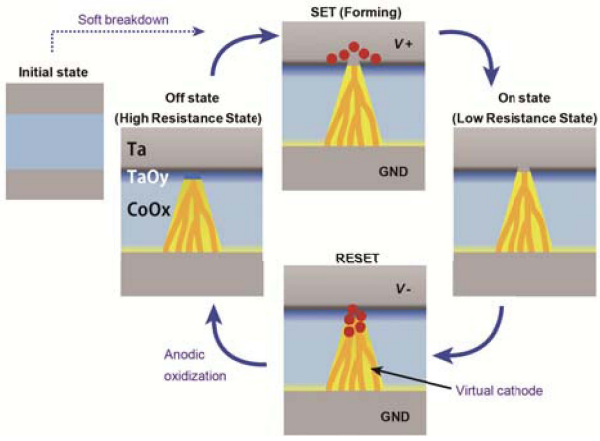

Fig. 5. Filamentary model for the ReRAM operation. By way of illustration, the combination of the $CoO_x/TaO_y/Ta$ structure is schematically shown. Note that the size of the memory element shown in this schematic image is the order of 100 nm.

band gap and increased the Schottky barrier height at the interface.

The above-mentioned filament and interface models are thought to be contradictory. However, by taking into account the size of the memory cell, the discrepancy will disappear. Fig. 6 shows the unified model for ReRAM operation [2]. In a submicrometer memory cell, the Forming process will bring about a filamentary low-resistance conductive path between the top electrode (TE) and bottom electrode (BE). Here, we assume that the external voltage is driven at Ta TE and the Forming process is carried out by applying the positive voltage. In this case, during the Forming process, the conductive state expands from the cathodic BE interface and finally reaches the anodic TE interface, followed by an increase in the interfacial TaO_y layer thickness. In the Reset operation, when the negative voltage pulse is applied at TE, the repulsive force makes O^{2-} ions migrate from TaO_y to CoO_x. In this case, the TaO_y layer acts as the oxygen supplier, and CoO_x is oxidized. Consequently, the CoO_x layer is transformed from the conductive state to the insulating state of CoO. On the other hand, in the Set operation, when the positive voltage pulse is applied at TE, O^{2-} ions again migrate from the bulk CoO_x to TaO_y. The TaO_y layer during this Set operation is assumed to be an oxygen reservoir, yielding the reducing transformation from the insulating CoO_x to the conductive state.

As has been described in section 2, the practical size of the memory cell is going to reach below 4X nm, and will move into beyond-2X-nm generation. Since the size of the faucet of the filamentary conductance path is in the range of $10 \sim 30$ nm for realistic operation currents, the size will become comparable to the memory cell size, at the latest in the beyond-2X-nm generation. When a ReRAM cell is prepared with a cell size smaller than 30 nm, the ReRAM operation model can be redrawn as shown in Fig. 6. The operation is exactly explained by the interface model. Namely, in the generation of a 2X-nm

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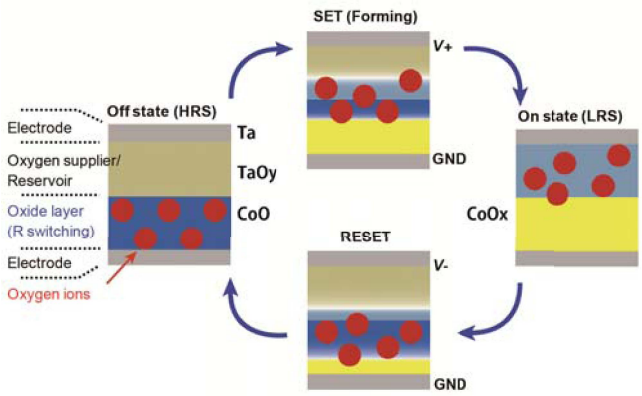

Fig. 6. Unified Redox model for the ReRAM operation. By way of illustration, the combination of the $CoO_x/TaO_y/Ta$ structure is schematically shown. Note that the size of the memory element is the order of 10 nm, smaller than the size of the faucet of the filamentary conductance path shown in Fig. 5.

node, the filament and interface models will be unified. Our unified Redox model has been accepted and utilized in many studies [27, 28].

In the bipolar switching, the assistance of the Joule heating accelerates the switching cooperatively to the electric field. In contrast, in the unipolar switching, the Joule heating contributes the resistance switching competitively to the electric field. Because of the temperature increase due to the Joule heating, where the diffusion constant is exponentially increased, O^{2-} ions migrate in order to suppress the concentration gradient, causing the Reset process. Accordingly, in the Joule-heating assisted switching process, the oxygen-affinity of the electrode material affects strongly the operation, and the higher Reset current is considered to be required in the unipolar operation.

Low-power operation is one of the most important issues of the technical assessment. The load resistor and embedded transistor used to regulate excessive current lowered the operation current [4]. The current regulation corresponds to controlling the redox reaction during the Reset operation and the number and/or total area of the conductive regions in the oxide layer. This is the great advantage of the ReRAM technology. We can control the size of the faucet, the size of the conductance path, and can expect a lower power operation with a smaller ReRAM device. The merit of scaling is evidenced. In addition, in view of the randomness inherent in the filamentary conduction path formation, the miniaturizing of a ReRAM cell is expected to improve the operation current stability by excluding candidate sites for the extra-path formation with the cyclic operation.

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4 Difficult challenges and the prospect

4.1 Improvement of memory performance

ReRAM is the most promising candidate for the next-generation of non-volatile memory because of its simple structure, high switching speed (~ 1 ns) and high scalability (< 10 nm). This high scalability is ensured by the fact that the present CMOS technologies are applicable to the technologies for ReRAM. As described in section 2, the endurance of the ReRAM device has reached 10^{10} [19]. These characteristics are very good enough to utilize ReRAM as a storage-class memory [1], which will be an essential memory to bridge the latency gap between DRAM and Flash memory. This number of the endurance, however, is not sufficiently large to allow the ReRAM device to replace DRAM itself. The endurance improvement is certainly one of the biggest challenges as a long-term objective. The key requirement is a method to control the oxygen movement at the interface between the electrode and the oxide layer. Inserting a second oxide layer at the interface will solve the problem. Since the other target of ReRAM applications is a high-density memory to replace NAND Flash memory, the development of the 1 Diode/1 Resistor (1D1R) operation, the cross-point operation and the vertical 3D-stack technology must be accelerated [29].

4.2 Stability and reliability

The critical requirements for the next few years are related to integration and reliability issues. From the viewpoint of integration technologies for the better stability in the ReRAM operation, we have to address the urgent priorities of controlling the oxidization of the metal element and the uniformity of the metal/oxide interface. Actually, with flattening of the electrode, both the uniformity of resistance states and switching endurance of the memory device were significantly improved [19]. To develop the memory-data management algorithms, such as the verify-programming method, will certainly promote the practical development of ReRAM with higher stability and reliability [30].

4.3 Other potential applications

The role of ReRAM will be much more important in an analog data processing and emerging brain computing. The non-volatile and analog resistance change was observed in some MOM structures exactly like the stacking structure of ReRAM. For instance, the Pt/TiO_x/Pt memristor [31] and the switchable rectifier [32, 33] were proposed, where charged oxygen vacancies were regarded as a mobile dopant in the semiconducting oxide and the electrical control of the vacancies was utilized to control the gradual and non-volatile resistance change of the device, as shown in Fig. 7. The state variable can be regarded as the distribution of the oxygen vacancies in this "beyond-CMOS" device.

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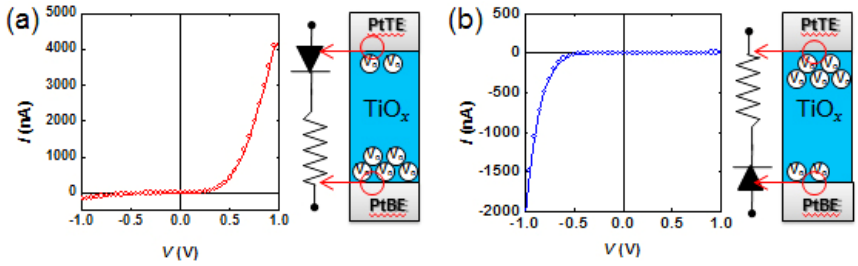

Fig. 7. *I-V* curves of $Pt/TiO_x/Pt$ MOM structure. Schematic illustrations of the oxygen vacancies show that the interface with the higher concentration becomes Ohmic, while that with the lower concentration shows the rectification behavior. The distribution of the oxygen vacancies was changed by the voltage pulse [32].

5 Conclusion

The scaling merit of Flash memory will enable it to be the booster in the nonvolatile memory technology because of its potential high-density data storage applications, at least until the 2X-nm generation [1]. However, beyond the 2X-nm generation, the scaling merit will not work, not for technical reasons, which can be solved by engineering developments, but because of the physical and fundamental difficulty. Due to the degradation such as leakage current the endurance of Flash memories is decreasing. Fast nanosecond-level operations will not be achieved in the Flash memory technology because of the intrinsic limit in terms of the write operation. Nevertheless, high-density nonvolatile memory with high-speed operation is absolutely imperative for the sustainable development of our society supported by information and communication technologies (ICT). Here, it should be noted that high-speed and low-power operations are competing two sides of the same coin of current semiconductor-based devices. This paper has shown that ReRAM, which is based on binary metal oxides, will be the best candidate to meet the conflicting requirements. The electrochemical redox reaction fulfills the crucial role of a key to solving the problem.

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