

A single-ended CMOS chopper amplifier for 1/f noise reduction of n-channel MOS transistors

Kamel Mars^{1a)} and Shoji Kawahito^{2b)}

¹ Graduate School of science and Technology, Shizuoka University

3–5–1 Johoku, Nakaku, Hamamatsu 432–8011, Japan

² Research Institute of Electronics, Shizuoka University

3–5–1 Johoku, Nakaku, Hamamatsu 432–8011, Japan

a) kamel@idl.rie.shizuoka.ac.jp

b) kawahito@idl.rie.shizuoka.ac.jp

Abstract: This paper describes a single-ended CMOS chopper amplifier for 1/f noise reduction of n-channel MOS transistors and its application to a low-noise high-gain switched-capacitor (SC) amplifier for sensor interface circuits. Since the chopping is used inside of the operational transconductance amplifier (OTA), this amplifier can be used for high output impedance sensors. To investigate the effect of the proposed chopping technique, a test chip was fabricated using 0.25 μm mixed-signal CMOS process. The total input-referred noise is greatly reduced by using a high chopping frequency of 256 kHz to 20 μV_{rms} from 295 μV_{rms} without chopping.

Keywords: chopping, low noise, 1/f noise reduction

Classification: Integrated circuits

References

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2010.

1 Introduction

A chopper-stabilization technique is useful for $1/f$ noise reduction of MOS transistors in high-precision low-noise CMOS amplifiers to detect small signal of sensor outputs. The chopper-stabilized amplifiers are usually implemented with cross-coupled switches in fully differential circuits, and to use the chopping technique, the output impedance of the sensors must be sufficiently small to drive the cross-coupled switch and the load capacitance [1, 2, 3]. If the sensor output has a single-end configuration, the fully differential circuit which often used for choppers stabilized amplifiers is not always suitable for a cost-effective front end amplifier of sensor signal outputs.

This letter proposes a single-ended switched-capacitor amplifier internally using a chopper-stabilization technique for the $1/f$ noise reduction and which can be used for high output impedance sensors. The proposed technique is based on a fact that an n-channel MOS (nMOS) transistor often has much larger $1/f$ noise than that of a p-channel MOS (pMOS) transistor. The chopping technique is used for reducing the $1/f$ noise of nMOS transistors only for the totally low-noise amplifiers.

2 Circuits and operation

The CMOS single-ended telescopic cascode amplifier with the chopping technique is shown in Fig. 1(a). By applying a clock ϕ_c to switches in the amplifier, the $1/f$ noise of nMOS transistors, MN1 and MN2 is modulated by the chopping clock. This circuit configuration allows the realization of a single-ended chopper amplifier for the $1/f$ noise reduction of nMOS transistors.

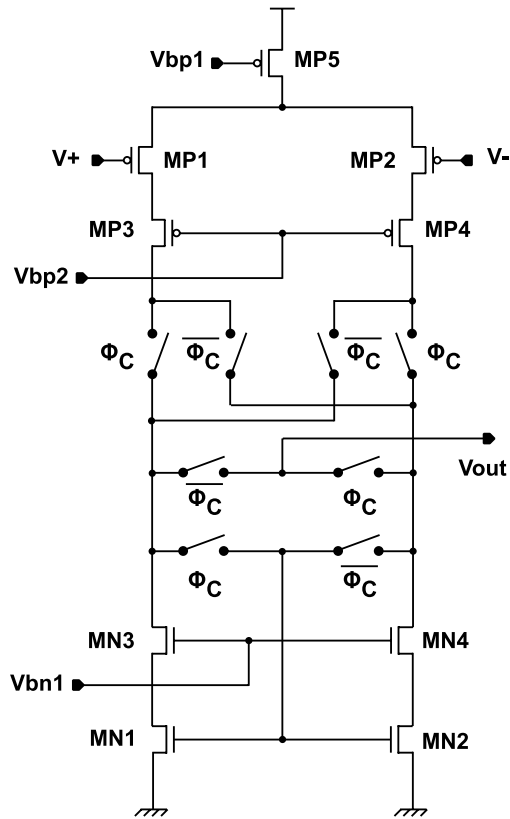
Small-signal equivalent circuits for the noise models in $\phi_c = "1"$ and $\phi_c = "0"$ phases are shown in Fig. 1(b) and 1(c), respectively. The noises in cascode transistors MP3, MP4, MN3 and MN4 have less influence to the output current than those of the others, and are ignored in Fig. 1(b) and 1(c).

The output noise currents $i_{n,out}(1)$ and $i_{n,out}(0)$ for $\phi_c = "1"$ and $\phi_c = "0"$ are given by

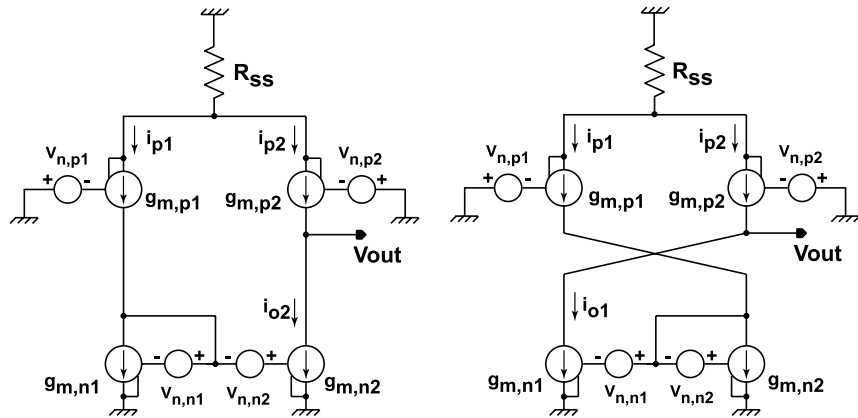
$$i_{n,out}(1) = g_{m,p2}v_{n,p2}(1) + g_{m,p1}\frac{g_{m,n2}}{g_{m,n1}}v_{n,p1}(1) - g_{m,n2}(v_{n,n1}(1) + v_{n,n2}(1)) \quad (1)$$

$$i_{n,out}(0) = g_{m,p2}v_{n,p2}(0) + g_{m,p1}\frac{g_{m,n1}}{g_{m,n2}}v_{n,p1}(0) + g_{m,n1}(v_{n,n1}(0) + v_{n,n2}(0)) \quad (2)$$

where $v_{n,p1}(x)$, $v_{n,p2}(x)$, $v_{n,n1}(x)$ and $v_{n,n2}(x)$ are noises of transistors MP1, MP2, MN1 and MN2 in phases of $\phi_c = "1"$ and $\phi_c = "0"$ and $x = 1$ and $x = 0$ corresponds to $\phi_c = "1"$ and $\phi_c = "0"$, respectively. Therefore, the noises of



(a) Single-ended chopper amplifier



(b) Noise model for $\phi_c = "1"$

(c) Noise model for $\phi_c = "0"$

Fig. 1. Low noise readout circuit with chopping technique

MN1 and MN2 are modulated by the chopping clock and low frequency noise components, or $1/f$ noises are reduced if a low-pass filter to attenuate the modulated noise is connected to the output of the chopper amplifier. The noises in pMOS transistors are not modulated by the chopping and there is noise reduction effect in pMOS transistors.

3 Application to two-stage switched-capacitor amplifier

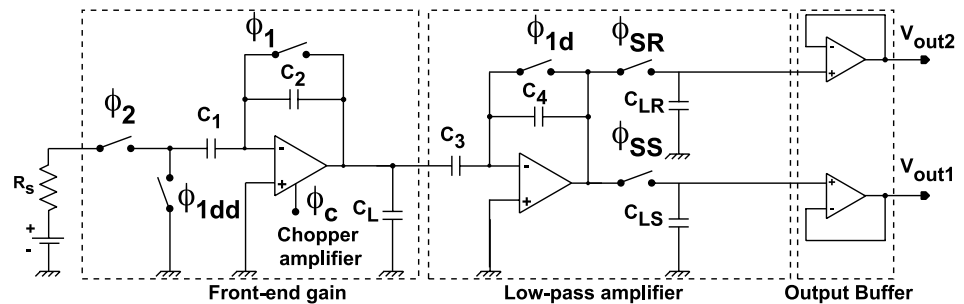
A two-stage switched-capacitor (SC) amplifier using the chopper amplifier in the front-end gain stage is designed and implemented for testing the effectiveness of the chopper amplifier. Fig. 2 (a) and 2 (b) show two-stage SC amplifier and the timing diagram of the operation clock signals. The gains of the front-end stage and the second low-pass filtering amplifier stage are given by C_1/C_2 (G_1) and C_3/C_4 (G_2), respectively, and the total gain is given by $G_1 \cdot G_2$.

The output signal of the second stage is sampled and held by a capacitor C_{LS} and a switch controlled by ϕ_{SS} . Another sample-and-hold circuit using a capacitor C_{LR} and a switch controlled by ϕ_{SR} for storing the reset noise and offset due to charge injection of switches by ϕ_1 and ϕ_{1d} and OTA's offset voltage are used. The final output is given by $V_{out2} - V_{out1}$ for canceling the reset noise and offset [4, 5].

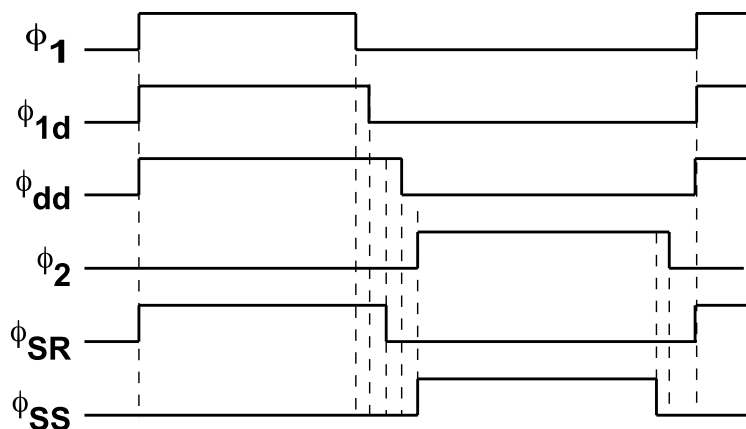
The cutoff frequency f_{co} of the second stage is given by

$$f_{co} = \frac{1}{2\pi} \frac{g_{m2}}{C_L (1 + C_3/C_4)} \quad (3)$$

where C_L is the capacitance of C_{LR} and C_{LS} , and g_{m2} is the transconductance of the internal operational transconductance amplifier (OTA) of the second



(a) Low noise readout circuit



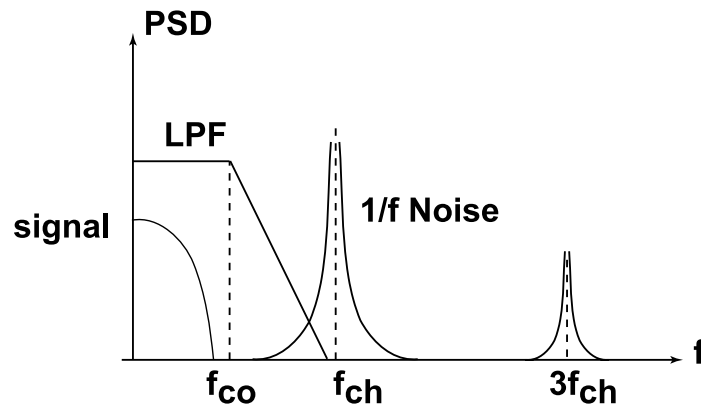
(b) Timing diagram

Fig. 2. Low noise readout circuit with chopping technique

stage. The second stage is used for gain enhancement and 1st-order low-pass filter for modulated $1/f$ noise reduction.

4 Measurement results

For measuring the noise characteristics of the SC amplifier of Fig. 2 and the effect of the chopper amplifier, a test chip was fabricated using $0.25\text{ }\mu\text{m}$ mixed-signal CMOS process. The designed gain given by $(C_1/C_2) \times (C_3/C_4)$ is 1024 using $C_1 = 4\text{ pF}$, $C_2 = 125\text{ fF}$, $C_3 = 4\text{ pF}$ and $C_4 = 125\text{ fF}$. Because of the stray capacitance and the finite OTA gain, the measured gain was 600 at the chopping clock frequency f_{ch} of 256 kHz. To investigate the effect of the proposed chopping technique, the input-referred noises for three cases ($f_{ch} = 0\text{ Hz}$, $f_{ch} = 16\text{ kHz}$ and $f_{ch} = 256\text{ kHz}$) were measured. The operation using $f_{ch} = 0\text{ Hz}$ means that the chopping technique is not used. The measured input-referred noises are shown in Fig. 3(b). Fig. 3(a) shows a diagram of power spectral density to explain the effect of chopping with respect to the choice of f_{ch} . The cutoff frequency of the second stage is 19 kHz using $g_{m2} = 40\text{ }\mu\text{ mho}$, $C_L = 10\text{ pF}$ and $C_3/C_4 = 32$. When f_{ch} is set to be very close to the cutoff f_{co} , the total input-referred noise is slightly reduced compared to the case without chopping. When a high chopping frequency of 256 kHz compared to f_{co} is used, the total input-referred noise is greatly reduced because all the $1/f$ noise components are suppressed by the low-pass filter. The use of $f_{ch} = 256\text{ kHz}$ and $f_{co} = 19\text{ kHz}$ reduces the total input



(a) Chopping Principle

$f_{ch}[\text{kHz}]$	Noise[μV_{rms}]
0	295
16	175
256	20.0

(b) Measurement results

Fig. 3. Chopping principle and measurement results

referred noise to $20\mu\text{V}_{\text{rms}}$.

5 Conclusion

In this paper a single-ended CMOS chopper amplifier for $1/f$ noise reduction of n-channel MOS transistors and an application to a high-gain SC amplifier have been presented. Since the chopping switches are used for the inside of the internal amplifier only, this technique can be used for readout circuits of high-output impedance sensors. The measured noise of a test chip shows the effectiveness of the chopping technique.

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