

# A fully integrated pulse width modulator for Class-S power amplifiers

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**Abstract:** A fully integrated pulsewidth modulator for Class-S power amplifiers is presented. It consists of a triangular signal generator, a comparator and output buffer. The HBT BiCMOS design of PWM circuit is applied to the LTE frequency range, which converts digitally modulated 955 MHz RF carrier with 2.87 GHz sampling clock. This PWM shows an EVM 6.6%, a differential output voltage swing 1.35 V<sub>p-p</sub> with 62.7 mA dissipating at 3.3 V power supply.

**Keywords:** pulse width modulator, Class-S, power amplifier, PAPR

**Classification:** Integrated circuits

## References

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## 1 Introduction

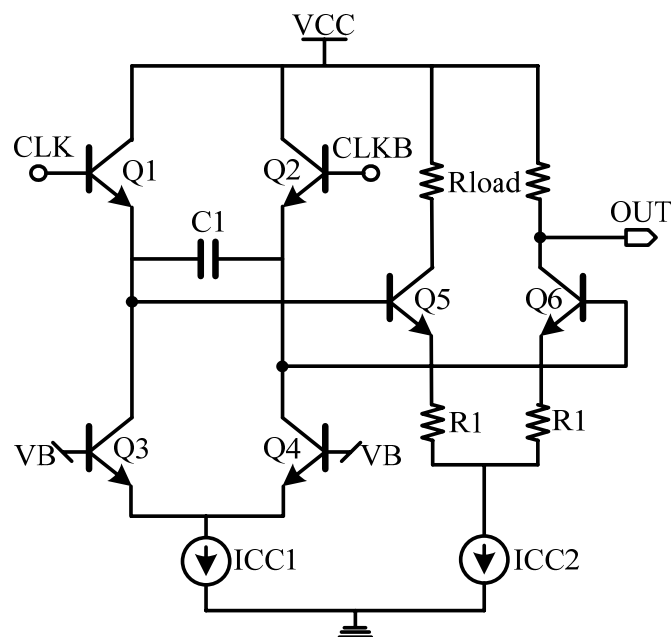
Recently, energy consumption of mobile telecommunication infrastructure has become a major concern, when introducing bandwidth-optimized modulation schemes with high peak-to-average power ratios (PAPRs). Therefore, the concepts for highly efficient power amplifiers (PAs) have

become the subject of intensive research [1]. One of candidates for implementing high efficiency transmitter is Class-S amplifier [2]. Pulse-width modulator (PWM) and Delta-sigma modulator (DSM) are crucial for converting non-constant envelope signal to bi-level digital signal in Class-S concept [3, 4, 5].

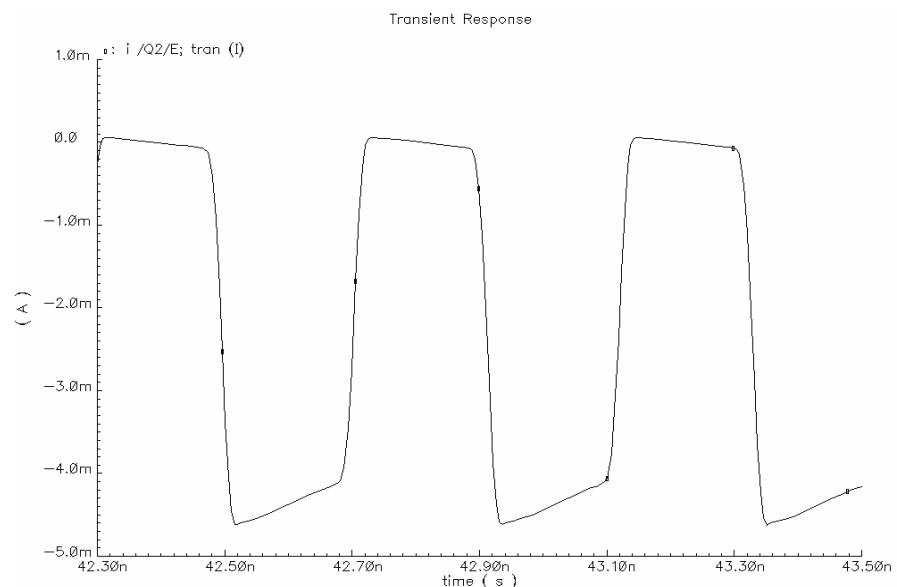
## 2 Circuit design

The PWM is composed of two main functional blocks; a triangle signal generator and a comparator. The schematic of signal generator without biasing circuit is shown in Fig. 1.

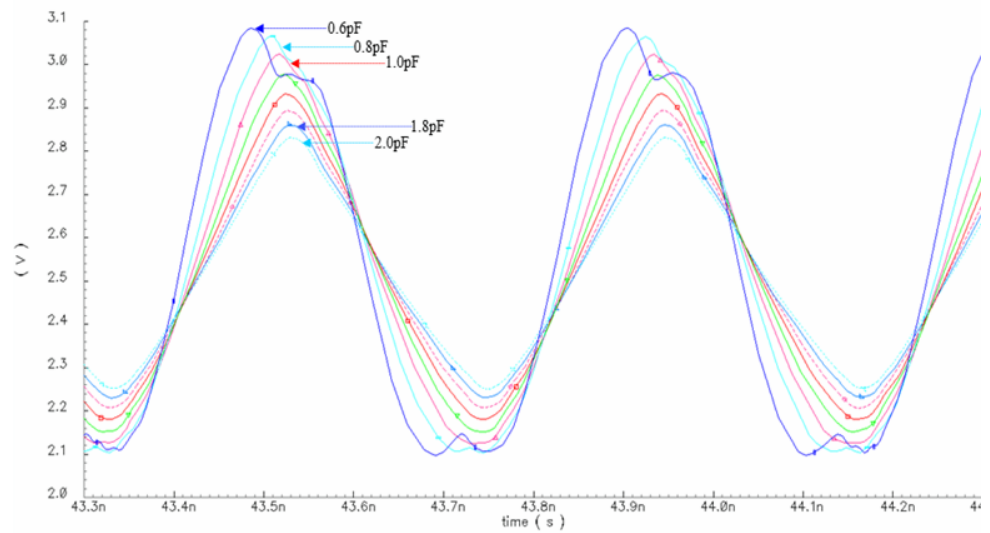
Differential sinewave clock signals are injected through CLK, CLKB nodes of 300 mV peak at each node. The capacitor C1 converts the rectangular-shaped current as shown in Fig. 2 to triangle-shaping voltage



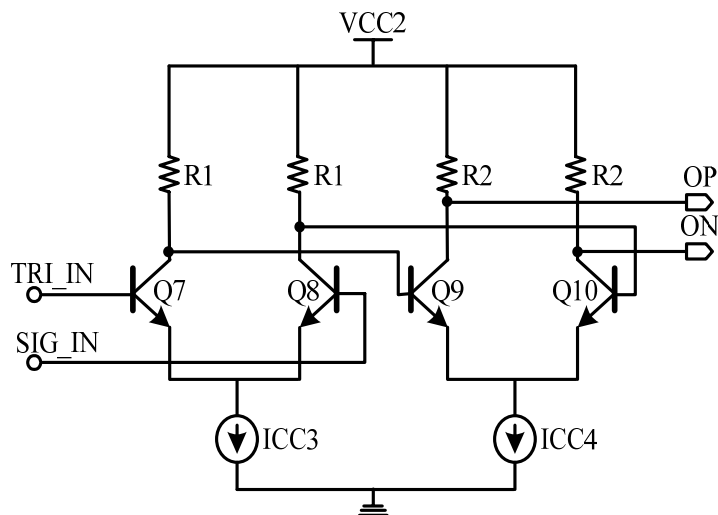
**Fig. 1.** Triangle signal generator



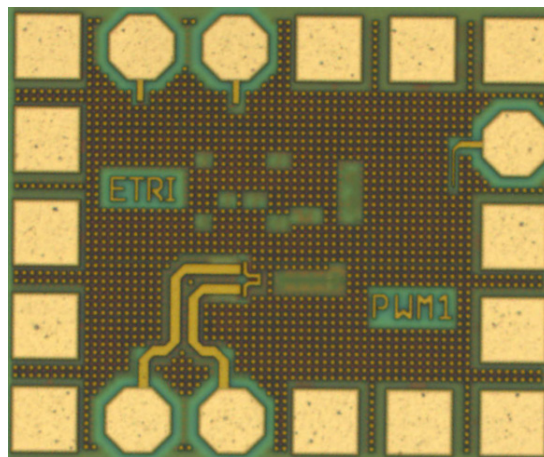
**Fig. 2.** Current waveform in Q1



**Fig. 3.** Output waveform of triangle signal generator



**Fig. 4.** Comparator circuit



**Fig. 5.** Micrograph of full chip PWM

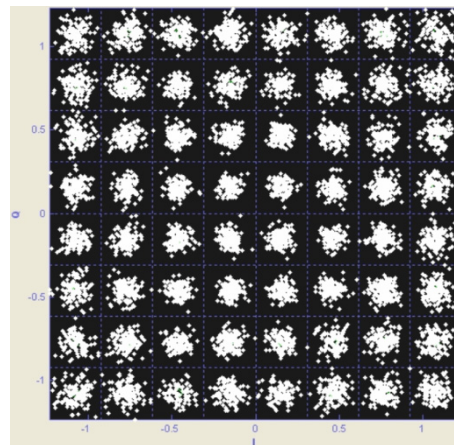
signal as (1)

$$v(t) = v(t_0) + \frac{1}{C1} \int_{t_0}^t i(t) dt \quad (1)$$

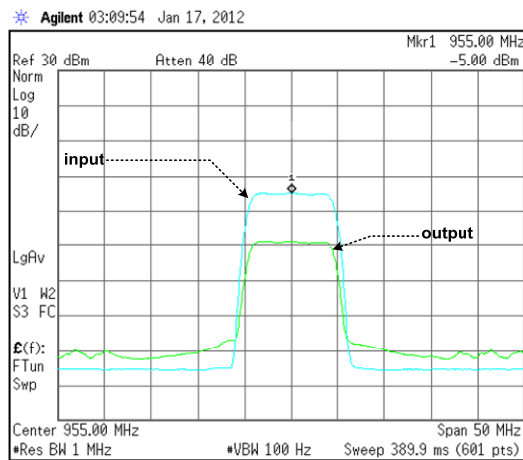
The direction of the charging current is alternately switched, so that the voltage across the capacitor rises and falls nearly linear with time, then 2nd



(a)



(b)



(c)

**Fig. 6.** Measured characteristics of PWM; (a) Time-domain characteristic, (b) Constellation of PWM, (c) Spectrum

stage differential amplifier generates the pure triangular signal. In contrast to the sawtooth reference signal, the triangular signal does not have steep falling edges, which save a considerable amount of bandwidth.

It is important to choose the capacitor C1 value because of making appropriate triangular shaped signal. Therefore, the characteristics of triangle signal generator are evaluated varying the value of C1. Fig. 3 shows the output simulation result of triangular circuit. The most suitable value of capacitor C1 is around 1 pF.

Comparator block compares the reference signal (triangular signal) with non-constant input signal. The circuit schematic of comparator is shown in Fig. 4, which makes the digitally pulse output at OP, ON nodes. The non-constant envelope RF signal is entered at node SIG\_IN and triangular reference signal is injected at node TRI\_IN. If the reference signal is larger than the RF signal then the output is “High” state and vice versa. Comparator is composed of 2-stage differential amplifier topology. It draws 16.5 mA current at 3.3 V supply.

### 3 Measurement results

The proposed PWM shown in Fig. 5 is fully integrated using 0.25  $\mu\text{m}$  SiGe BiCMOS technology, the total area is  $0.61 \times 0.5 \text{ mm}^2$ . As shown in Fig. 6a, the measured pulse shaping characteristic shows a 674 mV peak-to-peak swing in single-ended. The common-emitter differential amplifiers are used to enlarge the output voltage swing. In order to verify the adaptability of PWM as a Class-S Transmitter modulator a real down-link transmitting LTE signal with 10.5 dB PAPR is applied and constellation is measured. The signal is generated using matlab code and downloaded in signal generator then measured by vector signal analyzer. The measured result is shown in Fig 6b and error vector magnitude (EVM) is 6.6%. This EVM result satisfies the 8% of 64QAM LTE downlink specifications [6]. Fig. 6c shows the measured spectrum with 10 MHz long-term-evolution (LTE) signal. The adjacent channel power ratio (ACPR) is around 31 dBc. The measured performances of the PWM are summarized in Table I.

**Table I.** Summary of measured PWM performances

Parameter	Measurement results
Technology	0.25 $\mu\text{m}$ SiGe BiCMOS
Carrier frequency	945-965 MHz
Clock frequency	2865 MHz
Supply voltage	3.3 V
Power consumption includes buffer	207 mW
Output voltage swing (differential)	1.35 Vp-p
EVM (64QAM LTE) @10.5dB PAPR	5.9 % @ 945 MHz
	6.6 % @ 955 MHz
	6.8 % @ 965 MHz

### 4 Conclusion

The design and measurement results of the PWM for Class-S power amplifiers, which is implemented in 0.25  $\mu\text{m}$  BiCMOS technology, are

presented. The lower clock rate than the 4 times of the carrier frequency can adapt the mobile downlink standard. Furthermore it makes alleviate the wideband burden of power amplifier.

### **Acknowledgments**

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