

A compact low-power nonvolatile flip-flop using domain-wall-motion-device-based single-ended structure

Daisuke Suzuki^{1a)}, Noboru Sakimura², Masanori Natsui^{1,3},
Akira Mochizuki¹, Tadahiko Sugibayashi², Tetsuo Endoh^{1,4,5},
Hideo Ohno^{1,3,5,6}, and Takahiro Hanyu^{1,3,5}

¹ Center for Spintronics Integrated Systems, Tohoku University,
2–1–1 Katahira, Aoba-ku, Sendai 980–8577, Japan

² Green Platform Research Laboratories, NEC Corporation,
34 Miyukigaoka, Tsukuba 305–8501, Japan

³ Research Institute of Electrical Communication, Tohoku University,
2–1–1 Katahira, Aoba-ku, Sendai 980–8577, Japan

⁴ Graduate School of Engineering, Tohoku University,
6–6 Aramaki Aza Aoba-ku, Sendai 980–8579, Japan

⁵ Center for Innovative Integrated Electronic Systems, Tohoku University,
468–1 Aramaki Aza Aoba-ku, Sendai 980–0845, Japan

⁶ WPI-Advanced Institute for Materials Research, Tohoku University,
2–1–1 Katahira, Aoba-ku, Sendai 980–8577, Japan

a) show-you@ngc.riec.tohoku.ac.jp

Abstract: A nonvolatile flip-flop (NV-FF) is proposed for a zero-standby-power LSI using a domain-wall motion (DWM) device. Since the write current path is separated from the read current path in the DWM device, two nonvolatile memory function blocks, a write driver for storing temporal data into the DWM device, and a sense amplifier for recalling the stored data from the DWM device can be optimized independently. Moreover, the use of a nonvolatile storage cell with a DWM-device-based single-ended structure makes it possible to implement both of these functions as two CMOS inverters, which makes it possible to merge them into a CMOS delay flip-flop (D-FF) core. Since the nonvolatile storage cell is electrically separated from the D-FF core during the normal operation, there is no performance degradation. In fact, the area and the power-delay product of the proposed NV-FF are minimized compared to those of the previous works.

Keywords: nonvolatile logic, magnetic tunnel junction, spintronics

Classification: Integrated circuits

References

- [1] N. Sakimura, T. Sugibayashi, R. Nebashi and N. Kasai: IEEE J. Solid-State Circuits **44** (2009) 2244. DOI:10.1109/JSSC.2009.2023192
- [2] M. Natsui, D. Suzuki, N. Sakimura, R. Nebashi, Y. Tsuji, A. Morioka, T. Sugibayashi, S. Miura, H. Honjo, K. Kinoshita, S. Ikeda, T. Endoh, H. Ohno and T. Hanyu: IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap. (2013) 194. DOI:10.1109/ISSCC.2013.6487696
- [3] M. Qazi, A. Amerasekera and A. P. Chandrakasan: IEEE J. Solid-State Circuits **49** (2014) 202. DOI:10.1109/JSSC.2013.2282112
- [4] S. Yamamoto, Y. Shuto and S. Sugahara: Electron. Lett. **47** (2011) 1027. DOI:10.1049/el.2011.1807
- [5] K. Ryu, J. Kim, J. Jung, J.-P. Kim, S.-H. Kang and S.-O. Jung: IEEE Trans. VLSI Syst. **20** (2012) 2044. DOI:10.1109/TVLSI.2011.2172644
- [6] K. Huang and Y. Lian: IEEE Trans. Nanotechnol. **12** (2013) 1094. DOI:10.1109/TNANO.2013.2280338
- [7] S. Ikeda, K. Miura, H. Yamamoto, K. Mizunuma, H. D. Gan, M. Endo, S. Kanai, J. Hayakawa, F. Matsukura and H. Ohno: Nat. Mater. **9** (2010) 721. DOI:10.1038/nmat2804
- [8] S. Fukami, N. Ishiwata, N. Kasai, M. Yamanouchi, H. Sato, S. Ikeda and H. Ohno: IEEE Trans. Magn. **48** (2012) 2152. DOI:10.1109/TMAG.2012.2187792
- [9] S. Fukami, M. Yamanouchi, K.-J. Kim, T. Suzuki, N. Sakimura, D. Chiba, S. Ikeda, T. Sugibayashi, N. Kasai, T. Ono and H. Ohno: IEDM Tech. Dig. (2013) 72. DOI:10.1109/IEDM.2013.6724553
- [10] D. Suzuki, Y. Lin, M. Natsui and T. Hanyu: Jpn. J. Appl. Phys. **52** (2013) 04CM04. DOI:10.7567/JJAP.52.04CM04
- [11] N. Sakimura, R. Nebashi, H. Honjo, S. Saito, Y. Kato and T. Sugibayashi: Proc. Asian Solid-State Circuits Conf. (2008) 261. DOI:10.1109/ASSCC.2008.4708778
- [12] N. Sakimura, R. Nebashi, Y. Tsuji, H. Honjo, H. Koike, T. Ohsawa, S. Fukami, T. Hanyu, H. Ohno and T. Endoh: Proc. IEEE Int. Symp. Circuits and Systems (2012) 1971. DOI:10.1109/ISCAS.2012.6271663
- [13] http://www.csis.tohoku.ac.jp/files/introduction_ns-spice_mtj.pdf
- [14] H. Sato, M. Yamanouchi, S. Ikeda, S. Fukami, F. Matsukura and H. Ohno: IEEE Trans. Magn. **49** (2013) 4437. DOI:10.1109/TMAG.2013.2251326
- [15] R. Dorrance, F. Ren, Y. Toriyama, A. A. Hafez, C.-K. K. Yang and D. Marković: IEEE Trans. Electron. Dev. **59** 878 (2012). DOI:10.1109/TED.2011.2182053

1 Introduction

The combination of nonvolatile logic circuits together with a power-gating technique where power supply of all the idle function blocks are temporally turned off, is one promising solution for the standby power problem in nano-scale CMOS technologies [1, 2, 3]. A nonvolatile flip-flop (NV-FF) [1, 3, 4, 5, 6] is an essential component for a nonvolatile logic LSI since temporal data of each function block must be clock-synchronized and retained during power-off. Because temporal data in an NV-FF must be stored in a nonvolatile device every time before power-off, it is very important that the nonvolatile device has unlimited endurance as well as fast switching capability in nanoseconds. It

is also important that the area penalty due to the nonvolatile device is minimized. A spin-transfer torque magnetic tunnel junction (STT-MTJ) device is one viable candidate owing to its 3-dimensional stacking capability, virtually unlimited endurance, and fast switching capability [7]. To design an STT-MTJ-based NV-FF, on the other hand, it is very important to consider how to embed two nonvolatile memory function blocks; a write driver for storing temporal data into the STT-MTJ device before power-off, and a sense amplifier for recalling the stored data from the STT-MTJ device after power-on, since they may deteriorate circuit performances such as operating frequency and active power dissipation. Especially, since the read current path and the write current path are common in the STT-MTJ device, STT-MTJ-based NV-FFs must be designed carefully to avoid read disturbance wherein data is accidentally written into an STT-MTJ device during recalling the stored data.

In this paper, an NV-FF is proposed using a domain-wall motion (DWM) device [8, 9] together with single-ended voltage sensing [10]. Since the read current path is separated from the write current path in the DWM device, both the write driver and the sense amplifier can be optimized independently with no read disturbance. To be specific, the use of the DWM device makes it possible to drive sufficient write current with just two CMOS inverters since the resistance value of the write current path is quite small (less than $150\ \Omega$ [8]). Moreover, the MTJ resistance for reading can be determined independently of the write current. Therefore, sufficient read voltage can be achieved by the use of single-ended voltage sensing, which makes it possible to implement the sense amplifier by just only two CMOS inverters. As a result, the write driver and the sense amplifier are merged into the master latch and the slave latch in a CMOS delay flip-flop (D-FF) with no performance degradation. These benefits of the proposed NV-FF compared to conventional ones are described in the following section.

2 NV-FF using DWM device

Fig. 1(a) shows the device structure of a DWM device [8, 9]. The tunnel barrier and the reference layer are stacked on the DWM region and an MTJ is formed. If the spin directions of the reference layer and the DWM layer are parallel, the resistance R_{MTJ} takes the low value R_P , and if they are anti-parallel, R_{MTJ} takes the high value R_{AP} . The stored data M can be programmed by applying a bi-directional write current I_{WR} between T2 and T3 as shown in Fig. 1(b). Thus, the DWM device can be regarded as a variable resistor which stores a binary data M as a resistance value R_M as shown in Fig. 1(c).

To perform CMOS compatible high-speed operation, some MTJ-based NV-FFs operate as CMOS D-FFs during the normal operation, and MTJ read/write accesses are performed just only before power-on/off [1, 4, 5, 6]. Fig. 2 shows the comparison of such MTJ-based NV-FFs in terms of the location of the write driver and the sense amplifier. Conventional NV-FFs

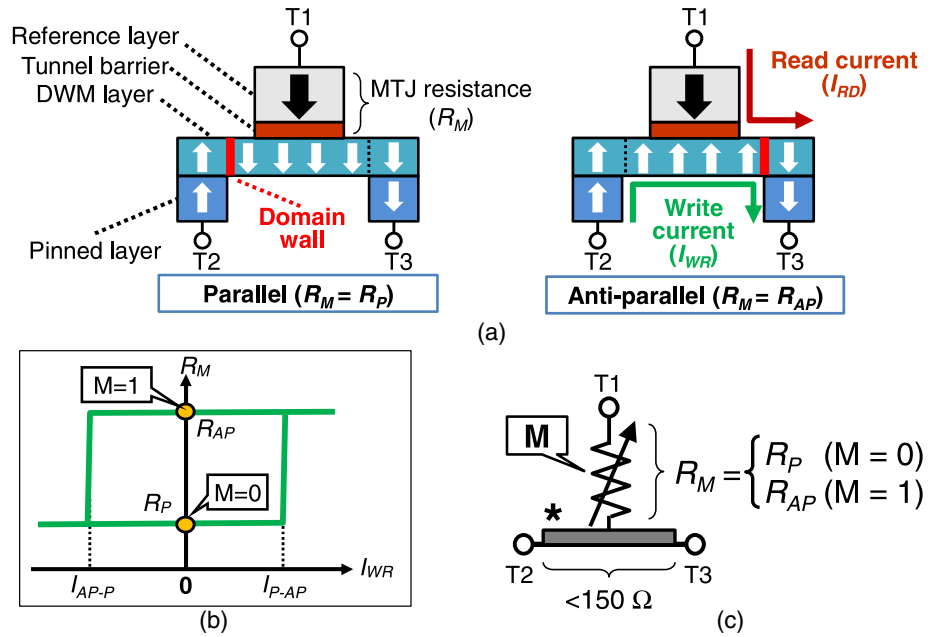


Fig. 1. DWM device: (a) Device structure. (b) Resistance versus current curve. (c) Schematic symbol.

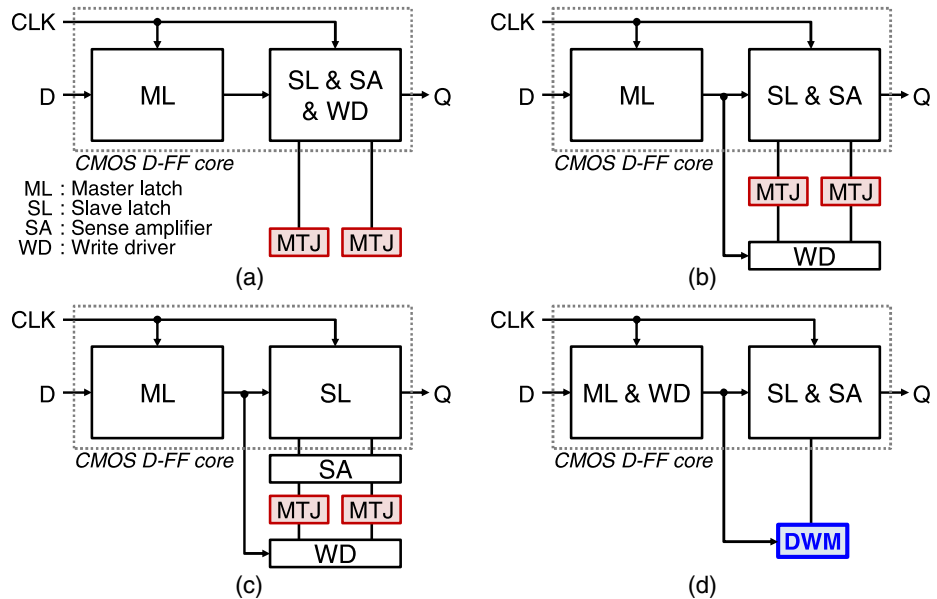


Fig. 2. MTJ-based NV-FFs: (a) Type 1 [4], (b) Type 2 [1, 6]. In [1], MTJ devices are replaced by DWM devices. (c) Type 3 [5], and (d) proposed.

utilize two MTJ devices where complementary data are programmed for achieving high sense margin. As shown in Fig. 2(a), Type 1 is a transistor-less structure since both the write driver and the sense amplifier are merged into the slave latch. However, the effective size of the slave latch must be enlarged to drive sufficient write current via high MTJ resistance. Moreover, it must be carefully designed due to the two-terminal nature of the STT-MTJ device; sufficient write current must be driven by the slave latch during the

store operation while read current must be limited during the recall operation to avoid read disturbance. To drive sufficient write current without such complex design space exploration, the write driver is separated from the slave latch in Type 2 as shown in Fig. 2(b). The drawbacks of Type 2 are the increase of transistor counts and the parasitic capacitance of the write driver which slows down the normal operation. As shown in Fig. 2(c), both the write driver and the sense amplifier are separated from the slave latch in Type 3. For the sake of transistor counts, the write driver and the sense amplifier are individually optimized and the parasitic capacitance due to the nonvolatile memory function blocks is reduced. Fig. 2(d) shows the proposed NV-FF structure where the write driver and the sense amplifier are merged into the master latch and the slave latch, respectively. By utilizing a DWM device, the read current path and the write current path are separated and the circuit structure is simplified.

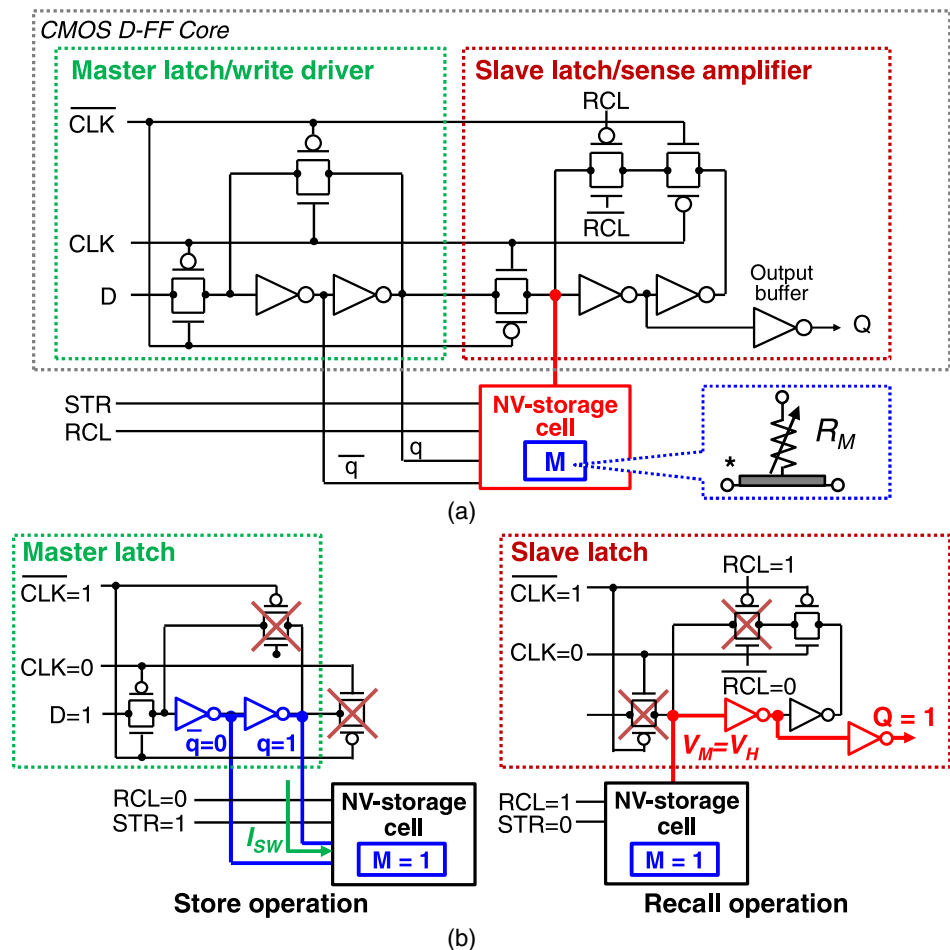


Fig. 3. Proposed NV-FF: (a) Schematic diagram. The NV-storage cell is electrically separated from the CMOS D-FF core during the normal operation. (b) Store and recall operations.

Fig. 3(a) shows a schematic diagram of the proposed NV-FF which is composed of a CMOS D-FF and an NV-storage cell using a DWM device. Two

inverters in the master latch are utilized as a write driver and those of in the slave latch are utilized as a sense amplifier, respectively. During the normal operation, STR and RCL become low and the NV-FF acts as a CMOS D-FF. Fig. 3(b) shows the store operation and the recall operation of the proposed NV-FF. During the store operation, STR becomes high and write current flows through the DWM device in accordance with the output of the master latch q . Since the resistance of the write current path in the DWM device is quite small, sufficient write current can be driven by small-size CMOS inverters, which also makes it possible to avoid the increase of active power dissipation. Note that, CLK is fixed low during the store operation to avoid a metastable output of the master latch propagating to the slave latch. During the recall operation, RCL becomes high and read voltage V_M is obtained in accordance with M ; when $M = 1$, V_M takes high value V_H , while it takes low value V_L when $M = 0$. V_M is amplified to a full-swing voltage signal by the two inverters in the slave latch (CLK is also set low during the recall operation).

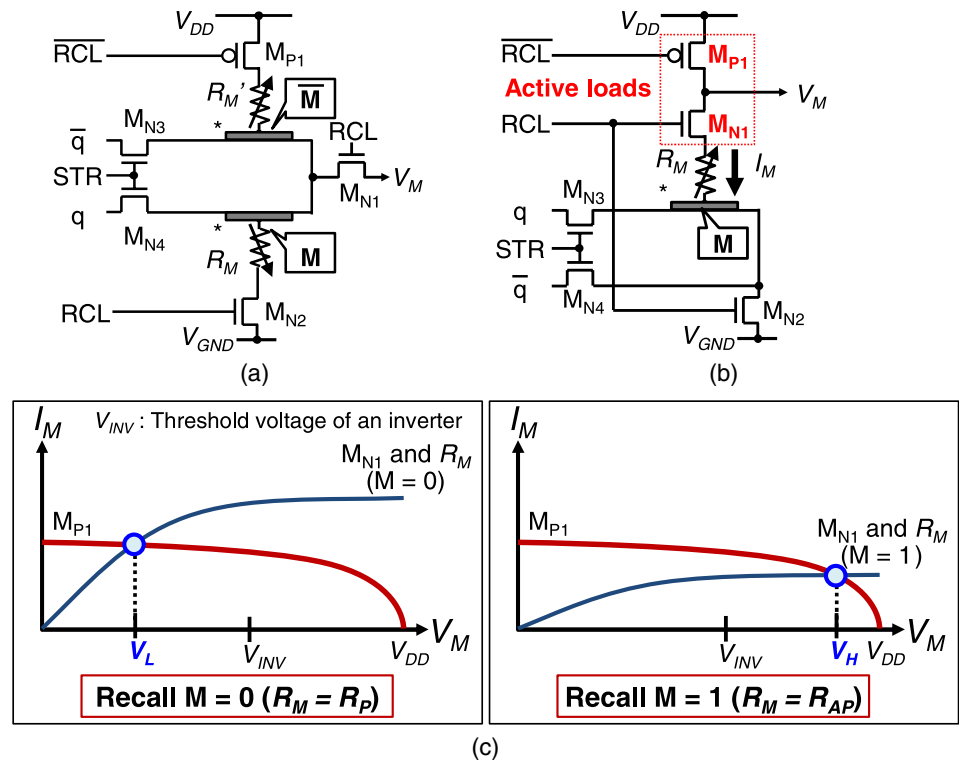


Fig. 4. NV-storage cell design: (a) Complementary DWM-based cell [11]. (b) Proposed cell. (c) Recall operation of the proposed cell.

To recall the stored data successfully, it is very important that the difference between V_H and V_L is sufficiently high. One possible way for achieving the high difference is to utilize complementary DWM-based sensing [11], where V_M is obtained by the voltage division between R_M and R_M' , as shown in Fig. 4(a). Since the resistance of the write current path is quite

small, two DWM devices are programmed by the same write current. In contrast to the complementary-DWM structure, only one DWM device is used in the proposed NV-storage cell as shown in Fig. 4(b). The bi-directional write current is driven via two NMOS transistors M_{N3} and M_{N4} during the store operation. During the recall operation, the PMOS transistor M_{P1} and the NMOS transistor M_{N1} are used as active loads. During the normal operation, they are turned off for separating the NV-storage cell from the slave latch. Fig. 4(c) shows the single-ended voltage sensing for the recall operation where voltage division between M_{P1} and M_{N1} together with R_M is used. The use of a PMOS load as well as an NMOS active load makes it possible to boost the difference between V_H and V_L [10]. They are tuned so that $(V_H + V_L)/2$ becomes the threshold voltage of the CMOS inverter V_{INV} in the slave latch. In this way, sufficient sense margin can be achieved just only one DWM device, which results in the reduction of write-error rate during store operation. If the write-error rate of the DWM device is defined as P_{WE} , the probability of the write fail in the complementary-DWM-based cell is expressed as

$$1 - (1 - P_{WE})^2 = P_{WE}(2 - P_{WE}). \quad (1)$$

Therefore probability of write fail in the proposed cell is $(2 - P_{WE})$ times lower than that of complementary-DWM-based one.

3 Evaluations

Table I. Device parameters for the evaluation.

	STT-MTJ device	DWM device
R_P [k Ω]	4.0	6.0
R_{AP} [k Ω]	9.0	13.5
$ I_{P-AP} $ [μ A]	110	100
$ I_{AP-P} $ [μ A]	60	100

For the evaluation, several types of MTJ-based NV-FFs are designed using 90 nm CMOS technology together with a SPICE simulator which supports a 2-terminal MTJ device model as well as a 3-terminal one [12, 13]. Instead of the junction size, the parameters such as MTJ resistance and write current of the MTJ model are directly specified by users. In this evaluation, the DWM device is implemented using the 3-terminal MTJ model. The parameters for the STT-MTJ device and the DWM device are summarized in Table I, that are estimated from 100 nm ϕ junction size with measurement results in [8, 9, 14]. Note that, I_{P-AP} and I_{AP-P} are the amounts of write current to program desired data in 2 ns.

Fig. 5 shows the simulated waveform of the proposed NV-FF where the measured V_H and V_L are 674 mV, 420 mV, respectively (V_{INV} is 543 mV). We can confirm that the proposed NV-FF operates as a standard CMOS D-FF

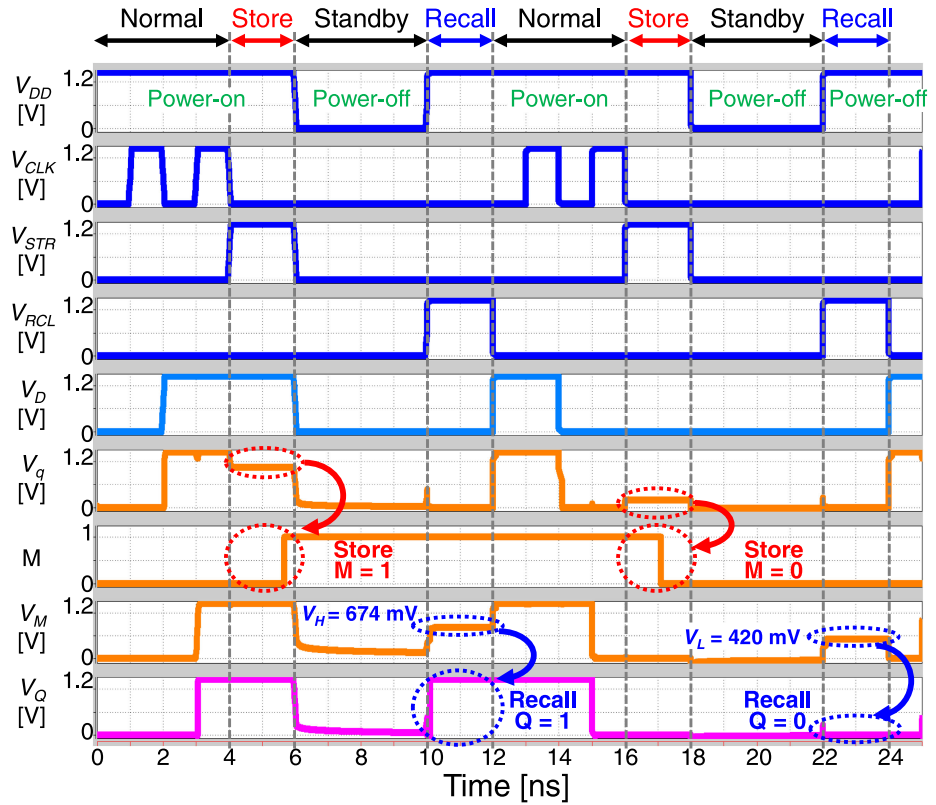


Fig. 5. Basic behavior. We can confirm that temporal data q is stored into the DWM device as M before power-off and it is recalled just after power-on.

during the normal operation, and temporal data q is stored into the DWM device as M before power-off and recalled just after power-on.

Table II summarizes comparison of a CMOS FF and five MTJ-based NV-FFs. While transistor counts of [4] are small, the effective area is large since CMOS inverters in the slave latch must be enlarged to drive sufficient write current, which results in large active power dissipation for the normal operation. The use of external write driver in [1, 6] also causes delay and power overheads due to additional gate capacitance of their write drivers. Separation of the write driver and the sensing circuit reduces the performance overhead [5], but area overhead is more than 2.5 time higher than that of the CMOS FF. In contrast, the proposed NV-FF exhibits the smallest area as well as power-delay product among the five NV-FFs. The reason for this result is that the CMOS D-FF is directly used for store and recall operations, and the NV-storage cell is electrically separated during the normal operation. The use of the DWM device also makes it possible to eliminate read disturbance since the read current path is separated from the write current path.

Table III summarizes the comparison of MTJ-based NV-FF characteristics. While previous works have zero-standby power capability by the use of the power gating technique, their standby power dissipations without the power gating technique are higher than that of the CMOS FF due to their peripheral circuits for store and recall operations. The amounts of the store energy in [4, 5, 6] are large since write current must be driven via high MTJ

Table II. Performance comparison (part 1).

	CMOS FF (volatile)	MTJ-based NV-FF (nonvolatile)				
		Type1 [4]	Type2 [1]	Type2 [6]	Type 3 [5]	Proposed
Transistor Counts ^(*)	22	27 ⁽²⁾	40	33	56	27
Area ⁽³⁾	1.00	1.62	1.75	1.56	2.69	1.38
Active power [μ W] ^(3,4)	12.3	15.1	16.5	17.7	14.3	12.7
Worst C-Q delay [ps] ⁽³⁾	63.9 (Rise)	74.6 (Rise)	72.5 (Rise)	73.9 (Fall)	61.0 (Rise)	62.2 (Rise)
Power-delay product [μ W*ps]	786	1149	1204	1308	872	790
MTJ type	N/A	STT	DWM	STT	STT	DWM
Read disturbance	N/A	Yes	No	Yes	Yes	No

(*)1 Transistor counts of a clock buffer is not included.

(*)2 An inverter is inserted for driving write current.

(*)3 A 90 nm CMOS technology (supply voltage $V_{DD} = 1.2$ V).

(*)4 Average power during normal operation at 1.0 GHz.

Table III. Performance comparison (part 2).

	CMOS FF (volatile)	MTJ-based NV-FF (nonvolatile)				
		Type1 [4]	Type2 [1]	Type2 [6]	Type 3 [5]	Proposed
Standby Power without PG ^(*) [nW]	24.6	33.9	46.7	67.9	68.0	24.3
Standby Power with PG ^(*) [nW]	N/A	0	0	0	0	0
Number of MTJ/DWM devices	0	2	2	2	2	1
Number of cycles for store operation	N/A	4	2	4	2	2
Store Energy [fJ] ^(*)	N/A	439	199	515	534	207
Recall Energy [fJ] ^(*)	N/A	102	101	124	85.3	60.4

(*)1 PG: Power-gating technique

(*)2 The pulse width of the clock signal is set 1 ns.

resistance and two STT-MTJ devices must be individually programmed. In terms of recall energy, [1], [4], [6] consume relatively high recall energy since these NV-FFs utilize differential current sensing and read currents flows through two STT-MTJ/DWM devices simultaneously. Meanwhile, the pro-

Table IV. Comparison of sense margin with [11].

	[11]	Proposed
V_H [mV]	671	674
V_L [mV]	419	420
$V_H - V_L$ [mV]	253	254

($V_{INV} = 543$ mV)

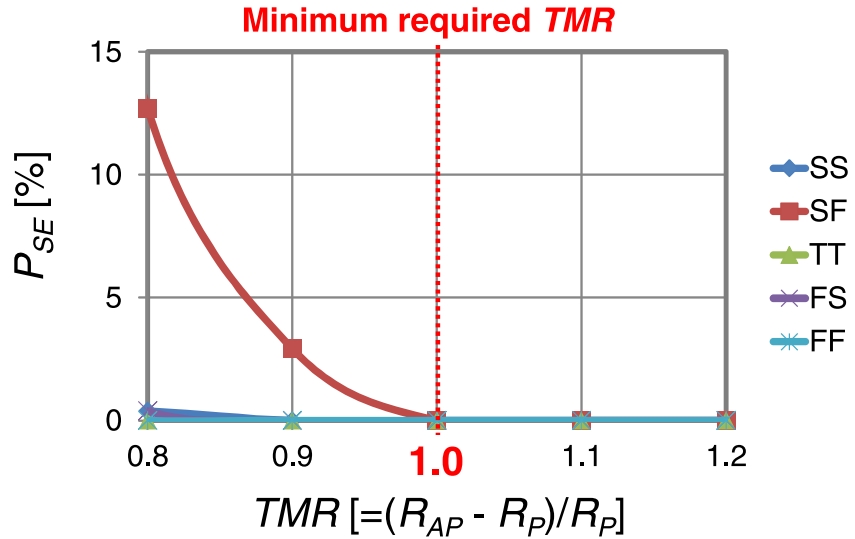


Fig. 6. The effect of MTJ resistance variation on sense error rate (P_{SE}). Both the standard deviations $\sigma R_P/R_P$ and $\sigma TMR/TMR$ [$TMR = (R_{AP} - R_P)/R_P$] are set 5% [15].

posed NV-FF exhibits the same degree of standby power dissipation without the power gating technique owing to its simplified circuitry. Moreover, the single-ended NV-storage cell structure make it possible to minimize the total energy for store and recall operations.

Table IV shows comparison of sense margin with [11]. By utilizing PMOS and NMOS active loads, the same degree of sense margin is achieved just only one DWM device in comparison with that of [11]. Fig. 6 shows the sense error rate P_{SE} in five process corners under MTJ resistance variation. Both of standard deviations $\sigma R_P/R_P$ and $\sigma TMR/TMR$ [$TMR = (R_{AP} - R_P)/R_P$] are set 5%, that are derived from measurement results [15]. Two capital letters such as ‘TT’ denote process corner of an NMOS transistor and that of a PMOS transistor (the letters F, T, S, correspond to *fast*, *typical*, *slow*, respectively). Because operating points are greatly moved to right relative to those of at the TT corner and V_L may exceed V_{INV} (see Fig. 4(c)), P_{SE} tends to be high at SF corner if TMR is low. As a result, minimum required TMR is estimated to be 100%, which can be easily realized in a current MTJ technology.

4 Conclusion

A compact, high-performance NV-FF using the DWM device has been proposed. Since the write current path is separated from the read current path in the DWM device, a write driver and a sense amplifier for store and recall operations are implemented just only CMOS inverters, which makes it possible to merge them into a CMOS D-FF core. Moreover, these functions are added without performance degradation since the nonvolatile storage cell is electrically separated from the CMOS D-FF core during the normal operation. As a result, both the area and the power-delay product of the proposed NV-FF are the smallest compared to those of conventional MTJ-based NV-FFs. As a next target, it is very important to apply the proposed NV-FF to various nonvolatile logic LSIs such as field-programmable gate arrays and processors.

Acknowledgments

This research is granted by the Japan Society for the Promotion of Science (JSPS) through the “Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program)”, initiated by the Council for Science and Technology Policy (CSTP). This research is also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence, Inc.